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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1812jbd144e

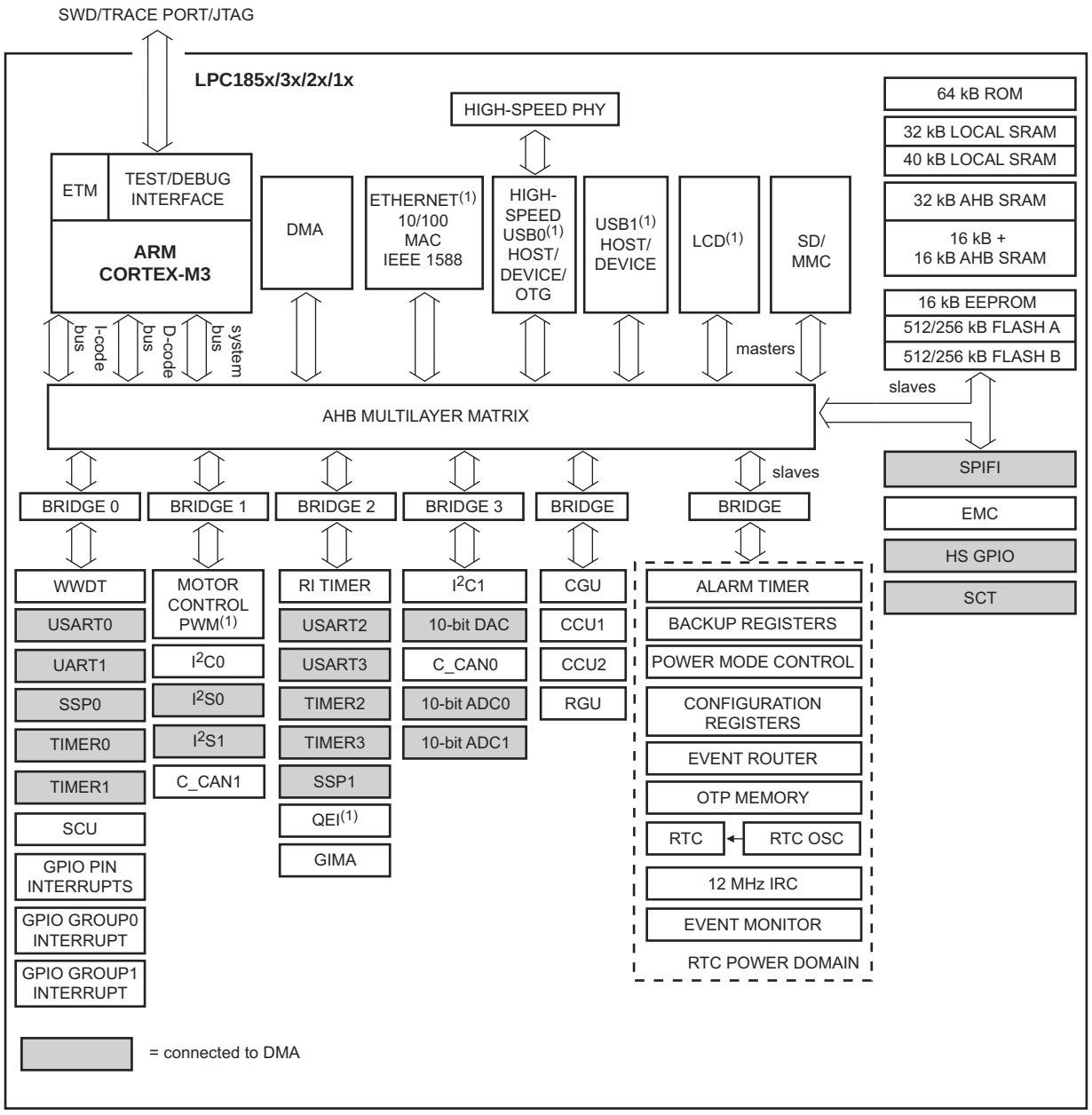
4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	Motor control PWM	QEI	ADC channels	Temperature range[1]	GPIO
LPC1857FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1857JET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1857JBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1853FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1853JET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1853JBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1837FET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1837JET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1837JBD144	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1837JET100	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1833FET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1833JET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1833JBD144	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1833JET100	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1827JBD144	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1827JET100	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1825JBD144	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1825JET100	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1823JBD144	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1823JET100	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1822JBD144	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1822JET100	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1817JBD144	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1817JET100	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1815JBD144	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1815JET100	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1813JBD144	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1813JET100	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	no	no	4	J	49
LPC1812JBD144	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1812JET100	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	no	no	4	J	49

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

5. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. LPC185x/3x/2x/1x block diagram

6. Pinning information

6.1 Pinning

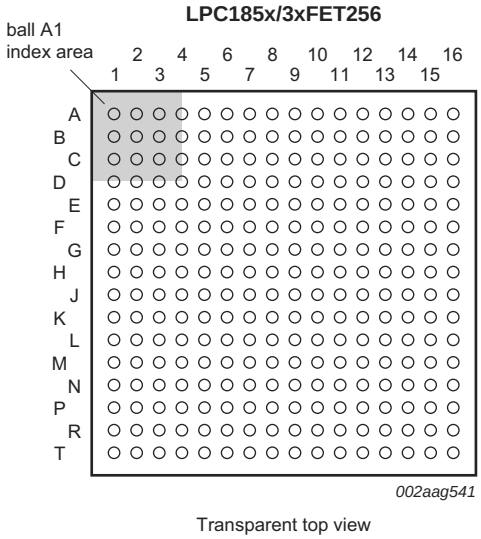


Fig 2. Pin configuration LBGA256 package

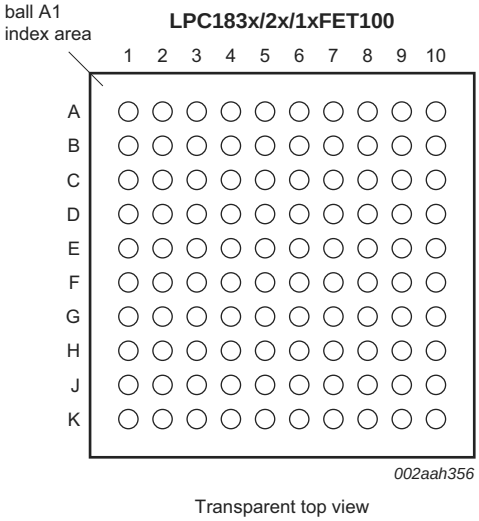


Fig 3. Pin configuration TFBGA100 package

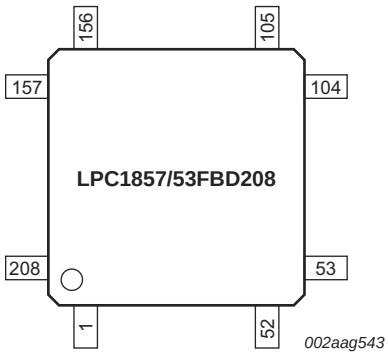


Fig 4. Pin configuration LQFP208 package

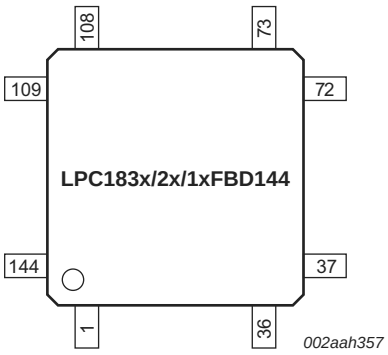


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC185x/3x/2x/1x, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the SCU registers.

The pin name is not indicative of the GPIO port assigned to it.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_5	R5	J4	48	65	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**EMC_CS0 —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**SD_POW —** SD/MMC card power monitor output.
P1_6	T4	K4	49	67	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**EMC_WE —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							O	**EMC_BLS0 —** LOW active Byte Lane select signal 0.
							-	**R —** Function reserved.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	G4	50	69	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_5	K14	D10	91	131	[3]	N; PU	-	**R —** Function reserved.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**GPIO5[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	G9	95	137	[2]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**EMC_A10 —** External memory address line 10.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[6] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
P2_7	H14	C10	96	138	[2]	N; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. ISP entry pin. If this pin is pulled LOW at reset, the part enters ISP mode or boots from an external source (see Table 4 and Table 5).
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**EMC_A9 —** External memory address line 9.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_6	C1	-	11	17	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P4_7	H4	-	14	21	[2]	O; PU	O	**LCD_DCLK —** LCD panel clock.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P4_8	E2	-	15	23	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							O	**LCD_VD9 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[12] —** General purpose digital input/output pin.
							O	**LCD_VD22 —** LCD data.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
P4_9	L2	-	33	48	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD11 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[13] —** General purpose digital input/output pin.
							O	**LCD_VD15 —** LCD data.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
WAKEUP0	A9	A4	130	187	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 0 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP1	A10	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 1 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP2	C9	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 2 of the event monitor. This pin does not have an internal pull-up.
WAKEUP3	D8	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration of at least 45 ns wakes up the part. This pin does not have an internal pull-up.
ADC pins								
ADC0_0/ ADC1_0/DAC	E3	A2	6	8	[8]	AI; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	A1	2	4	[8]	AI; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	143	206	[8]	AI; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	A3	139	200	[8]	AI; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	-	138	199	[8]	AI; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	-	144	208	[8]	AI; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	-	142	204	[8]	AI; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	-	136	197	[8]	AI; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC pins								
RTC_ALARM	A11	C3	129	186	[11]	-	O	RTC controlled output.
RTCX1	A8	A5	125	182	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B5	126	183	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
$\overline{\text{SAMPLE}}$	B9	-	-	-	[11]	O	O	Event monitor sample output.
Crystal oscillator pins								
XTAL1	D1	B1	12	18	[8]	-	I	Input to the oscillator circuit and internal clock generator circuits.

7.4 AHB multilayer matrix

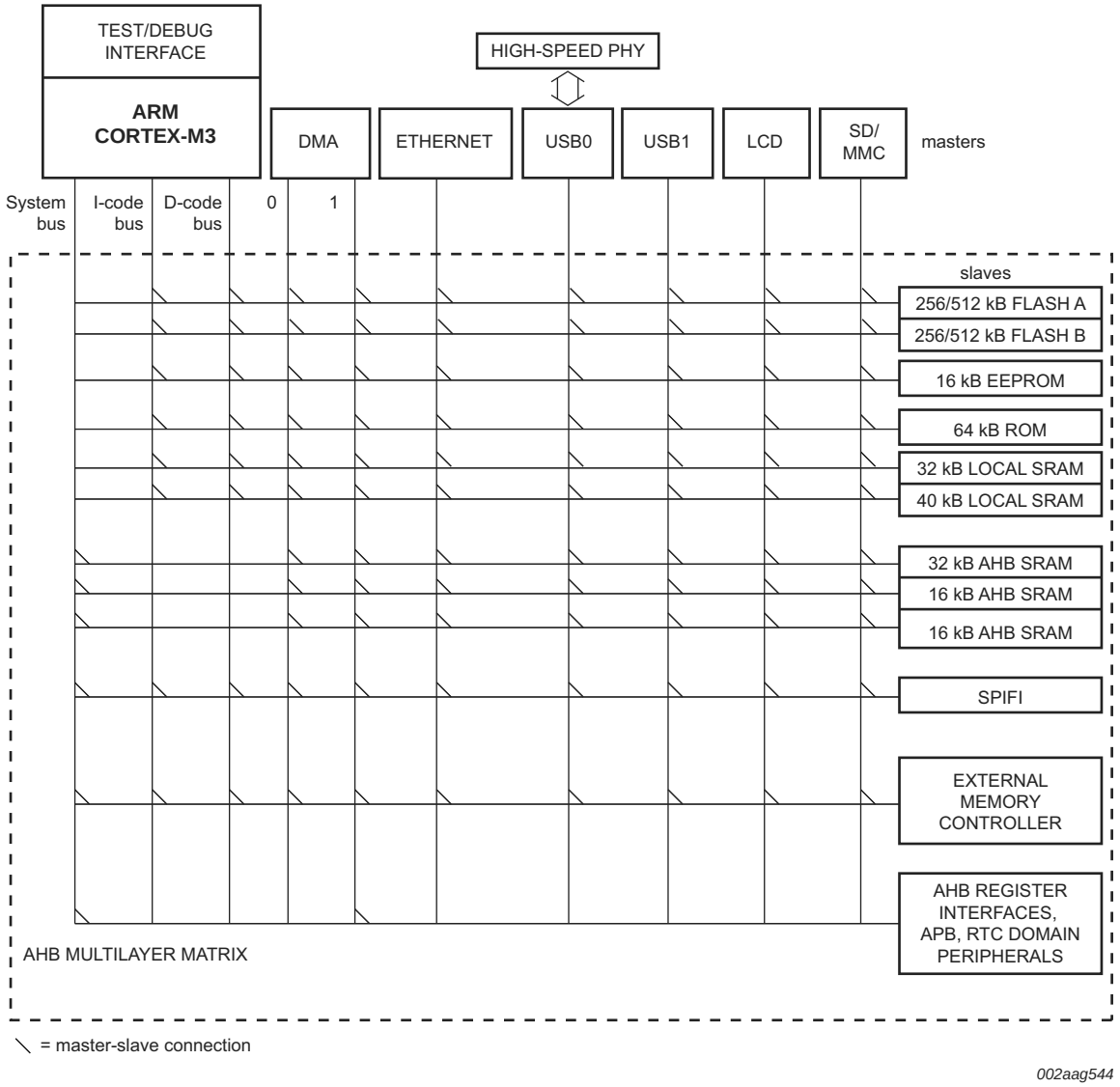


Fig 6. AHB multilayer matrix master and slave connections

7.5 Nested Vectored Interrupt Controller (NVIC)

The NVIC is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC185x/3x/2x/1x, the NVIC supports 53 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.

7.9 On-chip flash memory

The LPC185x/3x/2x/1x contain up to 1 MB of dual-bank flash program memory. With dual-bank flash memory, the user code can write or erase one flash bank while reading the other flash bank without interruption. A two-port flash accelerator maximizes the flash performance.

In-System Programming (ISP) and In-Application Programming (IAP) routines for programming the flash memory are provided in the Boot ROM.

7.10 EEPROM

The LPC185x/3x/2x/1x contain up to 16 kB of on-chip byte-erasable and byte-programmable EEPROM memory.

The EEPROM memory is divided into 128 pages. The user can access pages 1 through 127. Page 128 is protected.

7.11 Boot ROM

The internal ROM memory is used to store the boot code of the LPC185x/3x/2x/1x. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.
- Supports booting from external static memory such as NOR flash, SPI flash, quad SPI flash, USB0, and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

The default boot source is the flash memory. Several other boot modes are available if P2_7 is LOW on reset depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the states of the boot pins P2_9, P2_8, P1_2, and P1_1 determine the boot mode.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
Pin state	0	0	0	0	The reset state of P1_1, P1_2, P2_8, and P2_9 pins determines the boot source. See Table 5.
USART0	0	0	0	1	Enter ISP mode using USART0 functions on pins P2_0 and P2_1.
SPIFI	0	0	1	0	Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8.
EMC 8-bit	0	0	1	1	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.

- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines-wide static memory support.
- 16-bit and 32-bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs.
- Software-controlled dynamic memory self-refresh mode.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts.
- Separate reset domains allow auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.15.6 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on the following parts: LPC185x, LPC183x, LPC182x. USB0 is not available on the LPC181x parts.

The USB OTG module allows the part to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode.

7.15.6.1 Features

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.17 Counter/timers and motor control

7.17.1 General purpose 32-bit timers/external event counter

Remark: The LPC185x/3x/2x/1x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.17.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.17.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.17.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.17.3.1 Features

- Tracks encoder position.

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.
- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0. See Table 5.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.21 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_ DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	all peripherals disabled					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-	-	0.1	µA
I_{BAT}	battery supply current	Deep power-down mode; RTC running; $V_{DD(REG)(3V3)}$ floating; V_{BAT} = 3.3 V		-	3.0	-	µA
		$V_{DD(REG)(3V3)}$ = V_{BAT} = 3.3 V		-	1.5	-	µA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{BUS}	bus supply voltage		[17]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[18]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V. Special conditions for $V_{DD(REG)(3V3)}$ apply when writing to the flash and EEPROM. See Table 16 and Table 15.

[3] Pin VPP should either be not connected (when OTP does not need to be programmed) or tied to pins VDDIO and VDDREG to ensure the same ramp-up time for both supply voltages.

[4] $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V; T_{amb} = 25 °C.

[5] PLL1 disabled; IRC running; CCLK = 12 MHz.

[6] V_{BAT} = 3.6 V.

[7] T_{amb} = -40 °C to +105 °C; $V_{DD(IO)} = V_{DDA}$ = 3.6 V; over entire frequency range CCLK = 12 MHz to 180 MHz; in active mode, sleep mode; deep-sleep mode, power-down mode, and deep power-down mode.

[8] V_{ps} corresponds to the output of the power switch (see Figure 9) which is determined by the greater of V_{BAT} and $V_{DD(Reg)(3V3)}$.

[9] $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] To V_{SS}.

[12] The values specified are simulated and absolute values.

[13] The weak pull-up resistor is connected to the $V_{DD(IO)}$ rail and pulls up the I/O pin to the $V_{DD(IO)}$ level.

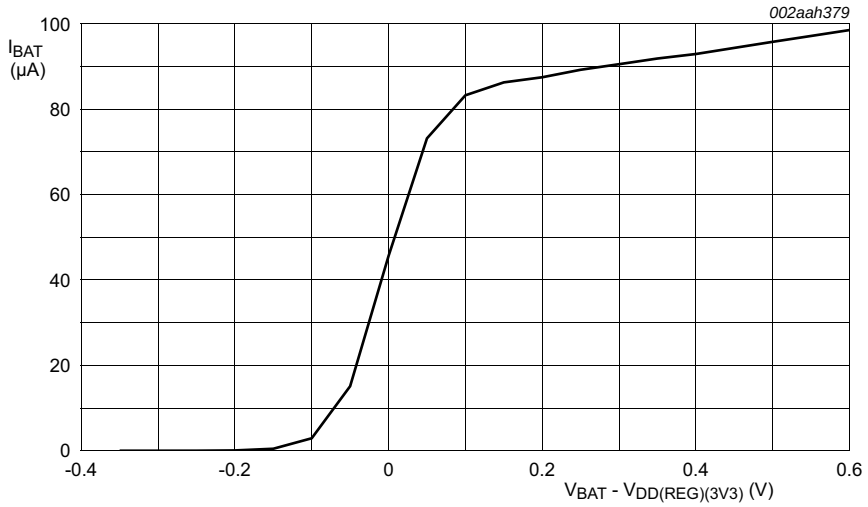
[14] The input cell disables the weak pull-up resistor when the applied input voltage exceeds $V_{DD(IO)}$.

[15] The parameter value specified is a simulated value excluding bond capacitance.

[16] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[17] $V_{DD(IO)}$ present.

[18] Includes external resistors of 33 Ω ± 1 % on D+ and D−.



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 2.6 V to 3.6 V; CCLK = 12 MHz.

Remark: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V.

Fig 18. Typical battery supply current in Active mode

10.2 Peripheral power consumption

The typical power consumption at T = 25 °C for each individual peripheral is measured as follows:

1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

Table 12. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
I2C1	CLK_APB3_I2C1	0.01	0.01
I2C0	CLK_APB1_I2C0	< 0.01	0.02
DAC	CLK_APB3_DAC	0.01	0.02
ADC0	CLK_APB3_ADC0	0.07	0.07
ADC1	CLK_APB3_ADC1	0.07	0.07
CAN0	CLK_APB3_CAN0	0.17	0.17
CAN1	CLK_APB1_CAN1	0.16	0.15
MOTOCON	CLK_APB1_MOTOCON	0.04	0.04
I2S	CLK_APB1_I2S	0.09	0.08
SPIFI	CLK_SPIFI, CLK_M3_SPIFI	1.14	2.29
GPIO	CLK_M3_GPIO	0.72	1.43

11.14 USB interface

Table 31. Dynamic characteristics: USB0 and USB1 pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(IO)}$, unless otherwise specified; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0	-	20.0	ns
t_f	fall time	10 % to 90 %		4.0	-	20.0	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111.11	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 35		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 35		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 35	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 35	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Remark: If only USB0 (HS USB) is used, the pins VDDREG and VDDIO can be at different voltages within the operating range but should have the same ramp up time. If USB1(FS USB) is used, the pins VDDREG and VDDIO should be a minimum of 3.0 V and be tied together.

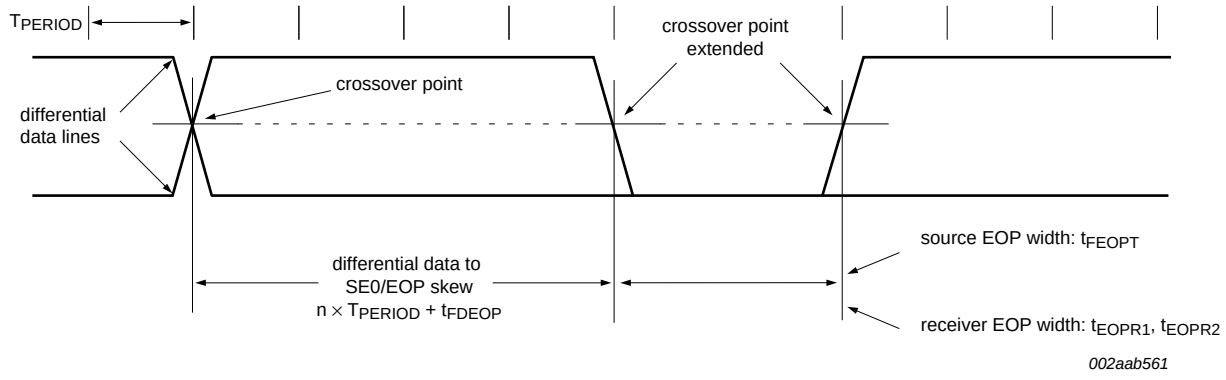


Fig 35. Differential data-to-EOP transition skew and EOP width

11.18 SPIFI

Table 36. Dynamic characteristics: SPIFI

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. C_L =20 pF. Sampled at 90 % and 10 % of the signal level. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	9.6	-	ns
t_{DS}	data set-up time	3.2	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	3.2	ns
$t_{h(Q)}$	data output hold time	0.6	-	ns

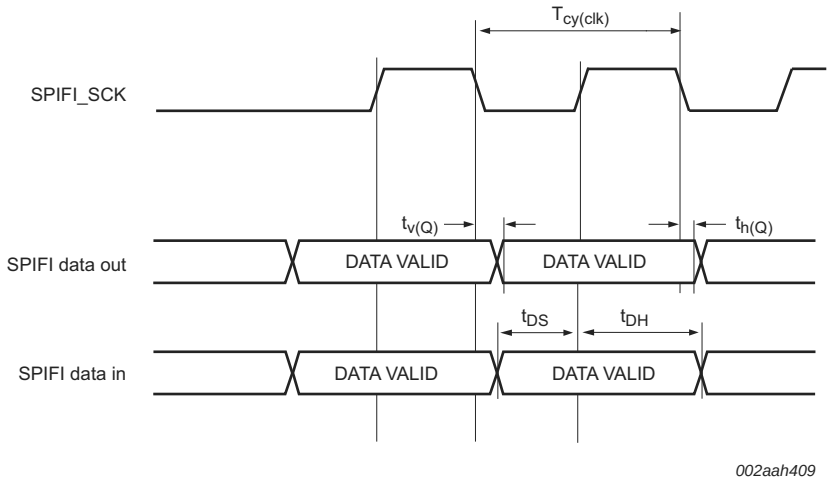


Fig 38. SPIFI timing (Mode 0)

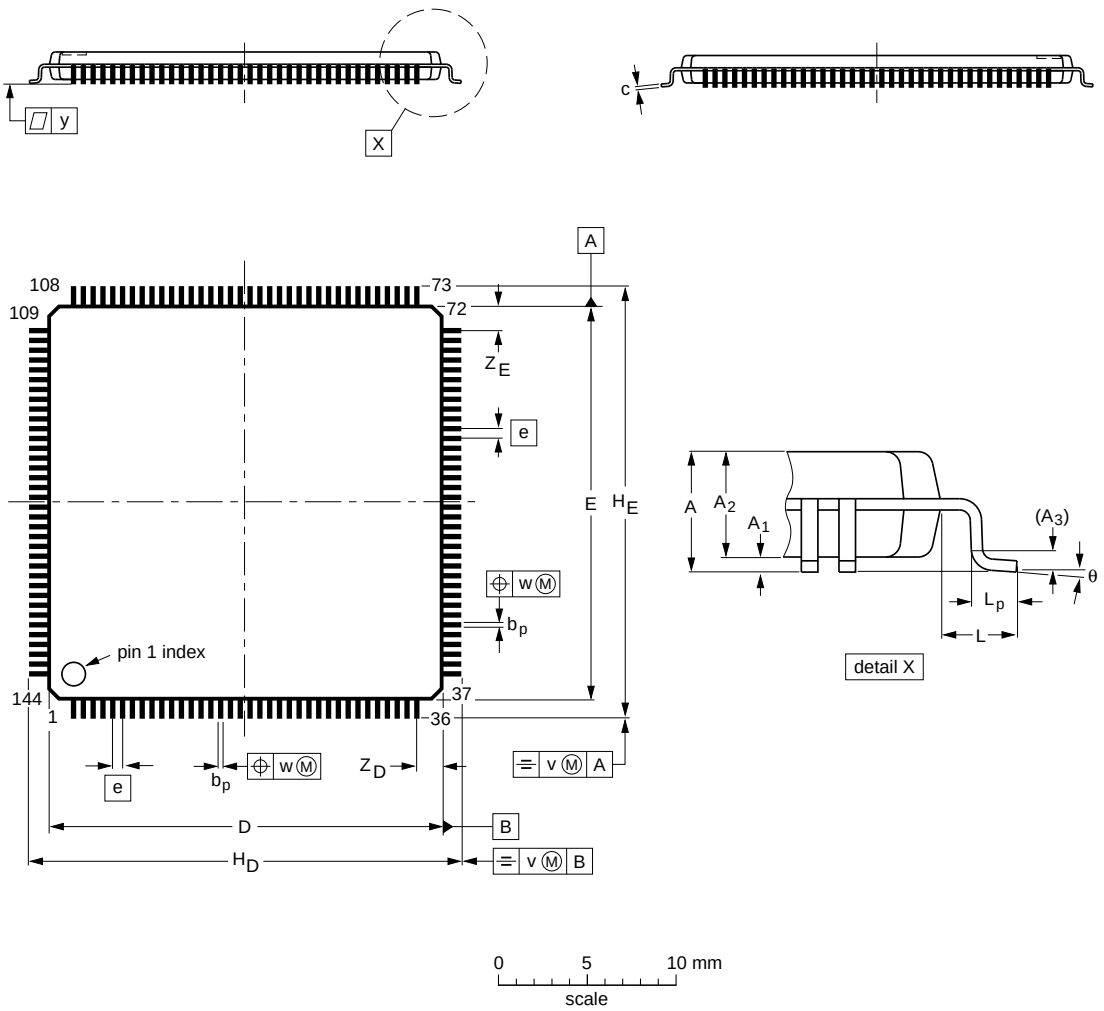
Table 40. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 41. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4		BLUE7
LCD_VD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3		BLUE6
LCD_VD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2		BLUE5
LCD_VD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1		BLUE4
LCD_VD19	-	-	P7_1	BLUE0	P7_1	BLUE0		BLUE3
LCD_VD18	-	-	-	-	P7_2	intensity		BLUE2
LCD_VD17	-	-	-	-	-	-	P7_3	BLUE1
LCD_VD16	-	-	-	-	-	-	P7_4	BLUE0
LCD_VD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCD_VD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCD_VD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCD_VD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCD_VD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCD_VD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCD_VD9	-	-	-	-	-	-	P4_8	GREEN1
LCD_VD8	-	-	-	-	-	-	P7_5	GREEN0
LCD_VD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCD_VD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCD_VD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCD_VD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4
LCD_VD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCD_VD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCD_VD1	-	-	-	-	-	-	P4_4	RED1

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 52. Package outline of the LQFP100 package

16. Abbreviations

Table 44. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
BGA	Ball Grid Array
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
GPIO	General-Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LQFP	Low Quad Flat Package
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OTG	On-The-Go
PHY	PHYsical layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface