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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | - |
| Speed | - |
| Connectivity | - |
| Peripherals | - |
| Number of I/O | - |
| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1813jbd144e |

- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 3 % accuracy over temperature and voltage (1.5 % accuracy for $T_{amb}$ = 0 °C to 85 °C).
- Ultra-low power RTC crystal oscillator.
- Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL can be used with the High-speed USB, the third PLL can be used as audio PLL.
- Clock output.

- Configurable digital peripherals:
  - State Configurable Timer/PWM (SCTimer/PWM) subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces:
  - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to an external high-speed PHY (USB1).
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Up to two C_CAN 2.0B controllers with one channel each.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One Fast-mode Plus $I^2C$-bus interface with monitor mode and with open-drain I/O pins conforming to the full $I^2C$-bus specification. Supports data rates of up to 1 Mbit/s.
  - One standard $I^2C$-bus interface with monitor mode and standard I/O pins.
  - Two $I^2S$ interfaces with DMA support, each with one input and one output.
- Digital peripherals:
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024H × 768V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - SD/MMC card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash total | Flash bank A | Flash bank B | Total SRAM | LCD | Ethernet | USB0 (Host, Device, OTG) | USB1 (Host, Device)/ ULPI interface | Motor control PWM | QEI | ADC channels | Temperature range[1] | GPIO |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LPC1857FET256 | 1 MB | 512 kB | 512 kB | 136 kB | yes | yes | yes | yes/yes | yes | yes | 8 | F | 164 |
| LPC1857JET256 | 1 MB | 512 kB | 512 kB | 136 kB | yes | yes | yes | yes/yes | yes | yes | 8 | J | 164 |
| LPC1857JBD208 | 1 MB | 512 kB | 512 kB | 136 kB | yes | yes | yes | yes/yes | yes | yes | 8 | J | 142 |
| LPC1853FET256 | 512 kB | 256 kB | 256 kB | 136 kB | yes | yes | yes | yes/yes | yes | yes | 8 | F | 164 |
| LPC1853JET256 | 512 kB | 256 kB | 256 kB | 136 kB | yes | yes | yes | yes/yes | yes | yes | 8 | J | 164 |
| LPC1853JBD208 | 512 kB | 256 kB | 256 kB | 136 kB | yes | yes | yes | yes/yes | yes | yes | 8 | J | 142 |
| LPC1837FET256 | 1 MB | 512 kB | 512 kB | 136 kB | no | yes | yes | yes/yes | yes | yes | 8 | F | 164 |
| LPC1837JET256 | 1 MB | 512 kB | 512 kB | 136 kB | no | yes | yes | yes/yes | yes | yes | 8 | J | 164 |
| LPC1837JBD144 | 1 MB | 512 kB | 512 kB | 136 kB | no | yes | yes | yes/yes | yes | no | 8 | J | 83 |
| LPC1837JET100 | 1 MB | 512 kB | 512 kB | 136 kB | no | yes | yes | yes/no | no | no | 4 | J | 49 |
| LPC1833FET256 | 512 kB | 256 kB | 256 kB | 136 kB | no | yes | yes | yes/yes | yes | yes | 8 | F | 164 |
| LPC1833JET256 | 512 kB | 256 kB | 256 kB | 136 kB | no | yes | yes | yes/yes | yes | yes | 8 | J | 164 |
| LPC1833JBD144 | 512 kB | 256 kB | 256 kB | 136 kB | no | yes | yes | yes/yes | yes | no | 8 | J | 83 |
| LPC1833JET100 | 512 kB | 256 kB | 256 kB | 136 kB | no | yes | yes | yes/no | no | no | 4 | J | 49 |
| LPC1827JBD144 | 1 MB | 512 kB | 512 kB | 136 kB | no | no | yes | no/no | yes | no | 8 | J | 83 |
| LPC1827JET100 | 1 MB | 512 kB | 512 kB | 136 kB | no | no | yes | no/no | no | no | 4 | J | 49 |
| LPC1825JBD144 | 768 kB | 384 kB | 384 kB | 136 kB | no | no | yes | no/no | yes | no | 8 | J | 83 |
| LPC1825JET100 | 768 kB | 384 kB | 384 kB | 136 kB | no | no | yes | no/no | no | no | 4 | J | 49 |
| LPC1823JBD144 | 512 kB | 256 kB | 256 kB | 104 kB | no | no | yes | no/no | yes | no | 8 | J | 83 |
| LPC1823JET100 | 512 kB | 256 kB | 256 kB | 104 kB | no | no | yes | no/no | no | no | 4 | J | 49 |
| LPC1822JBD144 | 512 kB | 512 kB | 0 kB | 104 kB | no | no | yes | no/no | yes | no | 8 | J | 83 |
| LPC1822JET100 | 512 kB | 512 kB | 0 kB | 104 kB | no | no | yes | no/no | no | no | 4 | J | 49 |
| LPC1817JBD144 | 1 MB | 512 kB | 512 kB | 136 kB | no | no | no | no/no | yes | no | 8 | J | 83 |
| LPC1817JET100 | 1 MB | 512 kB | 512 kB | 136 kB | no | no | no | no/no | no | no | 4 | J | 49 |
| LPC1815JBD144 | 768 kB | 384 kB | 384 kB | 136 kB | no | no | no | no/no | yes | no | 8 | J | 83 |
| LPC1815JET100 | 768 kB | 384 kB | 384 kB | 136 kB | no | no | no | no/no | no | no | 4 | J | 49 |
| LPC1813JBD144 | 512 kB | 256 kB | 256 kB | 104 kB | no | no | no | no/no | yes | no | 8 | J | 83 |
| LPC1813JET100 | 512 kB | 256 kB | 256 kB | 104 kB | no | no | no | no/no | no | no | 4 | J | 49 |
| LPC1812JBD144 | 512 kB | 512 kB | 0 kB | 104 kB | no | no | no | no/no | yes | no | 8 | J | 83 |
| LPC1812JET100 | 512 kB | 512 kB | 0 kB | 104 kB | no | no | no | no/no | no | no | 4 | J | 49 |

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP144 | LQFP208 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P4_10 | M3 | - | 35 | 51 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0. |
| | | | | | | | O | **LCD_VD10 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD14 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_0 | N3 | - | 37 | 53 | [2] | N; PU | I/O | **GPIO2[9] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOB2 —** Motor control PWM channel 2, output B. |
| | | | | | | | I/O | **EMC_D12 —** External memory data line 12. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART1. |
| | | | | | | | I | **T1_CAP0 —** Capture input 0 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_1 | P3 | - | 39 | 55 | [2] | N; PU | I/O | **GPIO2[10] —** General purpose digital input/output pin. |
| | | | | | | | I | **MCI2 —** Motor control PWM channel 2, input. |
| | | | | | | | I/O | **EMC_D13 —** External memory data line 13. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1. |
| | | | | | | | I | **T1_CAP1 —** Capture input 1 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_2 | R4 | - | 46 | 63 | [2] | N; PU | I/O | **GPIO2[11] —** General purpose digital input/output pin. |
| | | | | | | | I | **MCI1 —** Motor control PWM channel 1, input. |
| | | | | | | | I/O | **EMC_D14 —** External memory data line 14. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1. |
| | | | | | | | I | **T1_CAP2 —** Capture input 2 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP144 | LQFP208 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P6_3 | P15 | - | 79 | 113 | [2] | N; PU | I/O | **GPIO3[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_CS1 —** LOW active Chip Select 1 signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP2 —** Capture input 2 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_4 | R16 | F6 | 80 | 114 | [2] | N; PU | I/O | **GPIO3[3] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | O | **U0_TXD —** Transmitter output for USART0. |
| | | | | | | | O | **EMC_CAS —** LOW active SDRAM Column Address Strobe. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_5 | P16 | F9 | 82 | 117 | [2] | N; PU | I/O | **GPIO3[4] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1. |
| | | | | | | | I | **U0_RXD —** Receiver input for USART0. |
| | | | | | | | O | **EMC_RAS —** LOW active SDRAM Row Address Strobe. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_6 | L14 | - | 83 | 119 | [2] | N; PU | I/O | **GPIO0[5] —** General purpose digital input/output pin. |
| | | | | | | | O | **EMC_BLS1 —** LOW active Byte Lane select signal 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP3 —** Capture input 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP144 | LQFP208 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P6_11 | H12 | C9 | 101 | 143 | [2] | N; PU | I/O | **GPIO3[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_CKEOUT0 —** SDRAM clock enable 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T2_MAT3 —** Match output 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_12 | G15 | - | 103 | 145 | [2] | N; PU | I/O | **GPIO2[8] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P7_0 | B16 | - | 110 | 158 | [2] | N; PU | I/O | **GPIO3[8] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_LE —** Line end signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P7_1 | C14 | - | 113 | 162 | [2] | N; PU | I/O | **GPIO3[9] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3. |
| | | | | | | | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | O | **LCD_VD7 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U2_TXD —** Transmitter output for USART2. |
| | | | | | | | - | **R —** Function reserved. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP144 | LQFP208 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_8 | P8 | - | - | 74 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | I/O | **EMC_D22 —** External memory data line 22. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[22] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PD_9 | T11 | - | - | 84 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D23 —** External memory data line 23. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[23] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PD_10 | P11 | - | - | 86 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2. |
| | | | | | | | O | **$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[24] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PD_11 | N9 | - | - | 88 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **$\overline{\text{EMC\_CS3}}$ —** LOW active Chip Select 3 signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[25] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D0 —** ULPI link bidirectional data line 0. |
| | | | | | | | O | **CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP144 | LQFP208 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_3 | E10 | - | - | 170 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[18] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PF_4 | D10 | H4 | 120 | 172 | [2] | OL; PU | I/O | **SSP1_SCK —** Serial clock for SSP1. |
| | | | | | | | I | **GP_CLKIN —** General-purpose clock input to the CGU. |
| | | | | | | | O | **TRACECLK —** Trace clock. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S0_TX_MCLK —** $I^2S$ transmit master clock. |
| | | | | | | | I/O | **I2S0_RX_SCK —** $I^2S$ receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| PF_5 | E9 | - | - | 190 | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_UCLK —** Serial clock input/output for USART3 in synchronous mode. |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | O | **TRACEDATA[0] —** Trace data, bit 0. |
| | | | | | | | I/O | **GPIO7[19] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC1_4 —** ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |

# 7. Functional description

## 7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC185x/3x/2x/1x use a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals. Flexible connections allow different bus masters to access peripherals that are on different slave ports of the matrix simultaneously.

## 7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and low-power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual.

## 7.3 System Tick timer (SysTick)

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock can be generated from the peripheral clock, or from a clock input pin.

### 7.15.9 Ethernet

**Remark:** The ethernet controller is available on parts LPC185x and LPC183x. Ethernet is not available on parts LPC182x and LPC181x.

#### 7.15.9.1 Features

- 10/100 Mbit/s.
- DMA support.
- Power management remote wake-up frame and magic packet detection.
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Support for IEEE 1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

## 7.16 Digital serial peripherals

### 7.16.1 UART

**Remark:** The LPC185x/3x/2x/1x contain one UART with standard transmit and receive data lines.

UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

### 7.19.2 Event monitor/recorder

The event monitor/recorder allows recording and creating a time stamp of events related to the WAKEUP pins. Sensors report changes to the state of the WAKEUP pins, and the event monitor/recorder stores records of such events. The event recorder can be powered by the backup battery.

The event monitor/recorder can monitor the integrity of the device and record any tampering events.

#### 7.19.2.1 Features

- Supports three digital event inputs in the VBAT power domain.
- An event is defined as a level change at the digital event inputs.
- For each event channel, two timestamps mark the first and the last occurrence of an event. Each channel also has a dedicated counter tracking the total number of events. Timestamp values are taken from the RTC.
- Runs in VBAT power domain, independent of system power supply. The event/recorder/monitor can therefore operate in Deep power-down mode.
- Low power consumption.
- Interrupt available if system is running.
- A qualified event can be used as a wake-up trigger.
- State of event interrupts accessible by software through GPIO.

### 7.19.3 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt, if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

## 7.20 System control

### 7.20.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping

output frequency. The output frequency can be set as a multiple of the sampling frequency $f_s$ to $32 \times f_s$, $64 \times f_s$, $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, $512 \times f_s$ and the sampling frequency $f_s$ can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96,192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

### 7.20.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

### 7.20.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals.

### 7.20.9 Power control

The LPC185x/3x/2x/1x feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

# 9. Thermal characteristics

The average chip junction temperature, $T_j$ (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- $T_{amb}$ = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- $P_D$ = sum of internal and I/O power dissipation

The internal power dissipation is the product of $I_{DD(REG)(3V3)}$ and $V_{DD(REG)(3V3)}$. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

**Table 8. Thermal characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{j(max)}$ | maximum junction temperature | - | - | 125 | °C |

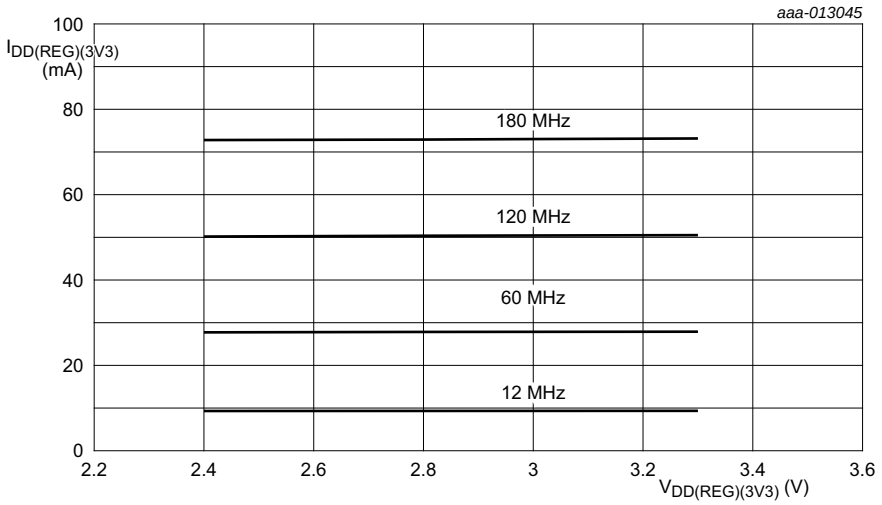
**Table 9. Thermal resistance (LQFP packages)**

| Symbol | Parameter | Conditions | Thermal resistance in °C/W ±15 % | |
|---|---|---|---|---|
| | | | LQFP144 | LQFP208 |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC (4.5 in × 4 in); still air | 38 | 31 |
| | | Single-layer (4.5 in × 3 in); still air | 50 | 39 |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | 11 | 10 |

**Table 10. Thermal resistance value (BGA packages)**

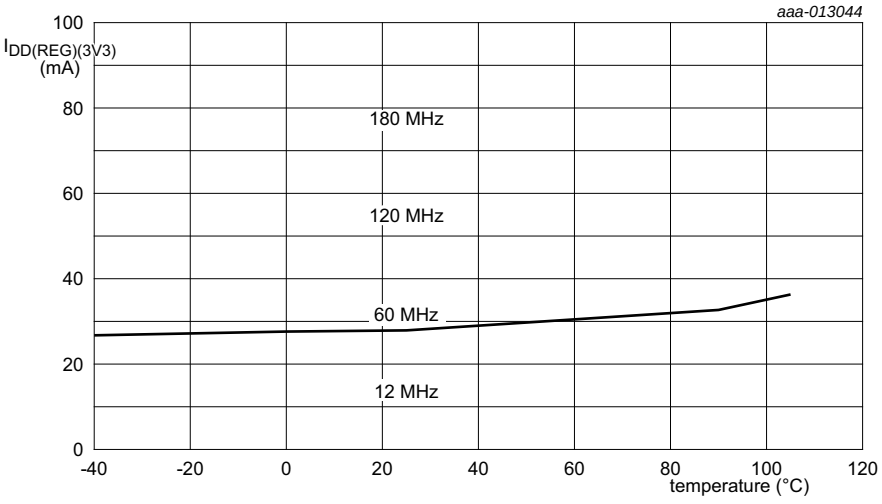
| Symbol | Parameter | Conditions | Thermal resistance in °C/W ±15 % | |
|---|---|---|---|---|
| | | | LBGA256 | TFBGA100 |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC (4.5 in × 4 in); still air | 29 | 46 |
| | | 8-layer (4.5 in × 3 in); still air | 24 | 37 |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | 14 | 11 |

## 10.1 Power consumption



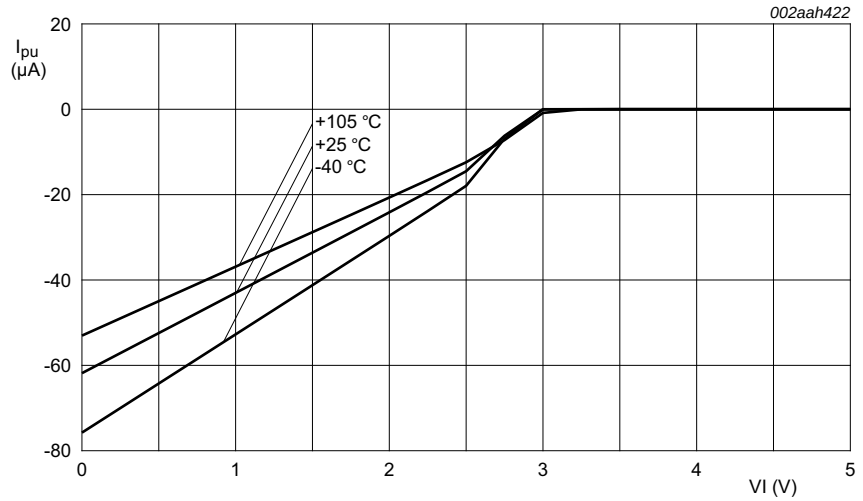

Conditions: $T_{amb}$ = 25 °C; executing code while (1){} from SRAM; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

**Fig 10. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode**



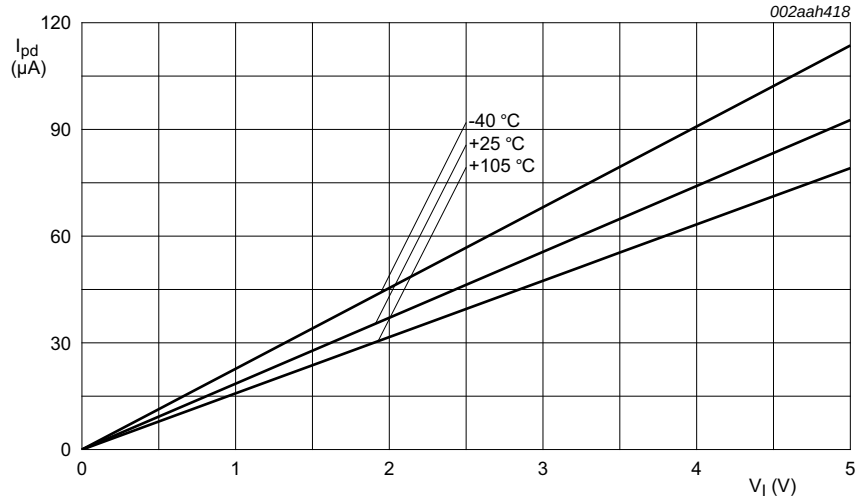

Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

**Fig 11. Typical supply current versus temperature in active mode**




Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

**Fig 23. Pull-up current $I_{pu}$ versus input voltage $V_I$**




Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

**Fig 24. Pull-down current $I_{pd}$ versus input voltage $V_I$**

## 11.13 External memory interface

**Table 28. Dynamic characteristics: Static asynchronous external memory interface**

*$C_L$ = 22 pF for EMC_Dn $C_L$ = 20 pF for all others; $T_{amb}$ = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register.Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted which results in multiple memory accesses.*

| Symbol | Parameter[1] | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Read cycle parameters** | | | | | | | |
| $t_{CSLAV}$ | $\overline{CS}$ LOW to address valid time | | | −3.1 | - | 1.6 | ns |
| $t_{CSLOEL}$ | $\overline{CS}$ LOW to $\overline{OE}$ LOW time | | [2] | −0.6 + $T_{cy(clk)}$ × WAITOEN | - | 1.3 + $T_{cy(clk)}$ × WAITOEN | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW time | PB = 1 | | −0.7 | - | 1.8 | ns |
| $t_{OELOEH}$ | $\overline{OE}$ LOW to $\overline{OE}$ HIGH time | | [2] | −0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ | - | −0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{am}$ | memory access time | | | - | - | −16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$ | ns |
| $t_{h(D)}$ | data input hold time | | | −16 | - | - | ns |
| $t_{CSHBLSH}$ | $\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time | PB = 1 | | −0.4 | - | 1.9 | ns |
| $t_{CSHOEH}$ | CS HIGH to $\overline{OE}$ HIGH time | | | −0.4 | - | 1.4 | ns |
| $t_{OEHANV}$ | $\overline{OE}$ HIGH to address invalid | PB = 1 | | −2.0 | - | 2.6 | ns |
| $t_{CSHEOR}$ | $\overline{CS}$ HIGH to end of read time | | [3] | −2.0 | - | 0 | ns |
| $t_{CSLSOR}$ | $\overline{CS}$ LOW to start of read time | | [4] | 0 | - | 1.8 | ns |
| **Write cycle parameters** | | | | | | | |
| $t_{CSLAV}$ | $\overline{CS}$ LOW to address valid time | | | −3.1 | - | 1.6 | ns |
| $t_{CSLDV}$ | $\overline{CS}$ LOW to data valid time | | | −3.1 | - | 1.5 | ns |
| $t_{CSLWEL}$ | $\overline{CS}$ LOW to $\overline{WE}$ LOW time | PB = 1 | | −1.5 + (WAITWEN + 1) × $T_{cy(clk)}$ | - | 0.2 + (WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW time | PB = 1 | | −0.7 | - | 1.8 | ns |
| $t_{WELWEH}$ | $\overline{WE}$ LOW to $\overline{WE}$ HIGH time | PB = 1 | [2] | −0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ | - | −0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{WEHDNV}$ | $\overline{WE}$ HIGH to data invalid time | PB = 1 | [2] | −0.9 + $T_{cy(clk)}$ | - | 2.3 + $T_{cy(clk)}$ | ns |
| $t_{WEHEOW}$ | $\overline{WE}$ HIGH to end of write time | PB = 1 | [2] [5] | −0.4 + $T_{cy(clk)}$ | - | −0.3 + $T_{cy(clk)}$ | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW | PB = 0 | | −0.7 + (WAITWEN + 1) × $T_{cy(clk)}$ | - | 1.8 + (WAITWEN + 1) × $T_{cy(clk)}$ | ns |

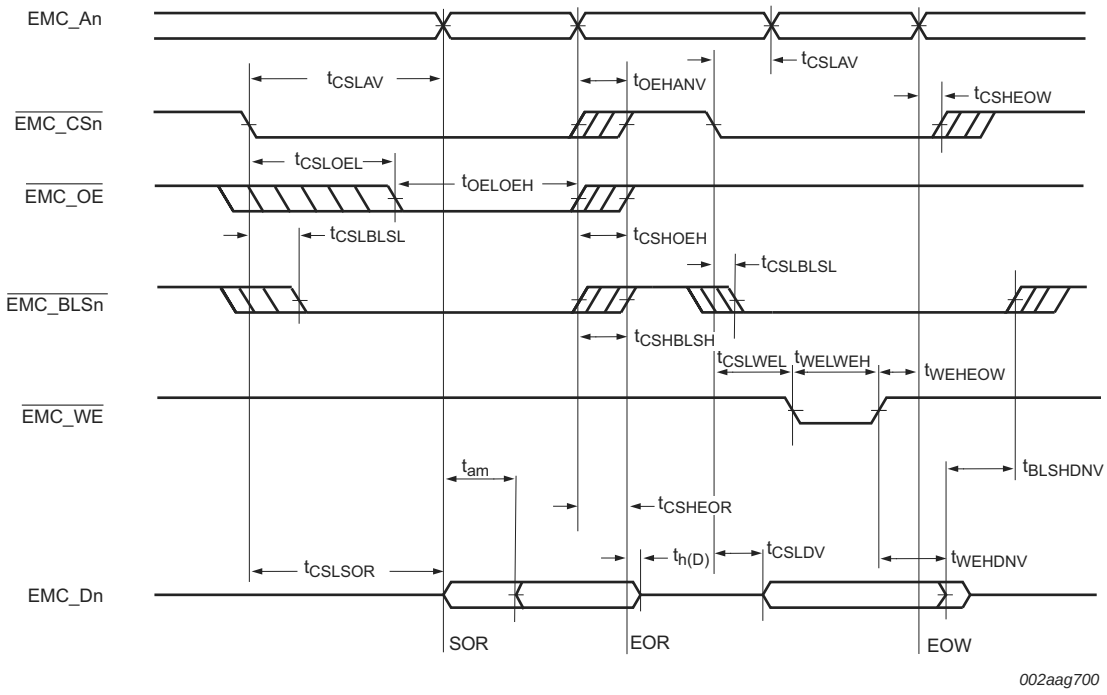
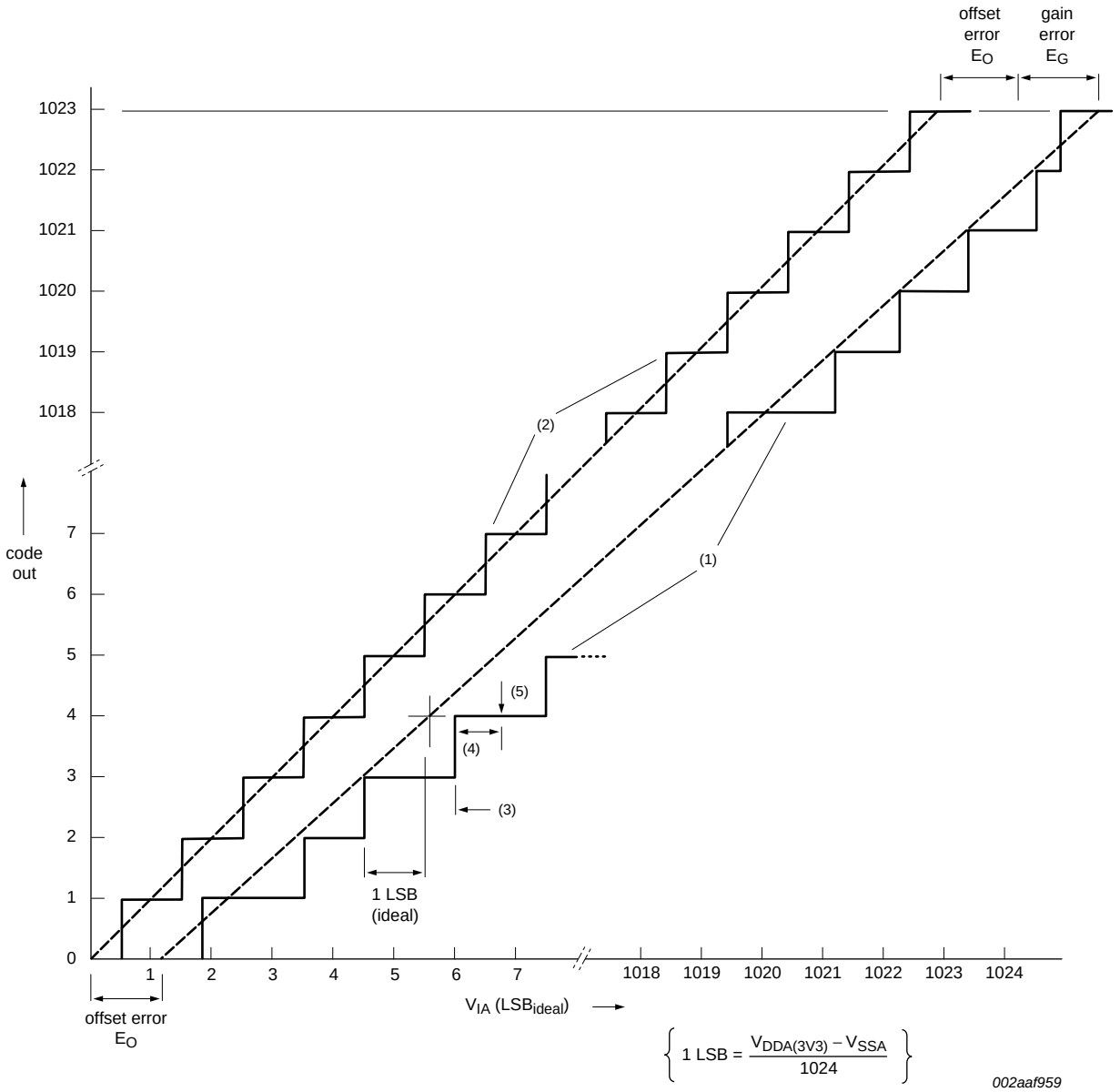



**Fig 33. External static memory read/write access (PB = 1)**




(1) Example of an actual transfer curve.

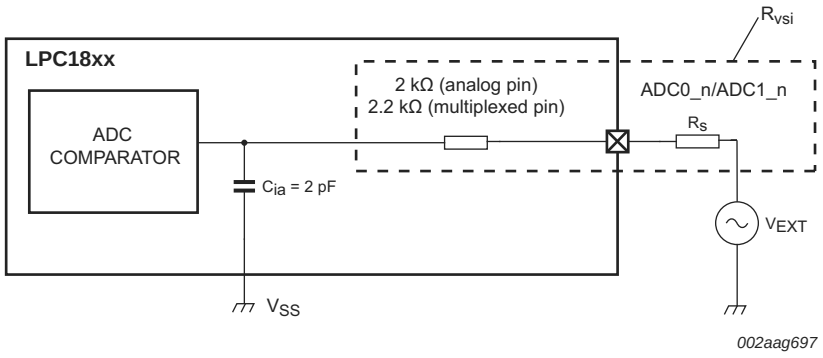
(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 39. 10-bit ADC characteristics**




$R_s < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

**Fig 40. ADC interface to pins**

**Table 38. DAC characteristics**

*$V_{DDA(3V3)}$ over specified ranges; $T_{amb}$ = −40 °C to +105 °C; unless otherwise specified*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $E_D$ | differential linearity error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [1] | - | ±0.8 | - | LSB |
| | | 2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±1.0 | - | LSB |
| $E_{L(adj)}$ | integral non-linearity | code = 0 to 975<br>2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [1] | - | ±1.0 | - | LSB |
| | | 2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±1.5 | - | LSB |
| $E_O$ | offset error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [1] | - | ±0.8 | - | LSB |
| | | 2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±1.0 | - | LSB |
| $E_G$ | gain error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [1] | - | ±0.3 | - | % |
| | | 2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±1.0 | - | % |
| $C_L$ | load capacitance | | | - | - | 200 | pF |
| $R_L$ | load resistance | | | 1 | - | - | kΩ |
| $t_s$ | settling time | | [2] | | 0.4 | | μS |

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC18xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

**Table 45. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC1857_53 v.3.1 | 20120904 | Preliminary data sheet | - | LPC1857_53 v.3 |
| Modifications: | • SSP0 boot pin functions added in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI.<br>• Peripheral power consumption data added in Table 12.<br>• BOD de-assertion levels add in Table 13.<br>• Minimum value for all supply voltages changed to -0.5 V n Table 7. | | | |
| LPC1857_53 v.3 | 20120711 | Preliminary data sheet | - | LPC1857_53 v.2 |
| Modifications: | • Data sheet status changed to preliminary.<br>• AES removed. Available on parts LPC18Sxx only.<br>• Minimum value of $V_I$ for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”, “USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6.<br>• Dynamic characteristics of the SD/MMC controller updated in Table 29.<br>• Dynamic characteristics of the LCD controller updated in Table 30.<br>• Dynamic characteristics of the SSP controller updated in Table 22.<br>• Section 10.2 added.<br>• Table 8 “Thermal resistance value (BGA packages)” added.<br>• Description of pins USB1_DP and USB1_DM updated in Table 3.<br>• Editorial updates.<br>• Parameters $I_{IL}$ and $I_{IH}$ renamed to $I_{LL}$ and $I_{LH}$ in Table 9. | | | |
| LPC1857_53 v.2 | 20120515 | Objective data sheet | - | LPC1857_53 v.1 |
| LPC1857_53 v.1 | 20111214 | Objective data sheet | - | - |

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## 19.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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