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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1815jbd144e

4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	Motor control PWM	QEI	ADC channels	Temperature range ^[1]	GPIO
LPC1857FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1857JET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1857JBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1853FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1853JET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1853JBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1837FET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1837JET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1837JBD144	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1837JET100	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1833FET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1833JET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1833JBD144	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1833JET100	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1827JBD144	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1827JET100	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1825JBD144	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1825JET100	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1823JBD144	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1823JET100	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1822JBD144	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1822JET100	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1817JBD144	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1817JET100	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1815JBD144	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1815JET100	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1813JBD144	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1813JET100	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	no	no	4	J	49
LPC1812JBD144	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1812JET100	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	no	no	4	J	49

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_5	R5	J4	48	65	[2]	N; PU	I/O	GPIO1[8] — General purpose digital input/output pin.
							O	CTOUT_10 — SCTimer/PWM output 10. Match output 3 of timer 3.
							-	R — Function reserved.
							O	EMC_CS0 — LOW active Chip Select 0 signal.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	SSP1_SSEL — Slave Select for SSP1.
							-	R — Function reserved.
							O	SD_POW — SD/MMC card power monitor output.
P1_6	T4	K4	49	67	[2]	N; PU	I/O	GPIO1[9] — General purpose digital input/output pin.
							I	CTIN_5 — SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	R — Function reserved.
							O	EMC_WE — LOW active Write Enable signal.
							-	R — Function reserved.
							O	EMC_BLS0 — LOW active Byte Lane select signal 0.
							-	R — Function reserved.
							I/O	SD_CMD — SD/MMC command signal.
P1_7	T5	G4	50	69	[2]	N; PU	I/O	GPIO1[0] — General purpose digital input/output pin.
							I	U1_DSR — Data Set Ready input for UART1.
							O	CTOUT_13 — SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	EMC_D0 — External memory data line 0.
							O	USB0_PPWR — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_12	R9	K7	56	78	[2]	N; PU	I/O	GPIO1[5] — General purpose digital input/output pin.
							I	U1_DCD — Data Carrier Detect input for UART1.
							-	R — Function reserved.
							I/O	EMC_D5 — External memory data line 5.
							I	T0_CAP1 — Capture input 1 of timer 0.
							-	R — Function reserved.
							-	R — Function reserved.
P1_13	R10	H8	60	83	[2]	N; PU	I/O	GPIO1[6] — General purpose digital input/output pin.
							O	U1_TXD — Transmitter output for UART1.
							-	R — Function reserved.
							I/O	EMC_D6 — External memory data line 6.
							I	T0_CAP0 — Capture input 0 of timer 0.
							-	R — Function reserved.
							-	R — Function reserved.
P1_14	R11	J8	61	85	[2]	N; PU	I/O	GPIO1[7] — General purpose digital input/output pin.
							I	U1_RXD — Receiver input for UART1.
							-	R — Function reserved.
							I/O	EMC_D7 — External memory data line 7.
							O	T0_MAT2 — Match output 2 of timer 0.
							-	R — Function reserved.
							-	R — Function reserved.
P1_15	T12	K8	62	87	[2]	N; PU	I/O	GPIO0[2] — General purpose digital input/output pin.
							O	U2_TXD — Transmitter output for USART2.
							-	R — Function reserved.
							I	ENET_RXD0 — Ethernet receive data 0 (RMII/MII interface).
							O	T0_MAT1 — Match output 1 of timer 0.
							-	R — Function reserved.
							I/O	EMC_D8 — External memory data line 8.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_2	M15	F5	84	121	[2]	N; PU	-	R — Function reserved.
							I/O	U0_UCLK — Serial clock input/output for USART0 in synchronous mode.
							I/O	EMC_A11 — External memory address line 11.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							I/O	GPIO5[2] — General purpose digital input/output pin.
							I	CTIN_6 — SCTimer/PWM input 6. Capture input 1 of timer 3.
							I	T3_CAP2 — Capture input 2 of timer 3.
P2_3	J12	D8	87	127	[3]	N; PU	O	EMC_CS1 — LOW active Chip Select 1 signal.
							-	R — Function reserved.
							I/O	I2C1_SDA — I ² C1 data input/output (this pin does not use a specialized I ² C pad).
							O	U3_TXD — Transmitter output for USART3. See Table 4 for ISP mode.
							I	CTIN_1 — SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	GPIO5[3] — General purpose digital input/output pin.
							-	R — Function reserved.
P2_4	K11	D9	88	128	[3]	N; PU	O	T3_MAT0 — Match output 0 of timer 3.
							O	USB0_PPWR — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	R — Function reserved.
							I/O	I2C1_SCL — I ² C1 clock input/output (this pin does not use a specialized I ² C pad).
							I	U3_RXD — Receiver input for USART3. See Table 4 for ISP mode.
							I	CTIN_0 — SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	GPIO5[4] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT1 — Match output 1 of timer 3.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_12	E15	B9	106	153	[2]	N; PU	I/O	GPIO1[12] — General purpose digital input/output pin.
							O	CTOUT_4 — SCTimer/PWM output 4. Match output 3 of timer 3.
							-	R — Function reserved.
							I/O	EMC_A3 — External memory address line 3.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P2_13	C16	A10	108	156	[2]	N; PU	I/O	GPIO1[13] — General purpose digital input/output pin.
							I	CTIN_4 — SCTimer/PWM input 4. Capture input 2 of timer 1.
							-	R — Function reserved.
							I/O	EMC_A4 — External memory address line 4.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P3_0	F13	A8	112	161	[2]	N; PU	I/O	I2S0_RX_SCK — I ² S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the <i>I²S-bus specification</i> .
							O	I2S0_RX_MCLK — I ² S receive master clock.
							I/O	I2S0_TX_SCK — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the <i>I²S-bus specification</i> .
							O	I2S0_TX_MCLK — I ² S transmit master clock.
							I/O	SSP0_SCK — Serial clock for SSP0.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P5_3	T8	-	54	76	[2]	N; PU	I/O	GPIO2[12] — General purpose digital input/output pin.
							I	MCI0 — Motor control PWM channel 0, input.
							I/O	EMC_D15 — External memory data line 15.
							-	R — Function reserved.
							I	U1_RI — Ring Indicator input for UART1.
							I	T1_CAP3 — Capture input 3 of timer 1.
							-	R — Function reserved.
							-	R — Function reserved.
P5_4	P9	-	57	80	[2]	N; PU	I/O	GPIO2[13] — General purpose digital input/output pin.
							O	MCOB0 — Motor control PWM channel 0, output B.
							I/O	EMC_D8 — External memory data line 8.
							-	R — Function reserved.
							I	U1_CTS — Clear to Send input for UART1.
							O	T1_MAT0 — Match output 0 of timer 1.
							-	R — Function reserved.
P5_5	P10	-	58	81	[2]	N; PU	I/O	GPIO2[14] — General purpose digital input/output pin.
							O	MCOA1 — Motor control PWM channel 1, output A.
							I/O	EMC_D9 — External memory data line 9.
							-	R — Function reserved.
							I	U1_DCD — Data Carrier Detect input for UART1.
							O	T1_MAT1 — Match output 1 of timer 1.
							-	R — Function reserved.
P5_6	T13	-	63	89	[2]	N; PU	I/O	GPIO2[15] — General purpose digital input/output pin.
							O	MCOB1 — Motor control PWM channel 1, output B.
							I/O	EMC_D10 — External memory data line 10.
							-	R — Function reserved.
							O	U1_TXD — Transmitter output for UART1.
							O	T1_MAT2 — Match output 2 of timer 1.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P5_7	R12	-	65	91	[2]	N; PU	I/O	GPIO2[7] — General purpose digital input/output pin.
							O	MCOA2 — Motor control PWM channel 2, output A.
							I/O	EMC_D11 — External memory data line 11.
							-	R — Function reserved.
							I	U1_RXD — Receiver input for UART1.
							O	T1_MAT3 — Match output 3 of timer 1.
							-	R — Function reserved.
							-	R — Function reserved.
P6_0	M12	H7	73	105	[2]	N; PU	-	R — Function reserved.
							O	I2S0_RX_MCLK — I ² S receive master clock.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	I2S0_RX_SCK — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the <i>I²S-bus specification</i> .
							-	R — Function reserved.
							-	R — Function reserved.
P6_1	R15	G5	74	107	[2]	N; PU	I/O	GPIO3[0] — General purpose digital input/output pin.
							O	EMC_DYCS1 — SDRAM chip select 1.
							I/O	U0_UCLK — Serial clock input/output for USART0 in synchronous mode.
							I/O	I2S0_RX_WS — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the <i>I²S-bus specification</i> .
							-	R — Function reserved.
							I	T2_CAP0 — Capture input 2 of timer 2.
							-	R — Function reserved.
P6_2	L13	J9	78	111	[2]	N; PU	I/O	GPIO3[1] — General purpose digital input/output pin.
							O	EMC_CKEOUT1 — SDRAM clock enable 1.
							I/O	U0_DIR — RS-485/EIA-485 output enable/direction control for USART0.
							I/O	I2S0_RX_SDA — I ² S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the <i>I²S-bus specification</i> .
							-	R — Function reserved.
							I	T2_CAP1 — Capture input 1 of timer 2.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PC_3	F5	-	-	11	[5]	N; PU	I/O	USB1_ULPI_D5 — ULPI link bidirectional data line 5.
							-	R — Function reserved.
							O	U1_RTS — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	ENET_TXD3 — Ethernet transmit data 3 (MII interface).
							I/O	GPIO6[2] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							O	SD_VOLT1 — SD/MMC bus voltage select output 1.
PC_4	F4	-	-	16	[2]	N; PU	AI	ADC1_0 — ADC1 and ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							-	R — Function reserved.
							I/O	USB1_ULPI_D4 — ULPI link bidirectional data line 4.
							-	R — Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	GPIO6[3] — General purpose digital input/output pin.
							-	R — Function reserved.
							I	T3_CAP1 — Capture input 1 of timer 3.
PC_5	G4	-	-	20	[2]	N; PU	I/O	SD_DAT0 — SD/MMC data bus line 0.
							-	R — Function reserved.
							I/O	USB1_ULPI_D3 — ULPI link bidirectional data line 3.
							-	R — Function reserved.
							O	ENET_TX_ER — Ethernet Transmit Error (MII interface).
							I/O	GPIO6[4] — General purpose digital input/output pin.
							-	R — Function reserved.
							I	T3_CAP2 — Capture input 2 of timer 3.
PC_6	H6	-	-	22	[2]	N; PU	I/O	SD_DAT1 — SD/MMC data bus line 1.
							-	R — Function reserved.
							I/O	USB1_ULPI_D2 — ULPI link bidirectional data line 2.
							-	R — Function reserved.
							I	ENET_RXD2 — Ethernet receive data 2 (MII interface).
							I/O	GPIO6[5] — General purpose digital input/output pin.
							-	R — Function reserved.
							I	T3_CAP3 — Capture input 3 of timer 3.
PC_6	H6	-	-	22	[2]	N; PU	I/O	SD_DAT2 — SD/MMC data bus line 2.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PD_12	N11	-	-	94	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							O	EMC_CS2 — LOW active Chip Select 2 signal.
							-	R — Function reserved.
							I/O	GPIO6[26] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	CTOUT_10 — SCTimer/PWM output 10. Match output 3 of timer 3.
PD_13	T14	-	-	97	[2]	N; PU	-	R — Function reserved.
							I	CTIN_0 — SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							O	EMC_BLS2 — LOW active Byte Lane select signal 2.
							-	R — Function reserved.
							I/O	GPIO6[27] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	CTOUT_13 — SCTimer/PWM output 13. Match output 3 of timer 3.
PD_14	R13	-	-	99	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							O	EMC_DYCS2 — SDRAM chip select 2.
							-	R — Function reserved.
							I/O	GPIO6[28] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	CTOUT_11 — SCTimer/PWM output 11. Match output 3 of timer 2.
PD_15	T15	-	-	101	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							I/O	EMC_A17 — External memory address line 17.
							-	R — Function reserved.
							I/O	GPIO6[29] — General purpose digital input/output pin.
							I	SD_WP — SD/MMC card write protect input.
							O	CTOUT_8 — SCTimer/PWM output 8. Match output 0 of timer 2.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PE_7	F15	-	-	149	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_5 — SCTimer/PWM output 5. Match output 3 of timer 3.
							I	U1_CTS — Clear to Send input for UART1.
							I/O	EMC_D26 — External memory data line 26.
							I/O	GPIO7[7] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_8	F14	-	-	150	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_4 — SCTimer/PWM output 4. Match output 3 of timer 3.
							I	U1_DSR — Data Set Ready input for UART1.
							I/O	EMC_D27 — External memory data line 27.
							I/O	GPIO7[8] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_9	E16	-	-	152	[2]	N; PU	-	R — Function reserved.
							I	CTIN_4 — SCTimer/PWM input 4. Capture input 2 of timer 1.
							I	U1_DCD — Data Carrier Detect input for UART1.
							I/O	EMC_D28 — External memory data line 28.
							I/O	GPIO7[9] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_10	E14	-	-	154	[2]	N; PU	-	R — Function reserved.
							I	CTIN_3 — SCTimer/PWM input 3. Capture input 1 of timer 1.
							O	U1_DTR — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	EMC_D29 — External memory data line 29.
							I/O	GPIO7[10] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
Debug pins								
DBGEN	L4	A6	28	41	[2]	I	I	JTAG interface control signal. Also used for boundary scan. To use the part in functional mode, connect this pin in one of the following ways: • Leave DBGEN open. The DBGEN pin is pulled up internally by a 50 kΩ resistor. • Tie DBGEN to VDDIO. • Pull DBGEN up to VDDIO with an external pull-up resistor.
TCK/SWDCLK	J5	H2	27	38	[2]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
TRST	M4	B4	29	42	[2]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	C4	30	44	[2]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	H3	31	46	[2]	O	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	G3	26	35	[2]	I; PU	I	Test Data In for JTAG interface.
USB0 pins								
USB0_DP	F2	E1	18	26	[6]	-	I/O	USB0 bidirectional D+ line. Do not add an external series resistor.
USB0_DM	G2	E2	20	28	[6]	-	I/O	USB0 bidirectional D- line. Do not add an external series resistor.
USB0_VBUS	F1	E3	21	29	[6] [7]	-	I	VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 70 kΩ (typical) ± 30 kΩ.
USB0_ID	H2	F1	22	30	[8]	-	I	Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For use with OTG, this pin has an internal pull-up resistor.
USB0_RREF	H1	F3	24	32	[8]	-		12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference.
USB1 pins								
USB1_DP	F12	E9	89	129	[9]	-	I/O	USB1 bidirectional D+ line. Add an external series resistor of 33 Ω +/- 2 %.
USB1_DM	G12	E10	90	130	[9]	-	I/O	USB1 bidirectional D- line. Add an external series resistor of 33 Ω +/- 2 %.
I²C-bus pins								
I2C0_SCL	L15	D6	92	132	[10]	I; F	I/O	I ² C clock input/output. Open-drain output (for I ² C-bus compliance).
I2C0_SDA	L16	E6	93	133	[10]	I; F	I/O	I ² C data input/output. Open-drain output (for I ² C-bus compliance).
Reset and wake-up pins								
RESET	D9	B6	128	185	[11]	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin does not have an internal pull-up.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

7.18 Analog peripherals

7.18.1 Analog-to-Digital Converter

Remark: The LPC185x/3x/2x/1x contain two 10-bit ADCs. All input channels are shared between ADC0 and ADC1.

7.18.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.18.2 Digital-to-Analog Converter (DAC)

7.18.2.1 Features

- 10-bit resolution.
- Monotonic by design (resistor string architecture).
- Controllable conversion speed.
- Low power consumption.

7.19 Peripherals in the RTC power domain

7.19.1 RTC

The Real-Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.19.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.

- Timer/USART inputs
- Enabling the USB controllers

In addition, the CREG block contains the part identification and part configuration information.

7.20.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled. For pins that support a digital and analog function, the ADC function select registers in the SCU enable the analog function.

A separate set of analog I/Os for the ADCs and the DAC as well as most USB pins are located on separate pads and are not controlled through the SCU.

In addition, the clock delay register for the SDRAM EMC_CLK pins and the registers that select the pin interrupts are located in the SCU.

7.20.3 Clock Generation Unit (CGU)

The Clock Generator Unit (CGU) generates several base clocks. The base clocks can be unrelated in frequency and phase and can have different clock sources within the CGU. One CGU base clock is routed to the CLKOUT pins. The base clock that generates the CPU clock is referred to as CCLK.

Multiple branch clocks are derived from each base clock. The branch clocks offer flexible control for power-management purposes. All branch clocks are outputs of one of two Clock Control Units (CCUs) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase.

7.20.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy for $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ and 3% accuracy for $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $0\text{ }^{\circ}\text{C}$ and $T_{amb} = 85\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$.

Upon power-up or any chip reset, the LPC185x/3x/2x/1x use the IRC as the clock source. The boot loader then configures the PLL1 to provide a 96 MHz clock for the core and the PLL0USB or PLL0AUDIO as needed if an external boot source is selected.

7.20.5 PLL0USB (for USB0)

PLL0 is a dedicated PLL for the USB0 High-speed controller.

PLL0 accepts an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

7.20.6 PLL0AUDIO (for audio)

The audio PLL PLL0AUDIO is a general-purpose PLL with a small step size. This PLL accepts an input clock frequency derived from an external oscillator or internal IRC. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). A sigma-delta converter modulates the PLL divider ratios to obtain the desired

output frequency. The output frequency can be set as a multiple of the sampling frequency f_s to $32 \times f_s$, $64 \times f_s$, $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, $512 \times f_s$ and the sampling frequency f_s can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96, 192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

7.20.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

7.20.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals.

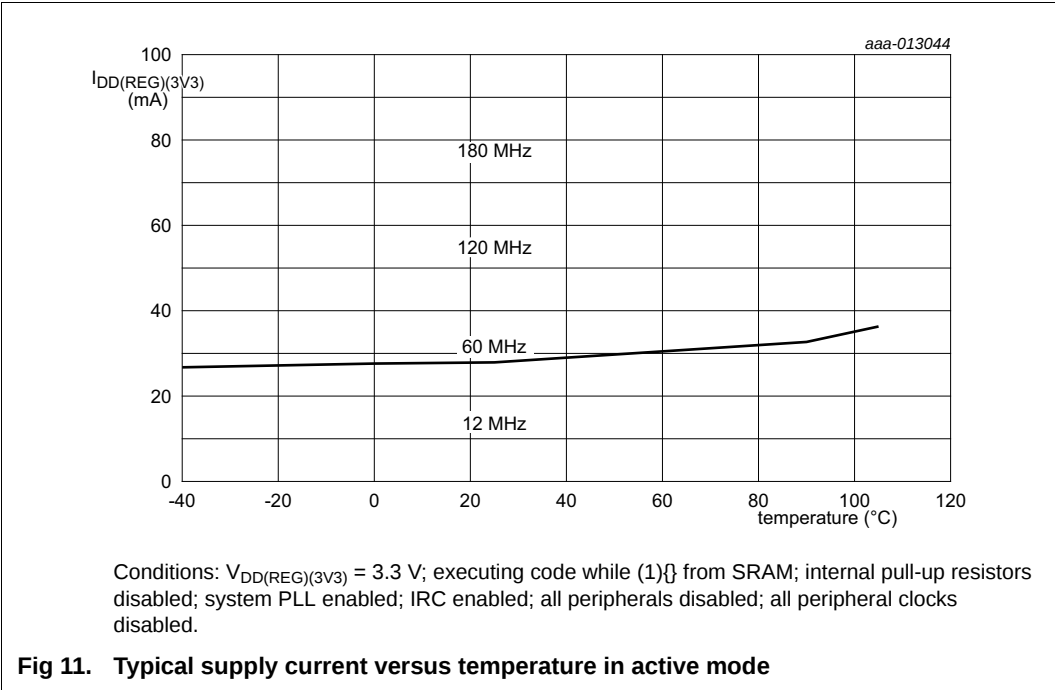
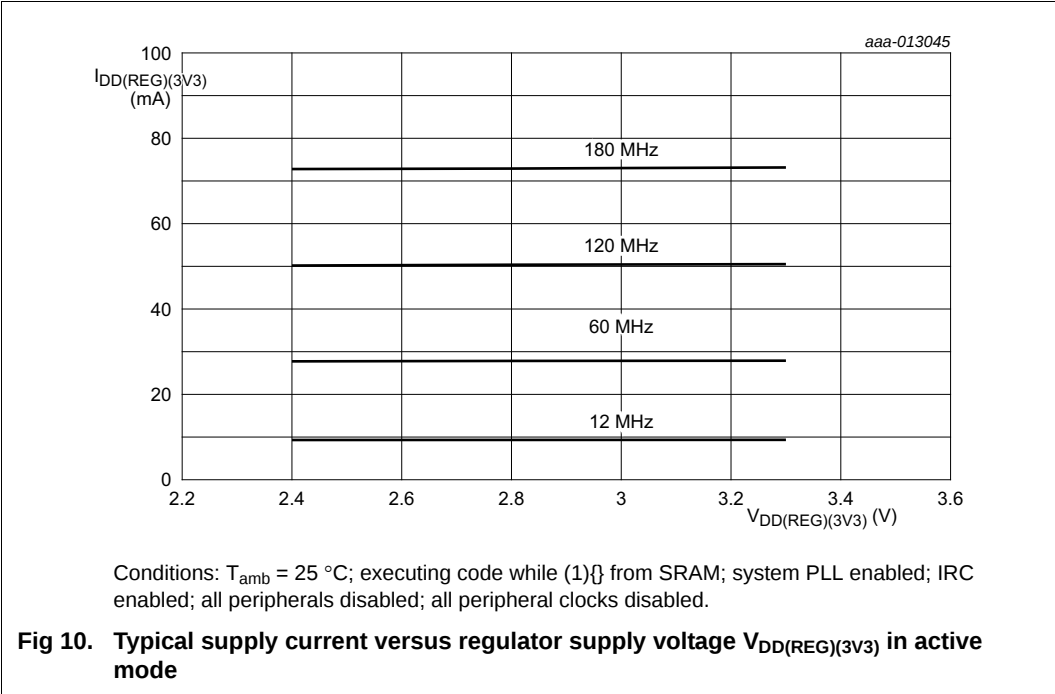
7.20.9 Power control

The LPC185x/3x/2x/1x feature several independent power domains to control power to the core and the peripherals (see [Figure 9](#)). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

Table 11. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
I/O pins - high drive strength: ultra-high drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(I/O)}$; on-chip pull-down resistor disabled		-	3	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	0.6	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 105\text{ }^{\circ}\text{C}$		-	63	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(I/O)} - 0.4\text{ V}$		-20	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(I/O)}$	[10]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	$V_I = 0\text{ V}$; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(I/O)}$; on-chip pull-down resistor disabled		-	3	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	0.5	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 105\text{ }^{\circ}\text{C}$		-	40	-	nA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$ to $V_{DD(I/O)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(I/O)} \geq 2.4\text{ V}$		0	-	5.5	V
		$V_{DD(I/O)} = 0\text{ V}$		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(I/O)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(I/O)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(I/O)}$	-	-	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -8\text{ mA}$		$V_{DD(I/O)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 8\text{ mA}$		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(I/O)} - 0.4\text{ V}$		-8	-	-	mA

10.1 Power consumption



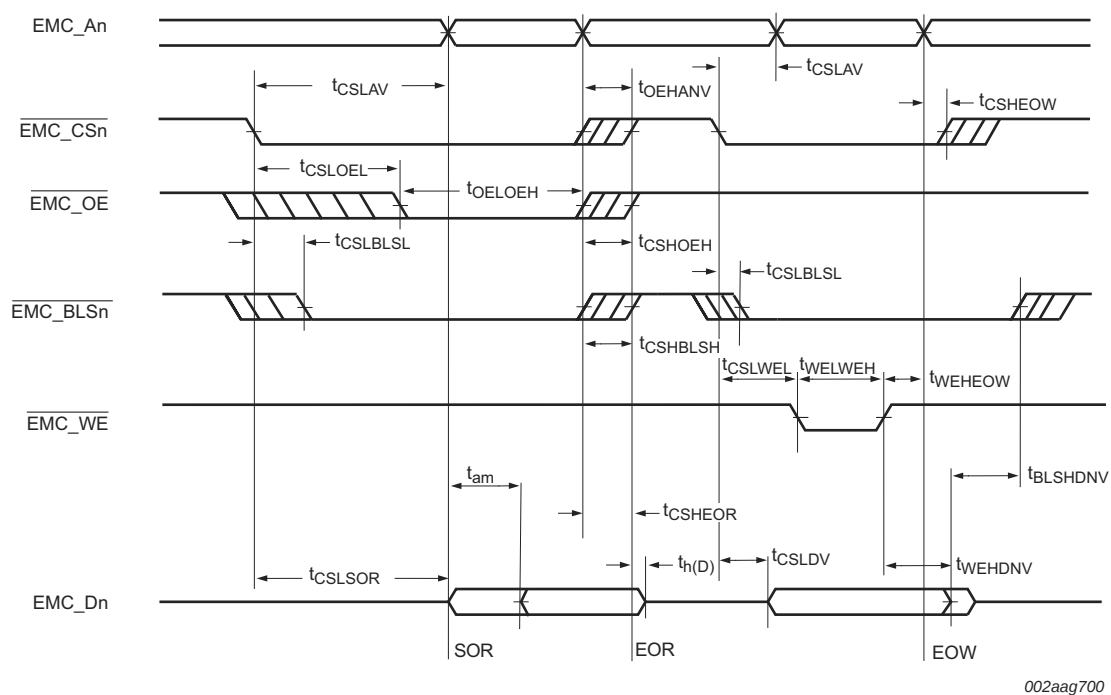
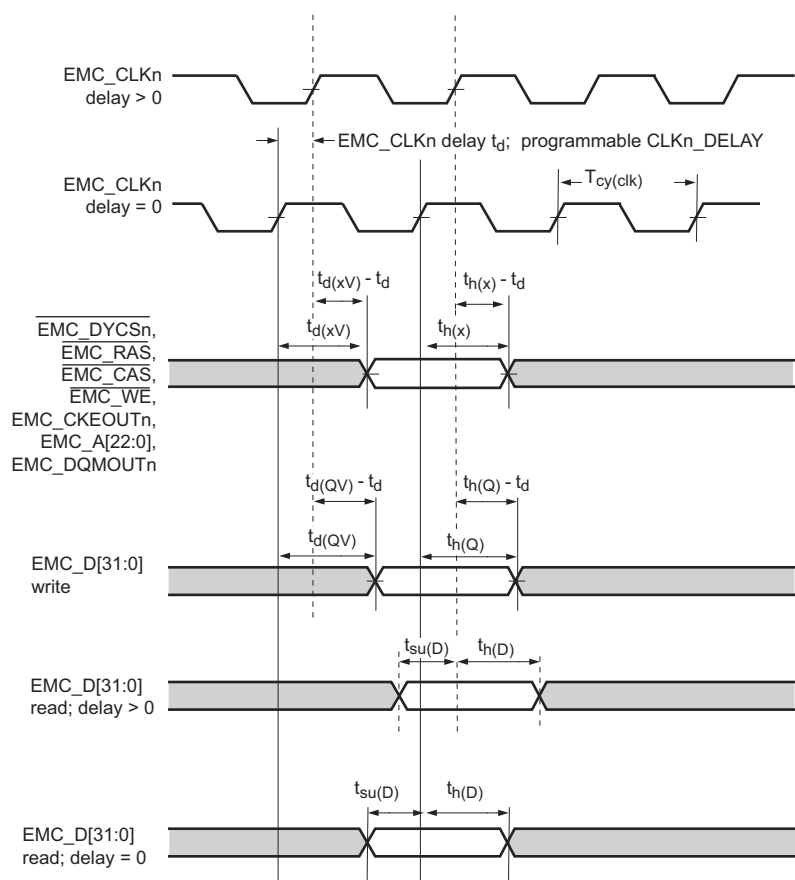


Fig 33. External static memory read/write access (PB = 1)



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For the programmable $EMC_CLK[3:0]$ clock delays $CLKn_DELAY$, see [Table 30](#).

Remark: For SDRAM operation, set $CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY$ in the $EMCDELAYCLK$ register.

Fig 34. SDRAM timing

Table 32. Static characteristics: USB0 PHY pins^[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P _{cons}	power consumption		[2]	-	68	-	mW
I _{DDA(3V3)}	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I _{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P _{cons}	power consumption		[2]	-	15	-	mW
I _{DDA(3V3)}	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I _{DDD}	digital supply current			-	3	-	mA
Suspend mode							
I _{DDA(3V3)}	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I _{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V _{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V _{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

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