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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1817jbd144e

4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	Motor control PWM	QEI	ADC channels	Temperature range ^[1]	GPIO
LPC1857FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1857JET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1857JBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1853FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1853JET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1853JBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1837FET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1837JET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1837JBD144	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1837JET100	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1833FET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1833JET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1833JBD144	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1833JET100	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1827JBD144	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1827JET100	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1825JBD144	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1825JET100	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1823JBD144	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1823JET100	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1822JBD144	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1822JET100	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1817JBD144	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1817JET100	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1815JBD144	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1815JET100	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1813JBD144	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1813JET100	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	no	no	4	J	49
LPC1812JBD144	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1812JET100	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	no	no	4	J	49

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

5. Block diagram

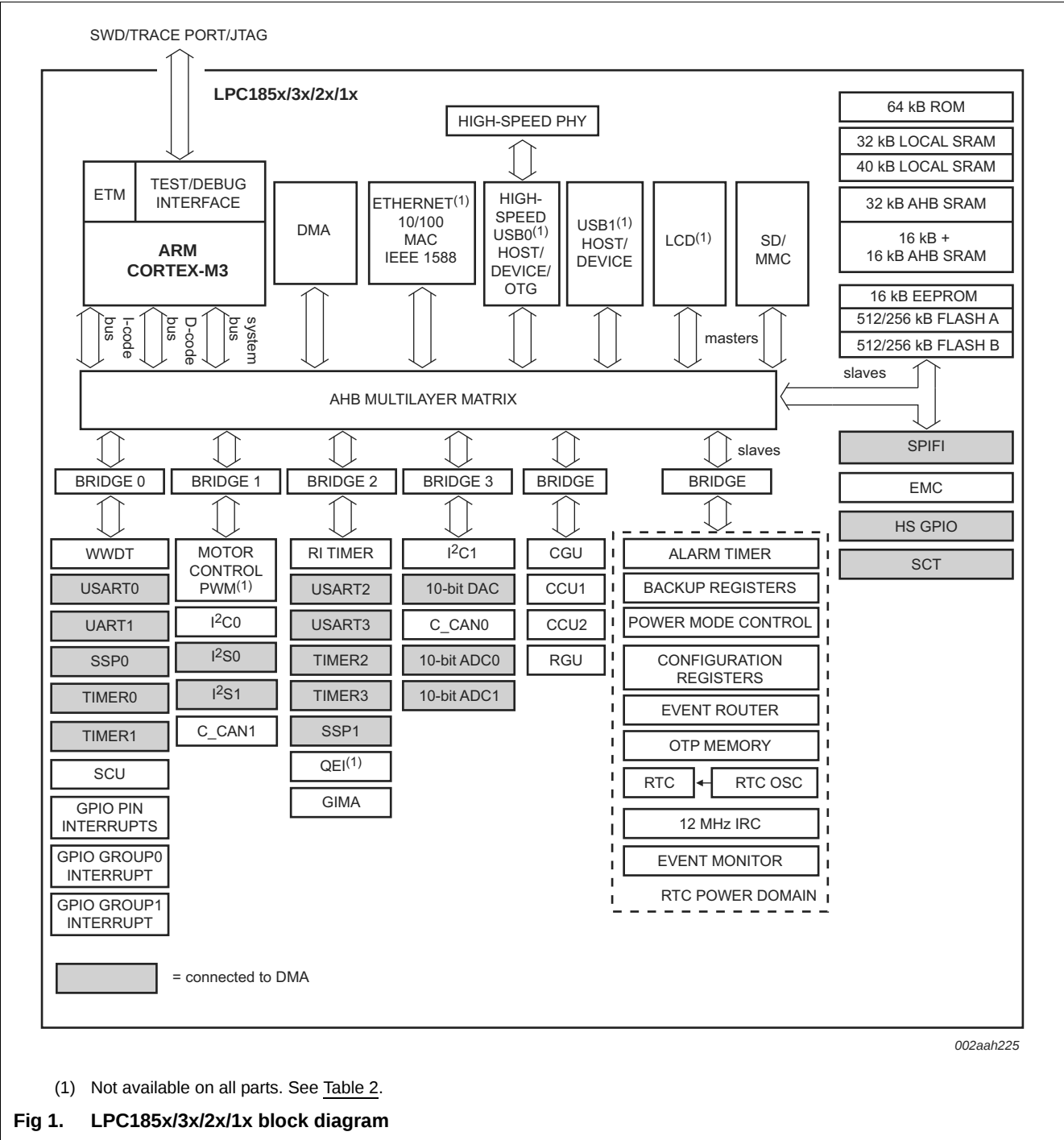


Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_8	R7	H5	51	71	[2]	N; PU	I/O	GPIO1[1] — General purpose digital input/output pin.
							O	U1_DTR — Data Terminal Ready output for UART1.
							O	CTOUT_12 — SCTimer/PWM output 12. Match output 3 of timer 3.
							I/O	EMC_D1 — External memory data line 1.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							O	SD_VOLT0 — SD/MMC bus voltage select output 0.
P1_9	T7	J5	52	73	[2]	N; PU	I/O	GPIO1[2] — General purpose digital input/output pin.
							O	U1_RTS — Request to Send output for UART1.
							O	CTOUT_11 — SCTimer/PWM output 11. Match output 3 of timer 2.
							I/O	EMC_D2 — External memory data line 2.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	SD_DAT0 — SD/MMC data bus line 0.
P1_10	R8	H6	53	75	[2]	N; PU	I/O	GPIO1[3] — General purpose digital input/output pin.
							I	U1_RI — Ring Indicator input for UART1.
							O	CTOUT_14 — SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	EMC_D3 — External memory data line 3.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	SD_DAT1 — SD/MMC data bus line 1.
P1_11	T9	J7	55	77	[2]	N; PU	I/O	GPIO1[4] — General purpose digital input/output pin.
							I	U1_CTS — Clear to Send input for UART1.
							O	CTOUT_15 — SCTimer/PWM output 15. Match output 3 of timer 3.
							I/O	EMC_D4 — External memory data line 4.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	SD_DAT2 — SD/MMC data bus line 2.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_12	R9	K7	56	78	[2]	N; PU	I/O	GPIO1[5] — General purpose digital input/output pin.
							I	U1_DCD — Data Carrier Detect input for UART1.
							-	R — Function reserved.
							I/O	EMC_D5 — External memory data line 5.
							I	T0_CAP1 — Capture input 1 of timer 0.
							-	R — Function reserved.
							-	R — Function reserved.
P1_13	R10	H8	60	83	[2]	N; PU	I/O	GPIO1[6] — General purpose digital input/output pin.
							O	U1_TXD — Transmitter output for UART1.
							-	R — Function reserved.
							I/O	EMC_D6 — External memory data line 6.
							I	T0_CAP0 — Capture input 0 of timer 0.
							-	R — Function reserved.
							-	R — Function reserved.
P1_14	R11	J8	61	85	[2]	N; PU	I/O	GPIO1[7] — General purpose digital input/output pin.
							I	U1_RXD — Receiver input for UART1.
							-	R — Function reserved.
							I/O	EMC_D7 — External memory data line 7.
							O	T0_MAT2 — Match output 2 of timer 0.
							-	R — Function reserved.
							-	R — Function reserved.
P1_15	T12	K8	62	87	[2]	N; PU	I/O	GPIO0[2] — General purpose digital input/output pin.
							O	U2_TXD — Transmitter output for USART2.
							-	R — Function reserved.
							I	ENET_RXD0 — Ethernet receive data 0 (RMII/MII interface).
							O	T0_MAT1 — Match output 1 of timer 0.
							-	R — Function reserved.
							I/O	EMC_D8 — External memory data line 8.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_2	M15	F5	84	121	[2]	N; PU	-	R — Function reserved.
							I/O	U0_UCLK — Serial clock input/output for USART0 in synchronous mode.
							I/O	EMC_A11 — External memory address line 11.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							I/O	GPIO5[2] — General purpose digital input/output pin.
							I	CTIN_6 — SCTimer/PWM input 6. Capture input 1 of timer 3.
							I	T3_CAP2 — Capture input 2 of timer 3.
							O	EMC_CS1 — LOW active Chip Select 1 signal.
P2_3	J12	D8	87	127	[3]	N; PU	-	R — Function reserved.
							I/O	I2C1_SDA — I ² C1 data input/output (this pin does not use a specialized I ² C pad).
							O	U3_TXD — Transmitter output for USART3. See Table 4 for ISP mode.
							I	CTIN_1 — SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	GPIO5[3] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT0 — Match output 0 of timer 3.
P2_4	K11	D9	88	128	[3]	N; PU	-	R — Function reserved.
							I/O	I2C1_SCL — I ² C1 clock input/output (this pin does not use a specialized I ² C pad).
							I	U3_RXD — Receiver input for USART3. See Table 4 for ISP mode.
							I	CTIN_0 — SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	GPIO5[4] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT1 — Match output 1 of timer 3.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P8_0	E5	-	-	2	[3]	N; PU	I/O	GPIO4[0] — General purpose digital input/output pin.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	R — Function reserved.
							I	MCI2 — Motor control PWM channel 2, input.
							-	R — Function reserved.
							-	R — Function reserved.
							O	T0_MAT0 — Match output 0 of timer 0.
P8_1	H5	-	-	34	[3]	N; PU	I/O	GPIO4[1] — General purpose digital input/output pin.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							-	R — Function reserved.
							I	MCI1 — Motor control PWM channel 1, input.
							-	R — Function reserved.
							-	R — Function reserved.
							O	T0_MAT1 — Match output 1 of timer 0.
P8_2	K4	-	-	36	[3]	N; PU	I/O	GPIO4[2] — General purpose digital input/output pin.
							O	USB0_IND0 — USB0 port indicator LED control output 0.
							-	R — Function reserved.
							I	MCI0 — Motor control PWM channel 0, input.
							-	R — Function reserved.
							-	R — Function reserved.
							O	T0_MAT2 — Match output 2 of timer 0.
P8_3	J3	-	-	37	[2]	N; PU	I/O	GPIO4[3] — General purpose digital input/output pin.
							I/O	USB1_ULPI_D2 — ULPI link bidirectional data line 2.
							-	R — Function reserved.
							O	LCD_VD12 — LCD data.
							O	LCD_VD19 — LCD data.
							-	R — Function reserved.
							O	T0_MAT3 — Match output 3 of timer 0.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PB_3	A13	-	-	178	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D6 — ULPI link bidirectional data line 6.
							O	LCD_VD20 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[23] — General purpose digital input/output pin.
							O	CTOUT_8 — SCTimer/PWM output 8. Match output 0 of timer 2.
							-	R — Function reserved.
PB_4	B11	-	-	180	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D5 — ULPI link bidirectional data line 5.
							O	LCD_VD15 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[24] — General purpose digital input/output pin.
							I	CTIN_5 — SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	R — Function reserved.
PB_5	A12	-	-	181	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D4 — ULPI link bidirectional data line 4.
							O	LCD_VD14 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[25] — General purpose digital input/output pin.
							I	CTIN_7 — SCTimer/PWM input 7.
							O	LCD_PWR — LCD panel power enable.
PB_6	A6	-	-	-	[5]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D3 — ULPI link bidirectional data line 3.
							O	LCD_VD13 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[26] — General purpose digital input/output pin.
							I	CTIN_6 — SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	LCD_VD19 — LCD data.
							-	R — Function reserved.
							AI	ADC0_6 and ADC1 — ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PE_11	D16	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_12 — SCTimer/PWM output 12. Match output 3 of timer 3.
							O	U1_TXD — Transmitter output for UART1.
							I/O	EMC_D30 — External memory data line 30.
							I/O	GPIO7[11] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_11 — SCTimer/PWM output 11. Match output 3 of timer 2.
							I	U1_RXD — Receiver input for UART1.
							I/O	EMC_D31 — External memory data line 31.
							I/O	GPIO7[12] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_14 — SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	I2C1_SDA — I ² C1 data input/output (this pin does not use a specialized I ² C pad).
							O	EMC_DQMOUT3 — Data mask 3 used with SDRAM and static devices.
							I/O	GPIO7[13] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_14	C15	-	-	-	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							O	EMC_DYCS3 — SDRAM chip select 3.
							I/O	GPIO7[14] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.

- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.6 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts.
- C_CAN0/1 and QEI interrupts.
- Ethernet, USB0, USB1 signals.
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3).

Remark: Any interrupt can wake up the ARM Cortex-M3 from sleep mode if enabled in the NVIC.

7.7 Global Input Multiplexer Array (GIMA)

The GIMA routes signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.

7.7.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.8 On-chip static RAM

The LPC185x/3x/2x/1x support up to 136 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI) ^[1] .
USART3	1	0	0	1	Enter ISP mode using USART3 functions on pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.

Remark: Pin functions for SPIFI and SSP0 boot are different.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Enter ISP mode using USART0 pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8 ^[1] .
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI) ^[1] .
USART3	HIGH	LOW	LOW	LOW	Enter ISP mode using USART3 pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.

Remark: Pin functions for SPIFI and SSP0 boot are different.

7.13 One-Time Programmable (OTP) memory

The OTP provides 64 bit+ 256 bit of memory for general-purpose use.

7.14 General-Purpose I/O (GPIO)

The LPC185x/3x/2x/1x provides 8 GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.14.1 Features

- Accelerated GPIO functions:
 - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
 - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
 - All GPIO registers are byte and half-word addressable.
 - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Two GPIO group interrupts can be triggered by any pin or pins in each port.

7.15 AHB peripherals

7.15.1 State Configurable Timer/PWM (SCTimer/PWM) subsystem

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DD(REG)(3V3)}	regulator supply voltage (3.3 V)	on pin VDDREG		−0.5	3.6	V
V _{DD(IO)}	input/output supply voltage	on pin VDDIO		−0.5	3.6	V
V _{DDA(3V3)}	analog supply voltage (3.3 V)	on pin VDDA		−0.5	3.6	V
V _{BAT}	battery supply voltage	on pin VBAT		−0.5	3.6	V
V _{prog(pf)}	polyfuse programming voltage	on pin VPP		−0.5	3.6	V
V _I	input voltage	when V _{DD(IO)} ≥ 2.4 V	[2]	−0.5	5.5	V
		5 V tolerant digital I/O pins				
		ADC/DAC pins and digital I/O pins configured for an analog function		−0.5	V _{DDA(3V3)}	V
		USB0 pins USB0_DP; USB0_DM; USB0_VBUS		−0.3	5.2	V
		USB0 pins USB0_ID; USB0_RREF		−0.3	3.6	V
		USB1 pins USB1_DP and USB1_DM		−0.3	5.2	V
I _{DD}	supply current	per supply pin	[3]	-	100	mA
I _{SS}	ground current	per ground pin	[3]	-	100	mA
I _{latch}	I/O latch-up current	−(0.5V _{DD(IO)}) < V _I < (1.5V _{DD(IO)}); T _j < 125 °C		-	100	mA
T _{stg}	storage temperature		[4]	−65	+150	°C
P _{tot(pack)}	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V _{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	−	2000	V

[1] The following applies to the limiting values:

- This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

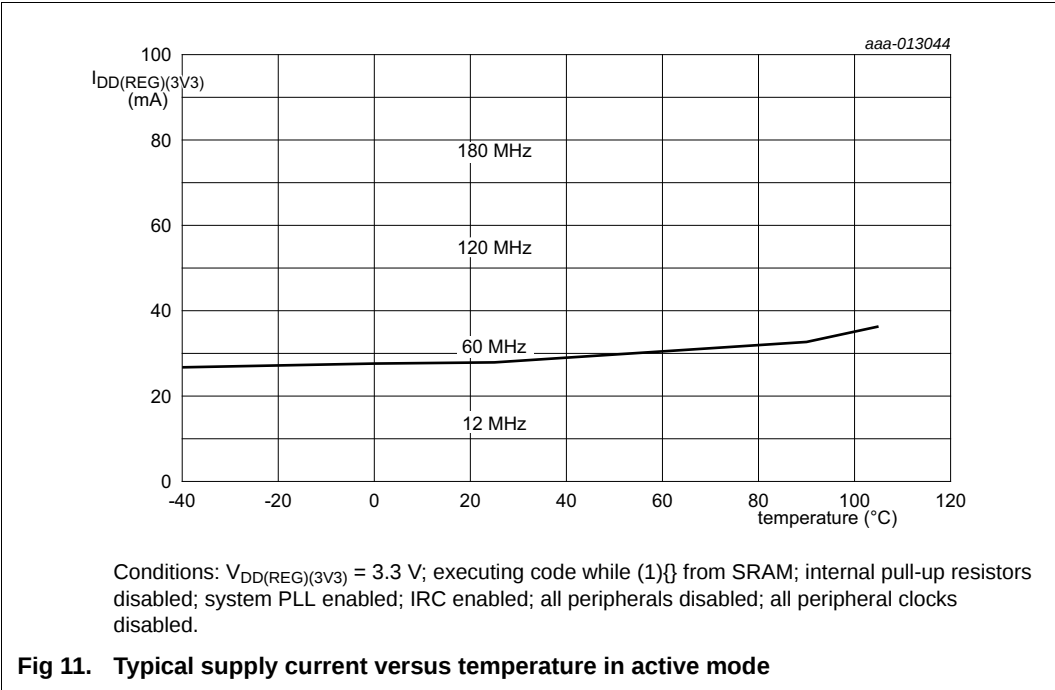
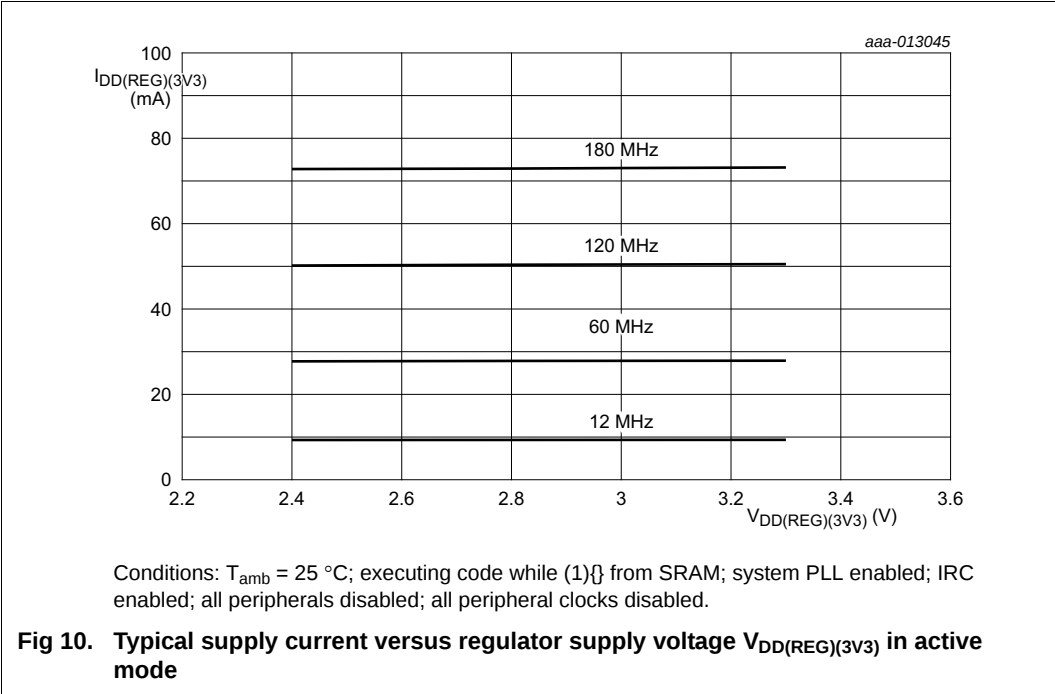
[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

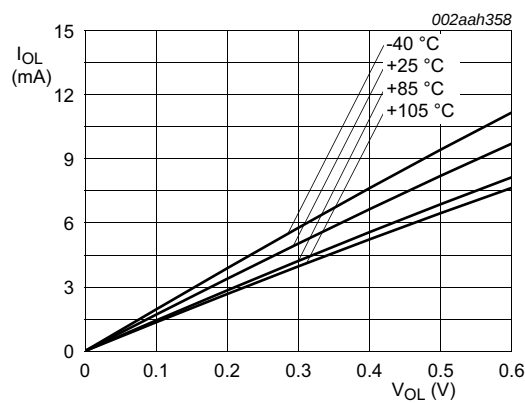
Table 11. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
I/O pins - high drive strength: ultra-high drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(I/O)}$; on-chip pull-down resistor disabled		-	3	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	0.6	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 105\text{ }^{\circ}\text{C}$		-	63	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(I/O)} - 0.4\text{ V}$		-20	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(I/O)}$	[10]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	$V_I = 0\text{ V}$; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(I/O)}$; on-chip pull-down resistor disabled		-	3	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	0.5	-	nA
		$V_I = 5\text{ V}$; $T_{amb} = 105\text{ }^{\circ}\text{C}$		-	40	-	nA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$ to $V_{DD(I/O)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(I/O)} \geq 2.4\text{ V}$		0	-	5.5	V
		$V_{DD(I/O)} = 0\text{ V}$		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(I/O)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(I/O)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(I/O)}$	-	-	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -8\text{ mA}$		$V_{DD(I/O)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 8\text{ mA}$		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(I/O)} - 0.4\text{ V}$		-8	-	-	mA

10.1 Power consumption

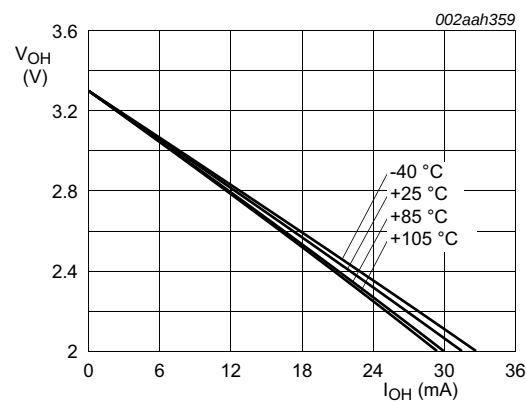


10.3 Electrical pin characteristics



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 19. Standard I/O pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 20. Standard I/O pins; typical HIGH level output voltage V_{OH} versus HIGH level output current I_{OH}

11.4 Crystal oscillator

Table 19. Dynamic characteristic: oscillator

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; $V_{DD(10)}$ over specified ranges; $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$ [1]

Symbol	Parameter	Conditions		Min	Typ ^[2]	Max	Unit
Low-frequency mode (1-20 MHz) ^[5]							
t _{jit(per)}	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 - 25 MHz) ^[6]							
t _{jit(per)}	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.5 IRC oscillator

Table 20. Dynamic characteristic: IRC oscillator

$2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	$-40\text{ }^{\circ}\text{C} \leq T_{amb} < 0\text{ }^{\circ}\text{C}$	12.0 - 3 %	12.0	12.0 + 3 %	MHz
		$0\text{ }^{\circ}\text{C} \leq T_{amb} \leq 85\text{ }^{\circ}\text{C}$	12.0 - 1.5 %	12.0	12.0 + 1.5 %	MHz
		$85\text{ }^{\circ}\text{C} < T_{amb} \leq 105\text{ }^{\circ}\text{C}$	12.0 - 3 %	12.0	12.0 + 3 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 RTC oscillator

See [Section 13.3](#) for connecting the RTC oscillator to an external clock source.

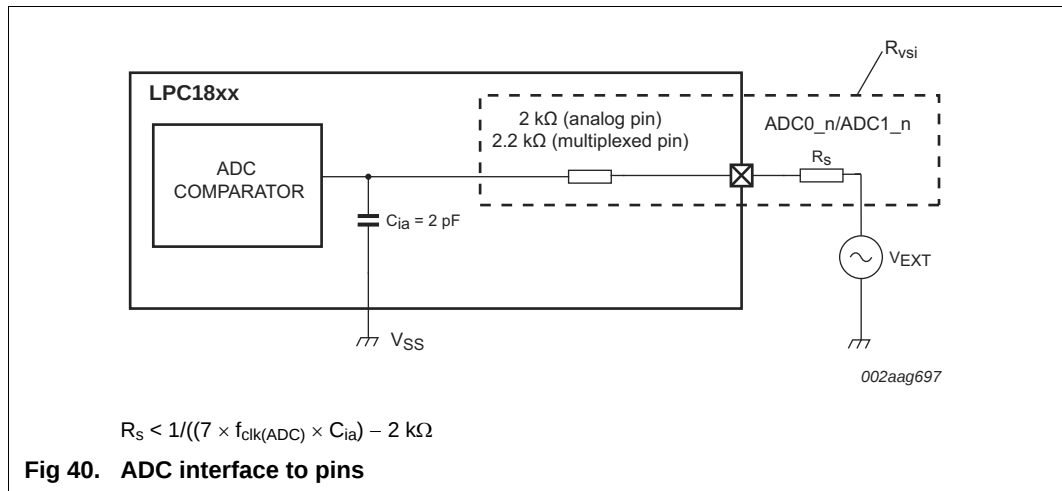
Table 21. Dynamic characteristic: RTC oscillator

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$ or $2.4\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$ [1]

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz
$I_{CC(osc)}$	oscillator supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

**Table 38. DAC characteristics**

$V_{DDA(3V3)}$ over specified ranges; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	$2.7 \text{ V} \leq V_{DDA(3V3)} \leq 3.6 \text{ V}$	[1]	-	± 0.8	-	LSB
		$2.4 \text{ V} \leq V_{DDA(3V3)} < 2.7 \text{ V}$		-	± 1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975	[1]	-	± 1.0	-	LSB
		$2.7 \text{ V} \leq V_{DDA(3V3)} \leq 3.6 \text{ V}$		-	± 1.5	-	LSB
E_O	offset error	$2.7 \text{ V} \leq V_{DDA(3V3)} \leq 3.6 \text{ V}$	[1]	-	± 0.8	-	LSB
		$2.4 \text{ V} \leq V_{DDA(3V3)} < 2.7 \text{ V}$		-	± 1.0	-	LSB
E_G	gain error	$2.7 \text{ V} \leq V_{DDA(3V3)} \leq 3.6 \text{ V}$	[1]	-	± 0.3	-	%
		$2.4 \text{ V} \leq V_{DDA(3V3)} < 2.7 \text{ V}$		-	± 1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	k Ω
t_s	settling time		[2]		0.4		μs

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC18xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

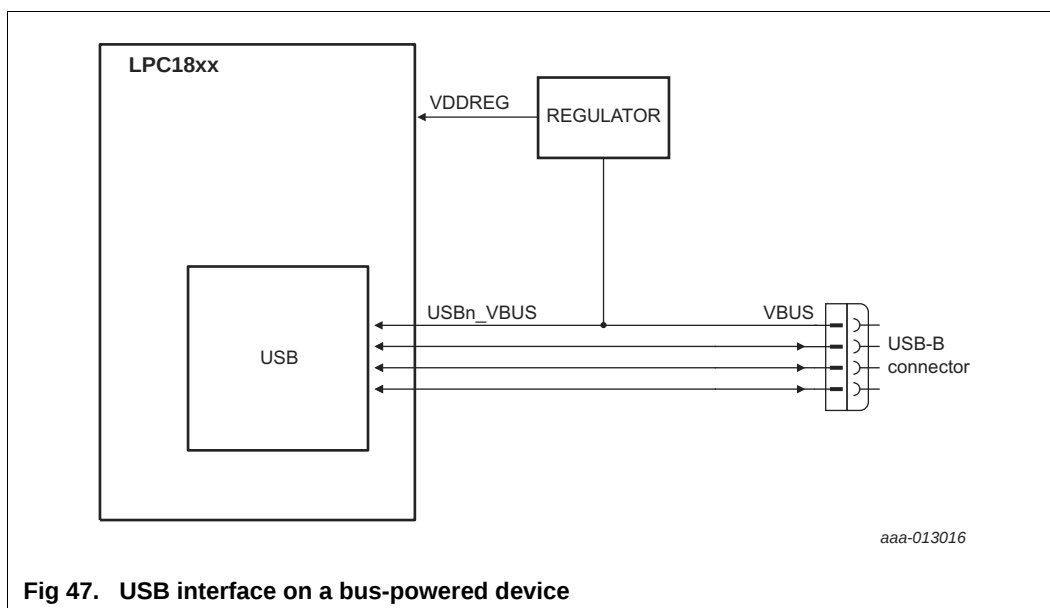


Fig 47. USB interface on a bus-powered device

Remark: If the VBUS function of the USB1 interface is not connected, configure the pin function for GPIO using the function control bits in the SYSCON block.

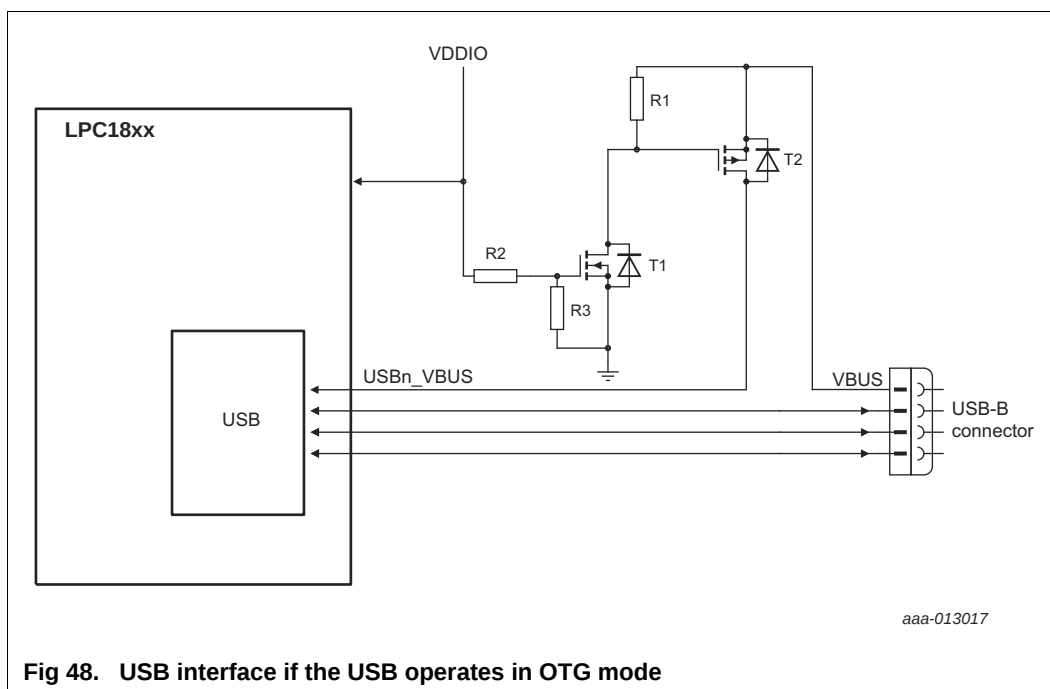


Fig 48. USB interface if the USB operates in OTG mode

Remark: In OTG mode, it is important to be able to detect the VBUS level and to charge and discharge VBUS. This requires adding active devices that disconnect the link when VDDIO is not present.

14. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm

SOT740-2

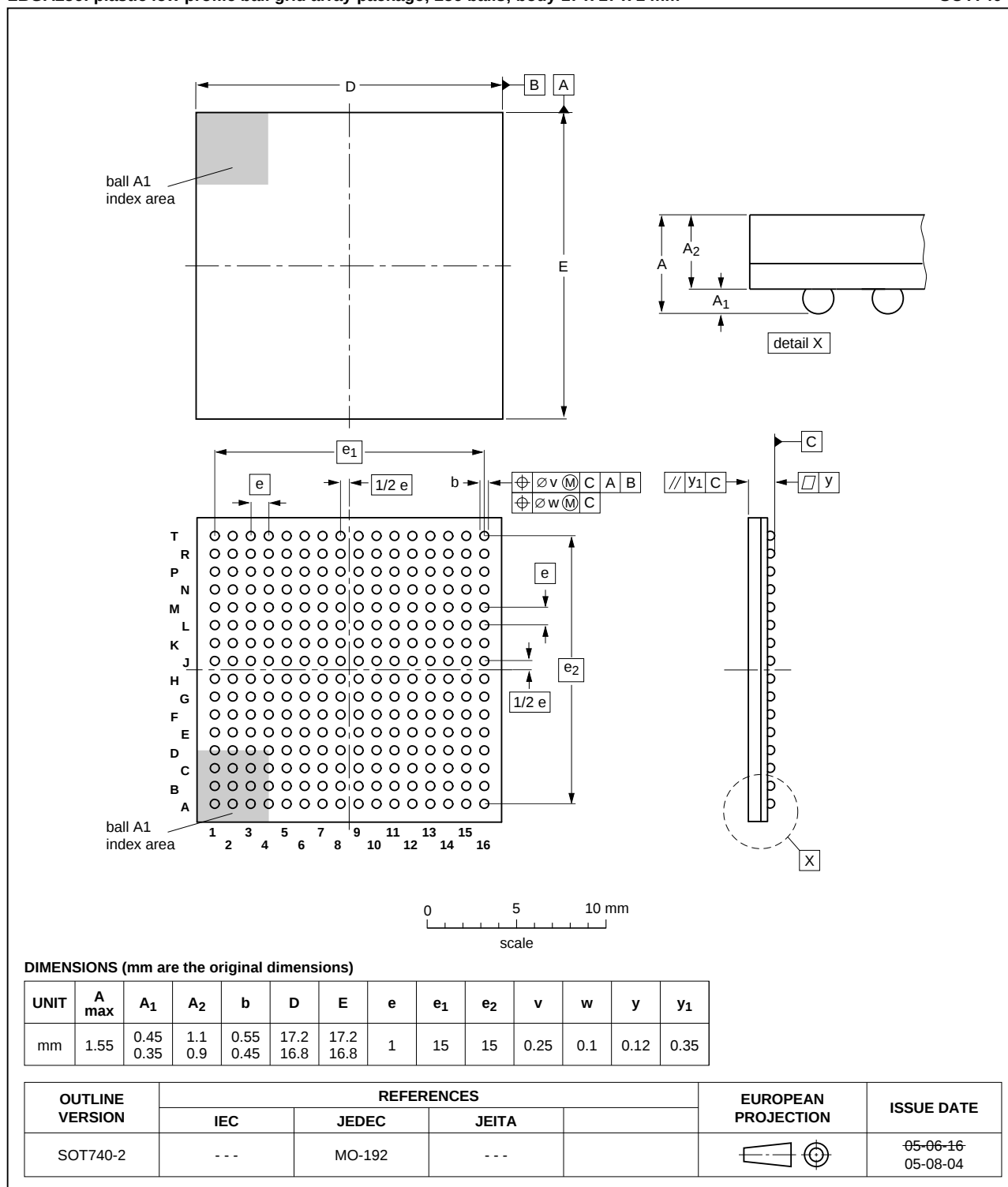


Fig 49. Package outline of the LPGA256 package

Table 45. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	- Parameter t_{ret} (retention time) for EEPROM updated in Table 15. - Parameter $V_{\text{DDA}(3\text{V3})}$ added for pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3 in Table 11. - Parameter name $I_{\text{DD(ADC)}}$ changed to I_{DDA} in Table 11. - Minimum wake-up time from sleep mode added in Table 16. - Data for $I_{\text{DD(IO)}}$ added in Table 11. - Data sheet status changed to Product data sheet. - IRC specifications corrected in Table 19 "Dynamic characteristic: IRC oscillator" and Section 2: Accuracy changed to +/- 3 % over the entire temperature range. - Bandgap characteristics removed. - Section 13.7 "Suggested USB interface solutions" added. $I_{\text{DD(REG)(3V3)}}$ updated in Table 11 "Static characteristics" for the following conditions: - Active mode: CCLK = 12 MHz; $I_{\text{DD(REG)(3V3)}}$ changed from 9.3 mA to 10 mA. - Active mode: CCLK = 60 MHz; $I_{\text{DD(REG)(3V3)}}$ changed from 26 mA to 28 mA. - Active mode: CCLK = 120 MHz; $I_{\text{DD(REG)(3V3)}}$ changed from 46 mA to 51 mA. - Active mode: CCLK = 180 MHz; $I_{\text{DD(REG)(3V3)}}$ changed from 66 mA to 74 mA. - Sleep mode: CCLK = 12 MHz; $I_{\text{DD(REG)(3V3)}}$ changed from 6.2 mA to 8.8 mA. - Figure 10 to Figure 13 updated. - General-purpose OTP size corrected.			
LPC185X_3X_2X_1X v.4	20121031	Preliminary data sheet	-	LPC1857_53 v.3.2
Modifications:	- Removed TFBGA180 package. - Parts LPC183x, LPC182x, and LPC181x added. - LQFP144 and TFBGA100 packages added. - T = 105 °C data added in Figure 19 to Figure 22. - Changed symbol names and parameter names in Table 21. - Parameter I_{LH} updated for condition $V_{\text{I}} = 5 \text{ V}$ and $T_{\text{amb}} = 25 \text{ °C}/105 \text{ °C}$ in Table 11. - Power consumption data added in Section 10.1.			
Modifications:	- SPIFI dynamic characteristics added in Section 11.16. - IRC accuracy corrected to $\pm 2 \text{ %}$ for $T_{\text{amb}} = -40 \text{ °C}$ to 0 °C and $T_{\text{amb}} = 85 \text{ °C}$ to 105 °C. - Pull-up and Pull-down current data (Figure 23 and Figure 24) updated with data for $T_{\text{amb}} = 105 \text{ °C}$. - SCT dither engine added and SCT bi-directional event enable features added. See Section 7.15.1. - SPIFI maximum data rate changed to 52 MB per second. - Recommendation for V_{BAT} use added: The recommended operating condition for the battery supply is $V_{\text{DD(REG)(3V3)}} > V_{\text{BAT}} + 0.2 \text{ V}$. See Table 11, Table note 2. - Table 14 "Band gap characteristics" added. - Minimum value for parameter V_{IL} changed to 0 V in Table 11 "Static characteristics". - Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. - OTP memory size changed to 64 bit. - Use of C_CAN peripheral restricted in Section 2. - ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.			
LPC1857_53 v.3.2	20120920	Preliminary data sheet	-	LPC1857_53 v.3.1
Position of index sector in Figure 4 "Pin configuration LQFP208 package" corrected.				