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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	49
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1825jet100e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1857FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1857JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1857JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1853FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1853JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1853JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1837FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1837JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1837JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1837JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1833FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1833JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1833JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1833JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1827JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1827JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1825JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1825JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1823JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1823JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1822JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1822JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1817JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1817JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1815JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1815JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1813JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1813JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1812JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1812JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P5_7	R12	-	65	91	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
							O	**MCOA2 —** Motor control PWM channel 2, output A.
							I/O	**EMC_D11 —** External memory data line 11.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART1.
							O	**T1_MAT3 —** Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_0	M12	H7	73	105	[2]	N; PU	-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I^2S receive master clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_1	R15	G5	74	107	[2]	N; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_DYCS1}}$ —** SDRAM chip select 1.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							I	**T2_CAP0 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_2	L13	J9	78	111	[2]	N; PU	I/O	**GPIO3[1] —** General purpose digital input/output pin.
							O	**EMC_CKEOUT1 —** SDRAM clock enable 1.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**I2S0_RX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							I	**T2_CAP1 —** Capture input 1 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P6_3	P15	-	79	113	[2]	N; PU	I/O	**GPIO3[2] —** General purpose digital input/output pin.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	**R —** Function reserved.
							O	**EMC_CS1 —** LOW active Chip Select 1 signal.
							-	**R —** Function reserved.
							I	**T2_CAP2 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_4	R16	F6	80	114	[2]	N; PU	I/O	**GPIO3[3] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**U0_TXD —** Transmitter output for USART0.
							O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_5	P16	F9	82	117	[2]	N; PU	I/O	**GPIO3[4] —** General purpose digital input/output pin.
							O	**CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1.
							I	**U0_RXD —** Receiver input for USART0.
							O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_6	L14	-	83	119	[2]	N; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
							O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
							-	**R —** Function reserved.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**T2_CAP3 —** Capture input 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PA_0	L12	-	-	126	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_RX_MCLK —** I^2S1 receive master clock.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
PA_1	J14	-	-	134	[3]	N; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_2	K15	-	-	136	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_3	H11	-	-	147	[3]	N; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
							I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PC_0	D4	-	-	7	[5]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY.
							-	**R —** Function reserved.
							I/O	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface).
							O	**LCD_DCLK —** LCD panel clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							AI	**ADC1_1 —** ADC1 and ADC0, input channel 1. Configure the pin as input (USB_ULPI_CLK) and use the ADC function select register in the SCU to select the ADC.
PC_1	E4	-	-	9	[2]	N; PU	I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
							-	**R —** Function reserved.
							I	**U1_RI —** Ring Indicator input for UART1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							I/O	**GPIO6[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
PC_2	F6	-	-	13	[2]	N; PU	I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							I/O	**GPIO6[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PD_12	N11	-	-	94	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS2}}$ —** LOW active Chip Select 2 signal.
							-	**R —** Function reserved.
							I/O	**GPIO6[26] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
PD_13	T14	-	-	97	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_0 —** SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							O	**$\overline{\text{EMC\_BLS2}}$ —** LOW active Byte Lane select signal 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[27] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
PD_14	R13	-	-	99	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_DYCS2}}$ —** SDRAM chip select 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[28] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							-	**R —** Function reserved.
PD_15	T15	-	-	101	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A17 —** External memory address line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[29] —** General purpose digital input/output pin.
							I	**SD_WP —** SD/MMC card write protect input.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PF_9	D6	-	-	203	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**GPIO7[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	-	205	[5]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**SD_WP —** SD/MMC card write protect input.
							-	**R —** Function reserved.
							AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	-	207	[5]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[25] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							-	**R —** Function reserved.
							AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
Clock pins								

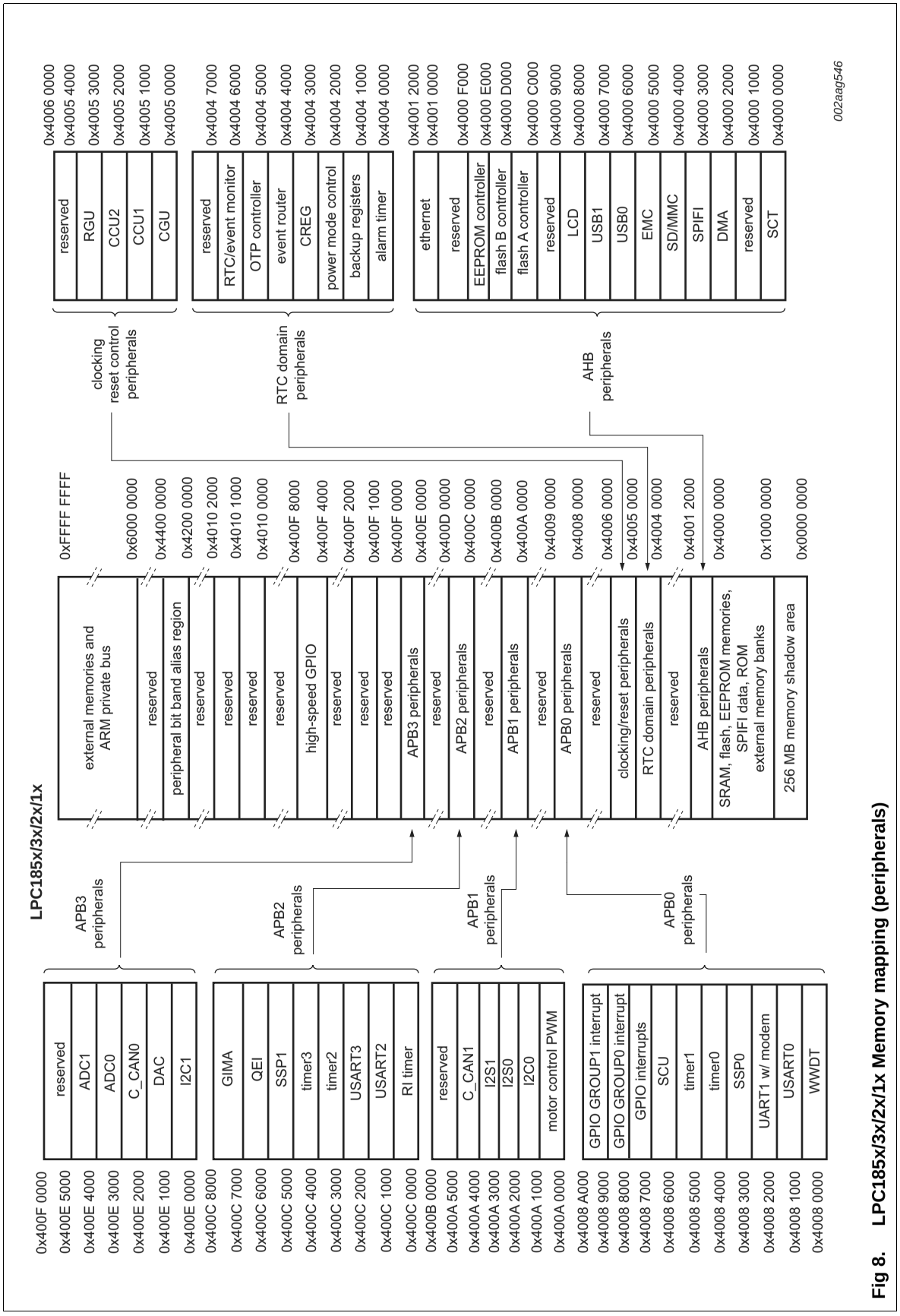


Fig 8. LPC185x/3x/2x/1x Memory mapping (peripherals)

transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.16.3.1 Features

- Maximum SSP speed in full-duplex mode of 25 Mbit/s; for transmit only 50 Mbit/s (master) and 15 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- Eight-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.
- Connected to the GPDMA.

7.16.4 I^2C-bus interface

Remark: The LPC185x/3x/2x/1x contain two I^2C-bus interfaces.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus interface is a multi-master bus and can be controlled by more than one bus master connected to it.

7.16.4.1 Features

- I^2C0 is a standard I^2C-bus compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- All I^2C-bus controllers support multiple address recognition and a bus monitor mode.

7.16.5 I^2S interface

Remark: The LPC185x/3x/2x/1x contain two I^2S interfaces.

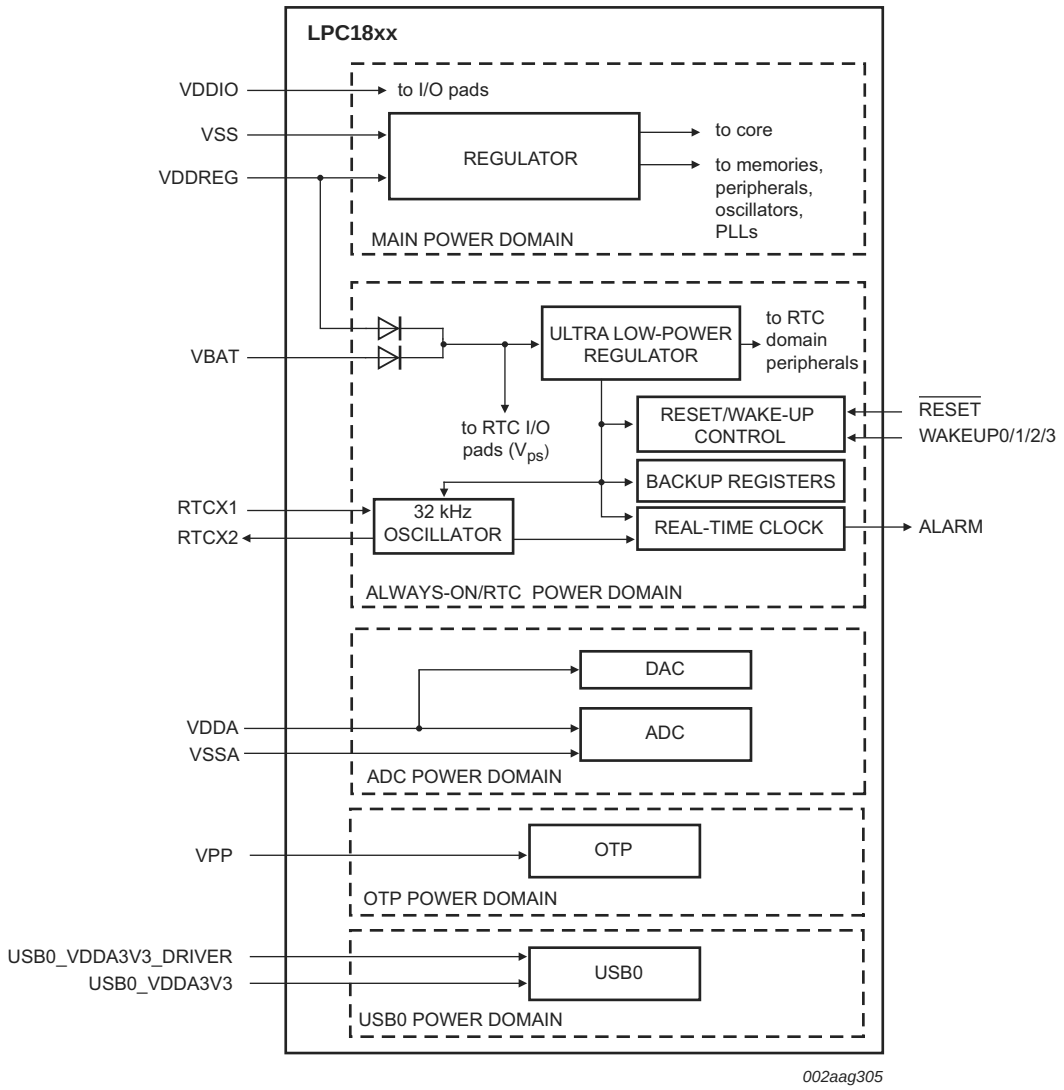


Fig 9. LPC185x/3x/2x/1x Power domains

The LPC185x/3x/2x/1x support four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.

The LPC185x/3x/2x/1x can wake up from Deep-sleep, Power-down, and Deep power-down modes via the WAKEUP[3:0] pins and interrupts generated by battery powered blocks in the RTC power domain.

7.20.10 Code security (Code Read Protection - CRP)

CRP enables different levels of security so that access to the on-chip flash and use of the JTAG and ISP can be restricted. CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by CRP.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of $I_{DD(REG)(3V3)}$ and $V_{DD(REG)(3V3)}$. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 8. Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature	-	-	125	°C

Table 9. Thermal resistance (LQFP packages)

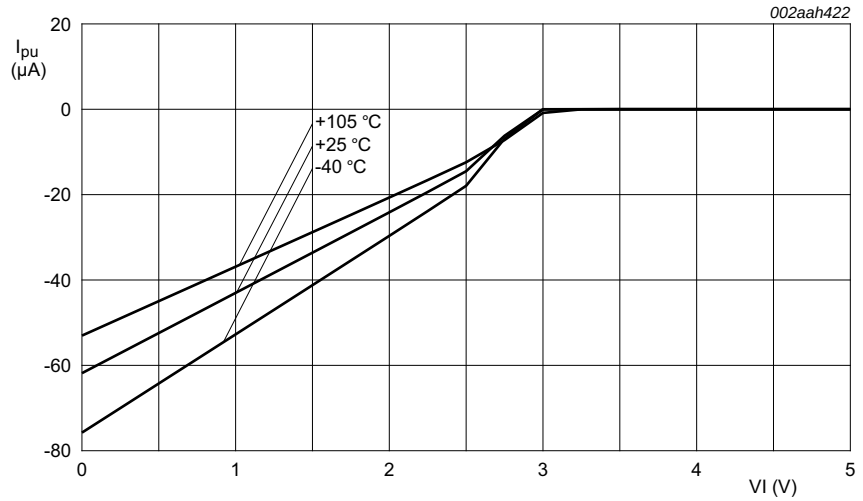
Symbol	Parameter	Conditions	Thermal resistance in °C/W ±15 %	
			LQFP144	LQFP208
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	38	31
		Single-layer (4.5 in × 3 in); still air	50	39
$R_{th(j-c)}$	thermal resistance from junction to case		11	10

Table 10. Thermal resistance value (BGA packages)

Symbol	Parameter	Conditions	Thermal resistance in °C/W ±15 %	
			LBGA256	TFBGA100
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	29	46
		8-layer (4.5 in × 3 in); still air	24	37
$R_{th(j-c)}$	thermal resistance from junction to case		14	11

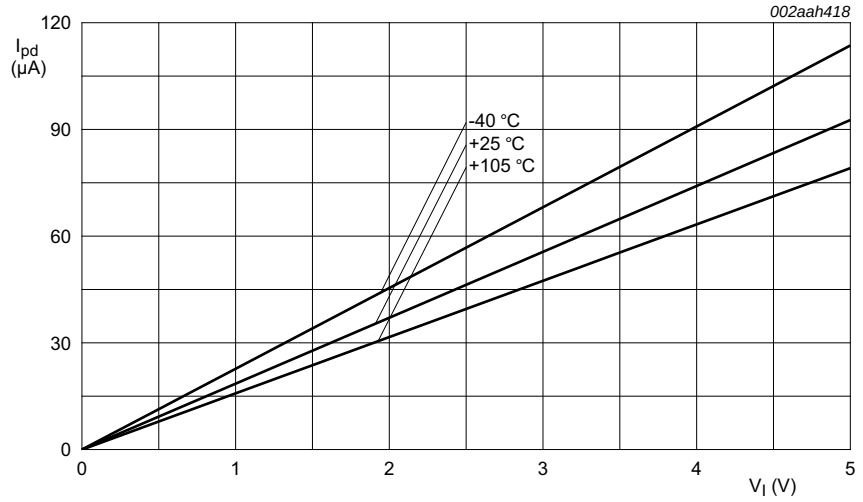
Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(IO)}$	I/O supply current	deep sleep mode		-	< 0.1	-	µA
		power-down mode		-	< 0.1	-	µA
		deep power-down mode		-	< 0.1	-	µA
I_{DDA}	Analog supply current	on pin VDDA; deep sleep mode	[9]	-	0.4	-	µA
		power-down mode	[9]	-	0.4	-	µA
		deep power-down mode	[9]	-	0.007	-	µA
$\overline{\text{RESET}}$ pin							
V_{IH}	HIGH-level input voltage		[8]	$0.8 \times (V_{ps} - 0.35)$	-	5.5	V
V_{IL}	LOW-level input voltage		[8]	0	-	$0.3 \times (V_{ps} - 0.1)$	V
V_{hys}	hysteresis voltage		[8]	$0.05 \times (V_{ps} - 0.35)$	-	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.5	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	40	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.4$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −6 mA		$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−6	-	-	mA



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

Fig 23. Pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

Fig 24. Pull-down current I_{pd} versus input voltage V_I

11.4 Crystal oscillator

Table 19. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 - 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.5 IRC oscillator

Table 20. Dynamic characteristic: IRC oscillator

2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-40 °C ≤ T_{amb} < 0 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz
		0 °C ≤ T_{amb} ≤ 85 °C	12.0 - 1.5 %	12.0	12.0 + 1.5 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 RTC oscillator

See Section 13.3 for connecting the RTC oscillator to an external clock source.

Table 21. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.4 V ≤ V_{BAT} ≤ 3.6 V[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz
$I_{CC(osc)}$	oscillator supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

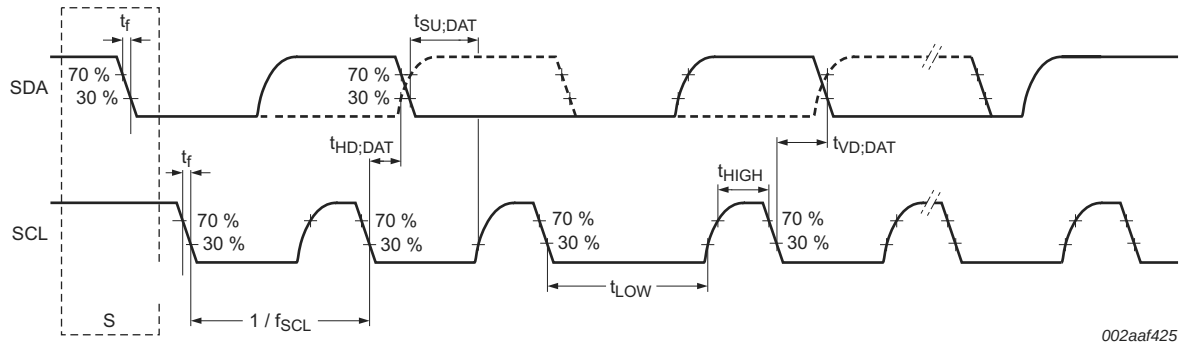


Fig 26. I^2C-bus pins clock timing

11.10 I^2S-bus interface

Table 25. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns, corresponds to the SCK signal in the *I^2S-bus specification*.

Table 28. Dynamic characteristics: Static asynchronous external memory interface *…continued*

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register.Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted which results in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	PB = 0	[2] [5]	−1.9 + $T_{cy(clk)}$	-	−0.5 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 0	[2]	−2.5 + $T_{cy(clk)}$	-	1.4 + $T_{cy(clk)}$	ns
t_{CSHEOW}	$\overline{CS}$ HIGH to end of write time		[5]	−2.0	-	0	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		−2.5	-	1.4	ns
t_{WEHANV}	WE HIGH to address invalid time	PB = 1		−0.9 + $T_{cy(clk)}$	-	2.4 + $T_{cy(clk)}$	ns

[1] Parameters specified for 40 % of $V_{DD(IO)}$ for rising edges and 60 % of $V_{DD(IO)}$ for falling edges.

[2] $T_{cy(clk)}$ = 1/CCLK (see *LPC18xx User manual*).

[3] End Of Read (EOR): longest of t_{CSHOEH}, t_{OEHANV}, $t_{CSHBLSH}$.

[4] Start Of Read (SOR): longest of t_{CSLAV}, t_{CSLOEL}, $t_{CSLBLSL}$.

[5] End Of Write (EOW): earliest of address not valid or $\overline{EMC\_BLSn}$ HIGH.

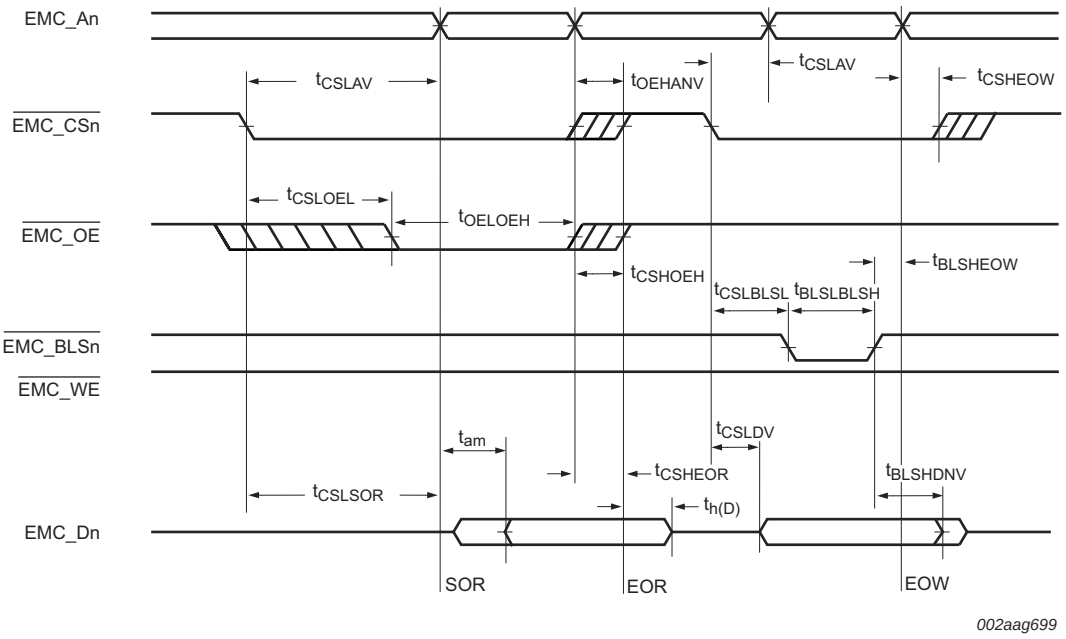


Fig 32. External static memory read/write access (PB = 0)

Table 29. Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for $\overline{EMC\_DYCSn}$, $\overline{EMC\_RAS}$, $\overline{EMC\_CAS}$, $\overline{EMC\_WE}$, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ =3.3 V ± 10 %; RD = 1 (see LPC18xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	dynamic chip select valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DYCS)}$	dynamic chip select hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	4.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	0.5 + 0.5 × $T_{cy(clk)}$	1.1 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	2.9 + 0.5 × $T_{cy(clk)}$	4.6 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	write enable valid delay time	-	3.2 + 0.5 × $T_{cy(clk)}$	5.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(WE)}$	write enable hold time	1.3 + 0.5 × $T_{cy(clk)}$	1.4 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	DQMOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.0 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	DQMOUT hold time	0.2 + 0.5 × $T_{cy(clk)}$	0.8 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.3 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	CKEOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	CKEOUT hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	2.2	0.8	-	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.2 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns

Table 30. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 105 °C; $V_{DD(IO)}$ =3.3 V ± 10 %; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	delay value	[1]				
		CLKn_DELAY = 0		0.0	0.0	0.0	ns
		CLKn_DELAY = 1	[1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2	[1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3	[1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4	[1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5	[1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6	[1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7	[1]	2.5	3.6	5.8	ns

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC18xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.

Table 41. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD0	-	-	-	-	-	-	P4_1	RED0
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB /LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC18xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode, couple the input clock signal with a capacitor of 100 pF (C_C in Figure 41), with an amplitude of at least 200 mV (RMS). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 42, and in Table 42 and Table 43. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (L, C_L and R_S represent the fundamental frequency). Capacitance C_P in Figure 42 represents the parallel package capacitance and must not be larger than 7 pF. Parameters F_C, C_L, R_S and C_P are supplied by the crystal manufacturer.

Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF

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