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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1827jet100e

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_1	R2	K2	42	58	[2]	N; PU	I/O	GPIO0[8] — General purpose digital input/output pin. External boot pin (see Table 5).
							O	CTOUT_7 — SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	EMC_A6 — External memory address line 6.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	SSP0_MISO — Master In Slave Out for SSP0.
							-	R — Function reserved.
							I/O	EMC_D13 — External memory data line 13.
P1_2	R3	K1	43	60	[2]	N; PU	I/O	GPIO0[9] — General purpose digital input/output pin. External boot pin (see Table 5).
							O	CTOUT_6 — SCTimer/PWM output 6. Match output 2 of timer 1.
							I/O	EMC_A7 — External memory address line 7.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	SSP0_MOSI — Master Out Slave in for SSP0.
							-	R — Function reserved.
							I/O	EMC_D14 — External memory data line 14.
P1_3	P5	J1	44	61	[2]	N; PU	I/O	GPIO0[10] — General purpose digital input/output pin.
							O	CTOUT_8 — SCTimer/PWM output 8. Match output 0 of timer 2.
							-	R — Function reserved.
							O	EMC_OE — LOW active Output Enable signal.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							I/O	SSP1_MISO — Master In Slave Out for SSP1.
							-	R — Function reserved.
							O	SD_RST — SD/MMC reset signal for MMC4.4 card.
P1_4	T3	J2	47	64	[2]	N; PU	I/O	GPIO0[11] — General purpose digital input/output pin.
							O	CTOUT_9 — SCTimer/PWM output 9. Match output 3 of timer 3.
							-	R — Function reserved.
							O	EMC_BLS0 — LOW active Byte Lane select signal 0.
							O	USB0_IND0 — USB0 port indicator LED control output 0.
							I/O	SSP1_MOSI — Master Out Slave in for SSP1.
							I/O	EMC_D15 — External memory data line 15.
							O	SD_VOLT1 — SD/MMC bus voltage select output 1.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_2	M15	F5	84	121	[2]	N; PU	-	R — Function reserved.
							I/O	U0_UCLK — Serial clock input/output for USART0 in synchronous mode.
							I/O	EMC_A11 — External memory address line 11.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							I/O	GPIO5[2] — General purpose digital input/output pin.
							I	CTIN_6 — SCTimer/PWM input 6. Capture input 1 of timer 3.
							I	T3_CAP2 — Capture input 2 of timer 3.
P2_3	J12	D8	87	127	[3]	N; PU	O	EMC_CS1 — LOW active Chip Select 1 signal.
							-	R — Function reserved.
							I/O	I2C1_SDA — I ² C1 data input/output (this pin does not use a specialized I ² C pad).
							O	U3_TXD — Transmitter output for USART3. See Table 4 for ISP mode.
							I	CTIN_1 — SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	GPIO5[3] — General purpose digital input/output pin.
							-	R — Function reserved.
P2_4	K11	D9	88	128	[3]	N; PU	O	T3_MAT0 — Match output 0 of timer 3.
							O	USB0_PPWR — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	R — Function reserved.
							I/O	I2C1_SCL — I ² C1 clock input/output (this pin does not use a specialized I ² C pad).
							I	U3_RXD — Receiver input for USART3. See Table 4 for ISP mode.
							I	CTIN_0 — SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	GPIO5[4] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT1 — Match output 1 of timer 3.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P3_8	C10	E7	124	179	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							I/O	SSP0_MOSI — Master Out Slave in for SSP0.
							I/O	SPIFI_CS — SPIFI serial flash chip select.
							I/O	GPIO5[11] — General purpose digital input/output pin.
							I/O	SSP0_SSEL — Slave Select for SSP0.
							-	R — Function reserved.
							-	R — Function reserved.
P4_0	D5	-	1	1	[2]	N; PU	I/O	GPIO2[0] — General purpose digital input/output pin.
							O	MCOA0 — Motor control PWM channel 0, output A.
							I	NMI — External interrupt input to NMI.
							-	R — Function reserved.
							-	R — Function reserved.
							O	LCD_VD13 — LCD data.
							I/O	U3_UCLK — Serial clock input/output for USART3 in synchronous mode.
							-	R — Function reserved.
P4_1	A1	-	3	3	[5]	N; PU	I/O	GPIO2[1] — General purpose digital input/output pin.
							O	CTOUT_1 — SCTimer/PWM output 1. Match output 3 of timer 3.
							O	LCD_VD0 — LCD data.
							-	R — Function reserved.
							-	R — Function reserved.
							O	LCD_VD19 — LCD data.
							O	U3_TXD — Transmitter output for USART3.
							I	ENET_COL — Ethernet Collision detect (MII interface).
P4_2	D3	-	8	12	[2]	N; PU	AI	ADC0_1 — ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							I/O	GPIO2[2] — General purpose digital input/output pin.
							O	CTOUT_0 — SCTimer/PWM output 0. Match output 0 of timer 0.
							O	LCD_VD3 — LCD data.
							-	R — Function reserved.
							-	R — Function reserved.
							O	LCD_VD12 — LCD data.
							I	U3_RXD — Receiver input for USART3.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_10	M3	-	35	51	[2]	N; PU	-	R — Function reserved.
							I	CTIN_2 — SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	LCD_VD10 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[14] — General purpose digital input/output pin.
							O	LCD_VD14 — LCD data.
							-	R — Function reserved.
							-	R — Function reserved.
P5_0	N3	-	37	53	[2]	N; PU	I/O	GPIO2[9] — General purpose digital input/output pin.
							O	MCOB2 — Motor control PWM channel 2, output B.
							I/O	EMC_D12 — External memory data line 12.
							-	R — Function reserved.
							I	U1_DSR — Data Set Ready input for UART1.
							I	T1_CAP0 — Capture input 0 of timer 1.
							-	R — Function reserved.
P5_1	P3	-	39	55	[2]	N; PU	I/O	GPIO2[10] — General purpose digital input/output pin.
							I	MCI2 — Motor control PWM channel 2, input.
							I/O	EMC_D13 — External memory data line 13.
							-	R — Function reserved.
							O	U1_DTR — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	T1_CAP1 — Capture input 1 of timer 1.
							-	R — Function reserved.
P5_2	R4	-	46	63	[2]	N; PU	I/O	GPIO2[11] — General purpose digital input/output pin.
							I	MCI1 — Motor control PWM channel 1, input.
							I/O	EMC_D14 — External memory data line 14.
							-	R — Function reserved.
							O	U1_RTS — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	T1_CAP2 — Capture input 2 of timer 1.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P7_5	A7	-	133	191	[5]	N; PU	I/O	GPIO3[13] — General purpose digital input/output pin.
							O	CTOUT_12 — SCTimer/PWM output 12. Match output 3 of timer 3.
							-	R — Function reserved.
							O	LCD_VD8 — LCD data.
							O	LCD_VD23 — LCD data.
							O	TRACEDATA[1] — Trace data, bit 1.
							-	R — Function reserved.
							-	R — Function reserved.
							AI	ADC0_3 — ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	-	134	194	[2]	N; PU	I/O	GPIO3[14] — General purpose digital input/output pin.
							O	CTOUT_11 — SCTimer/PWM output 1. Match output 3 of timer 2.
							-	R — Function reserved.
							O	LCD_LP — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	R — Function reserved.
							O	TRACEDATA[2] — Trace data, bit 2.
							-	R — Function reserved.
P7_7	B6	-	140	201	[5]	N; PU	I/O	GPIO3[15] — General purpose digital input/output pin.
							O	CTOUT_8 — SCTimer/PWM output 8. Match output 0 of timer 2.
							-	R — Function reserved.
							O	LCD_PWR — LCD panel power enable.
							-	R — Function reserved.
							O	TRACEDATA[3] — Trace data, bit 3.
							O	ENET_MDC — Ethernet MIIM clock.
							-	R — Function reserved.
							AI	ADC1_6 — ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P8_0	E5	-	-	2	[3]	N; PU	I/O	GPIO4[0] — General purpose digital input/output pin.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	R — Function reserved.
							I	MCI2 — Motor control PWM channel 2, input.
							-	R — Function reserved.
							-	R — Function reserved.
							O	T0_MAT0 — Match output 0 of timer 0.
P8_1	H5	-	-	34	[3]	N; PU	I/O	GPIO4[1] — General purpose digital input/output pin.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							-	R — Function reserved.
							I	MCI1 — Motor control PWM channel 1, input.
							-	R — Function reserved.
							-	R — Function reserved.
							O	T0_MAT1 — Match output 1 of timer 0.
P8_2	K4	-	-	36	[3]	N; PU	I/O	GPIO4[2] — General purpose digital input/output pin.
							O	USB0_IND0 — USB0 port indicator LED control output 0.
							-	R — Function reserved.
							I	MCI0 — Motor control PWM channel 0, input.
							-	R — Function reserved.
							-	R — Function reserved.
							O	T0_MAT2 — Match output 2 of timer 0.
P8_3	J3	-	-	37	[2]	N; PU	I/O	GPIO4[3] — General purpose digital input/output pin.
							I/O	USB1_ULPI_D2 — ULPI link bidirectional data line 2.
							-	R — Function reserved.
							O	LCD_VD12 — LCD data.
							O	LCD_VD19 — LCD data.
							-	R — Function reserved.
							O	T0_MAT3 — Match output 3 of timer 0.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PA_4	G13	-	-	151	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_9 — SCTimer/PWM output 9. Match output 3 of timer 3.
							-	R — Function reserved.
							I/O	EMC_A23 — External memory address line 23.
							I/O	GPIO5[19] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
PB_0	B15	-	-	164	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_10 — SCTimer/PWM output 10. Match output 3 of timer 3.
							O	LCD_VD23 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[20] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
PB_1	A14	-	-	175	[2]	N; PU	-	R — Function reserved.
							I	USB1_ULPI_DIR — ULPI link DIR signal. Controls the ULP data line direction.
							O	LCD_VD22 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[21] — General purpose digital input/output pin.
							O	CTOUT_6 — SCTimer/PWM output 6. Match output 2 of timer 1.
							-	R — Function reserved.
PB_2	B12	-	-	177	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D7 — ULPI link bidirectional data line 7.
							O	LCD_VD21 — LCD data.
							-	R — Function reserved.
							I/O	GPIO5[22] — General purpose digital input/output pin.
							O	CTOUT_7 — SCTimer/PWM output 7. Match output 3 of timer 1.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PE_11	D16	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_12 — SCTimer/PWM output 12. Match output 3 of timer 3.
							O	U1_TXD — Transmitter output for UART1.
							I/O	EMC_D30 — External memory data line 30.
							I/O	GPIO7[11] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_11 — SCTimer/PWM output 11. Match output 3 of timer 2.
							I	U1_RXD — Receiver input for UART1.
							I/O	EMC_D31 — External memory data line 31.
							I/O	GPIO7[12] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	CTOUT_14 — SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	I2C1_SDA — I ² C1 data input/output (this pin does not use a specialized I ² C pad).
							O	EMC_DQMOUT3 — Data mask 3 used with SDRAM and static devices.
							I/O	GPIO7[13] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
PE_14	C15	-	-	-	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							O	EMC_DYCS3 — SDRAM chip select 3.
							I/O	GPIO7[14] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PF_6	E7	-	-	192	[5]	N; PU	-	R — Function reserved.
							I/O	U3_DIR — RS-485/EIA-485 output enable/direction control for USART3.
							I/O	SSP1_MISO — Master In Slave Out for SSP1.
							O	TRACEDATA[1] — Trace data, bit 1.
							I/O	GPIO7[20] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							I/O	I2S1_TX_SDA — I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I2S-bus specification.
PF_7	B7	-	-	193	[5]	N; PU	AI	ADC1_3 — ADC1 and ADC0, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							-	R — Function reserved.
							I/O	U3_BAUD — Baud pin USART3.
							I/O	SSP1_MOSI — Master Out Slave in for SSP1.
							O	TRACEDATA[2] — Trace data, bit 2.
							I/O	GPIO7[21] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
PF_8	E6	-	-	-	[5]	N; PU	I/O	I2S1_TX_WS — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the I2S-bus specification.
							AI/ O	ADC1_7 — ADC1 and ADC0, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							-	R — Function reserved.
							I/O	U0_UCLK — Serial clock input/output for USART0 in synchronous mode.
							I	CTIN_2 — SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	TRACEDATA[3] — Trace data, bit 3.
							I/O	GPIO7[22] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							AI	ADC0_2 — ADC0 and ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

7.4 AHB multilayer matrix

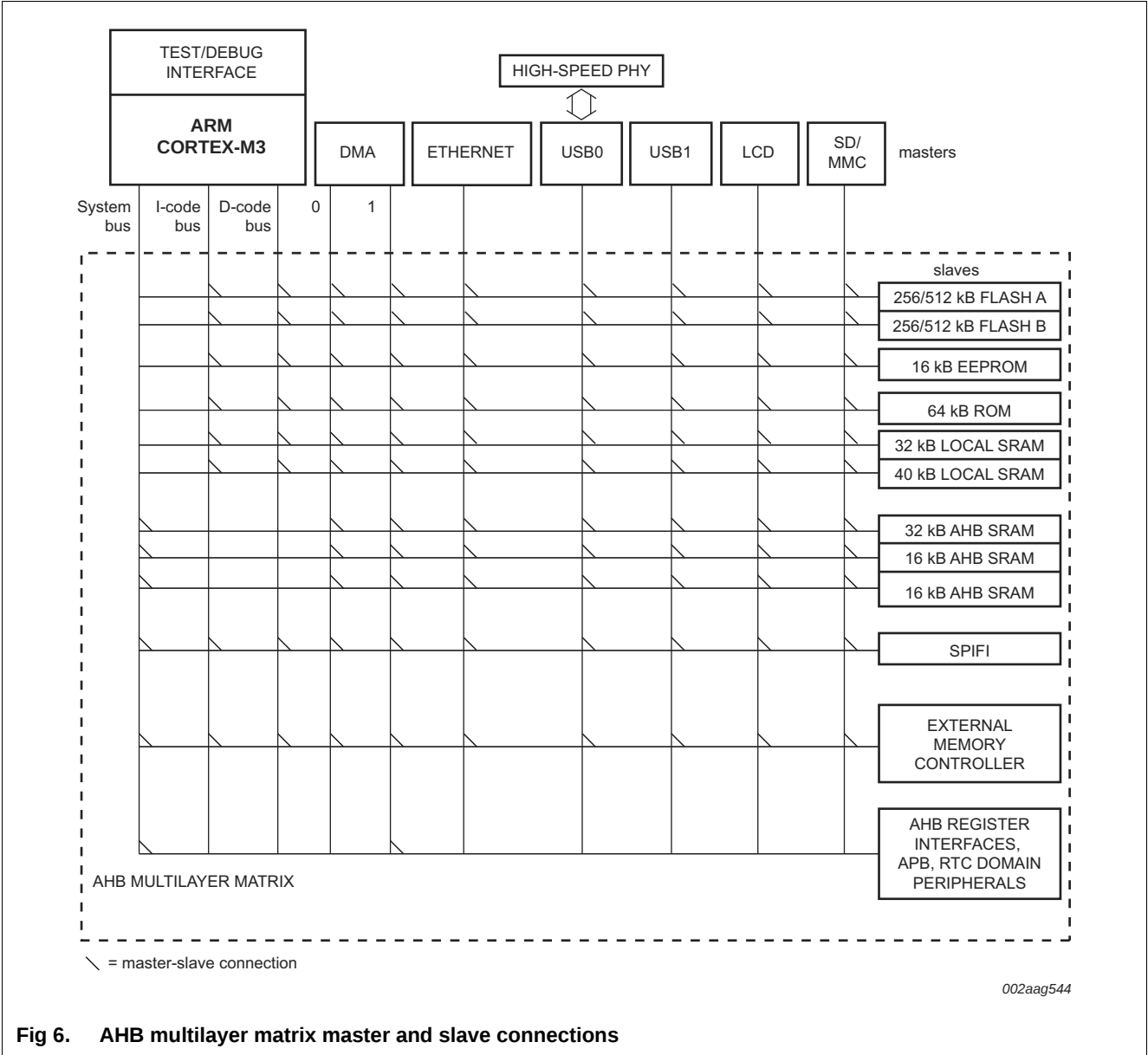


Fig 6. AHB multilayer matrix master and slave connections

7.5 Nested Vectored Interrupt Controller (NVIC)

The NVIC is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC185x/3x/2x/1x, the NVIC supports 53 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.

7.15.7 High-speed USB Host/Device interface with ULPI (USB1)

Remark: USB1 is available on the following parts: LPC185x and LPC183x. USB1 is not available on the LPC182x and LPC181x parts.

The USB1 interface can operate as a full-speed USB host/device interface or can connect to an external ULPI PHY for High-speed operation.

7.15.7.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.15.8 LCD controller

Remark: The LCD controller is only available on parts LPC185x. LCD is not available on parts LPC183x, LPC182x, and LPC181x.

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

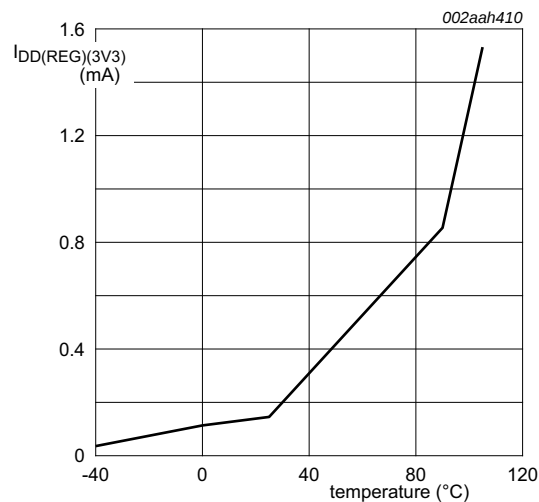
The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.15.8.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.

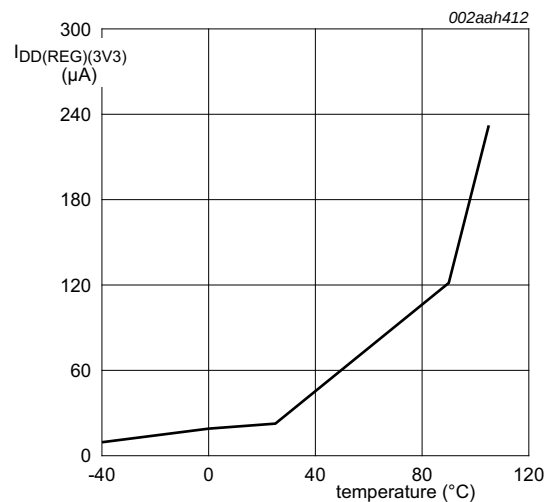
Table 11. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
I _{DD(I/O)}	I/O supply current	deep sleep mode		-	< 0.1	-	μA
		power-down mode		-	< 0.1	-	μA
		deep power-down mode		-	< 0.1	-	μA
I _{DDA}	Analog supply current	on pin VDDA; deep sleep mode	[9]	-	0.4	-	μA
		power-down mode	[9]	-	0.4	-	μA
		deep power-down mode	[9]	-	0.007	-	μA
RESET pin							
V _{IH}	HIGH-level input voltage		[8]	0.8 × (V _{ps} – 0.35)	-	5.5	V
V _{IL}	LOW-level input voltage		[8]	0	-	0.3 × (V _{ps} – 0.1)	V
V _{hys}	hysteresis voltage		[8]	0.05 × (V _{ps} – 0.35)	-	-	V
Standard I/O pins - normal drive strength							
C _I	input capacitance			-	-	2	pF
I _{LL}	LOW-level leakage current	V _I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I _{LH}	HIGH-level leakage current	V _I = V _{DD(I/O)} ; on-chip pull-down resistor disabled		-	3	-	nA
		V _I = 5 V; T _{amb} = 25 °C		-	0.5	-	nA
		V _I = 5 V; T _{amb} = 105 °C		-	40	-	nA
I _{OZ}	OFF-state output current	V _O = 0 V to V _{DD(I/O)} ; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V _I	input voltage	pin configured to provide a digital function; V _{DD(I/O)} ≥ 2.4 V		0	-	5.5	V
		V _{DD(I/O)} = 0 V		0	-	3.6	V
V _O	output voltage	output active		0	-	V _{DD(I/O)}	V
V _{IH}	HIGH-level input voltage			0.7 × V _{DD(I/O)}	-	5.5	V
V _{IL}	LOW-level input voltage			0	-	0.3 × V _{DD(I/O)}	V
V _{hys}	hysteresis voltage			0.1 × V _{DD(I/O)}	-	-	V
V _{OH}	HIGH-level output voltage	I _{OH} = –6 mA		V _{DD(I/O)} – 0.4	-	-	V
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA		-	-	0.4	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD(I/O)} – 0.4 V		–6	-	-	mA



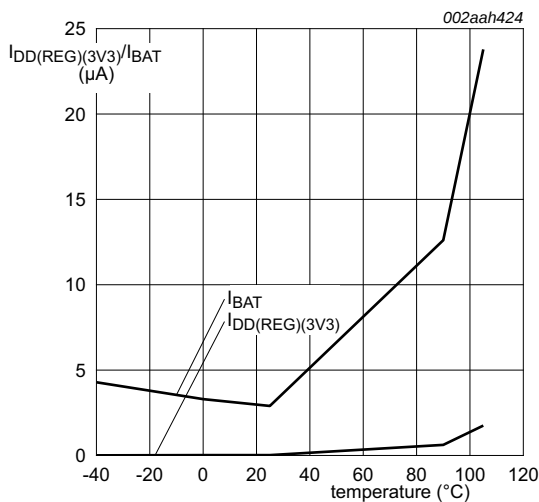
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$.

Fig 14. Typical supply current versus temperature in Deep-sleep mode



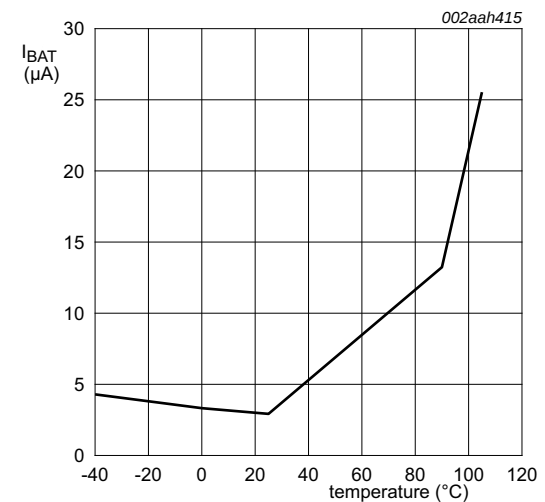
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$.

Fig 15. Typical supply current versus temperature in Power-down mode



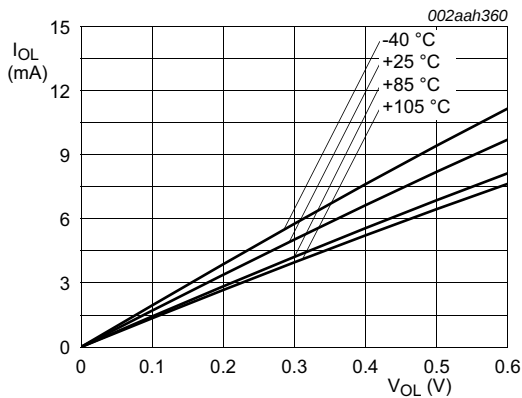
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$. $V_{BAT} = V_{DD(REG)(3V3)} + 0.4\text{ V}$.

Fig 16. Typical supply current versus temperature in Deep power-down mode

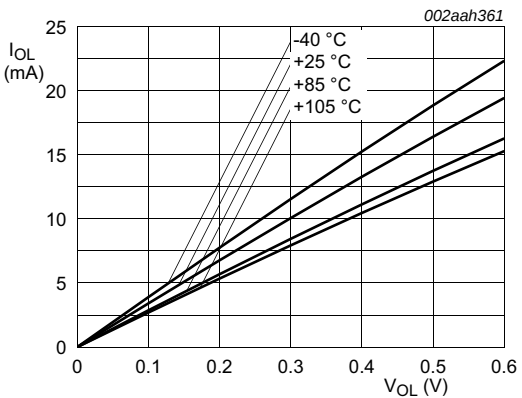


Conditions: $V_{BAT} = 3.6\text{ V}$. $V_{DD(REG)(3V3)}$ not present.

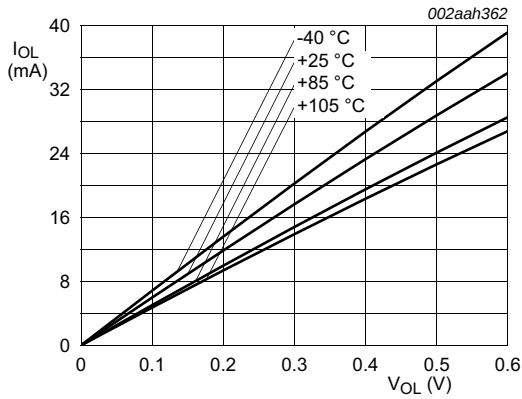
Fig 17. Typical battery supply current versus temperature



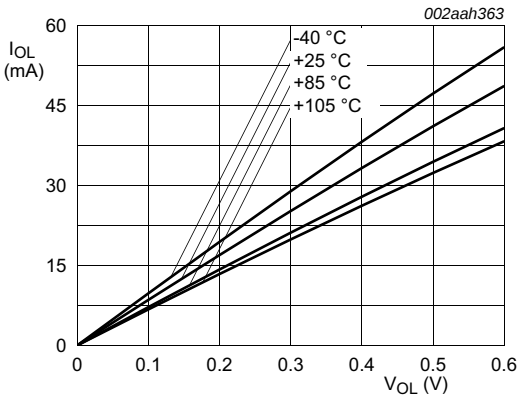
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; medium-drive; EHD = 0x1.

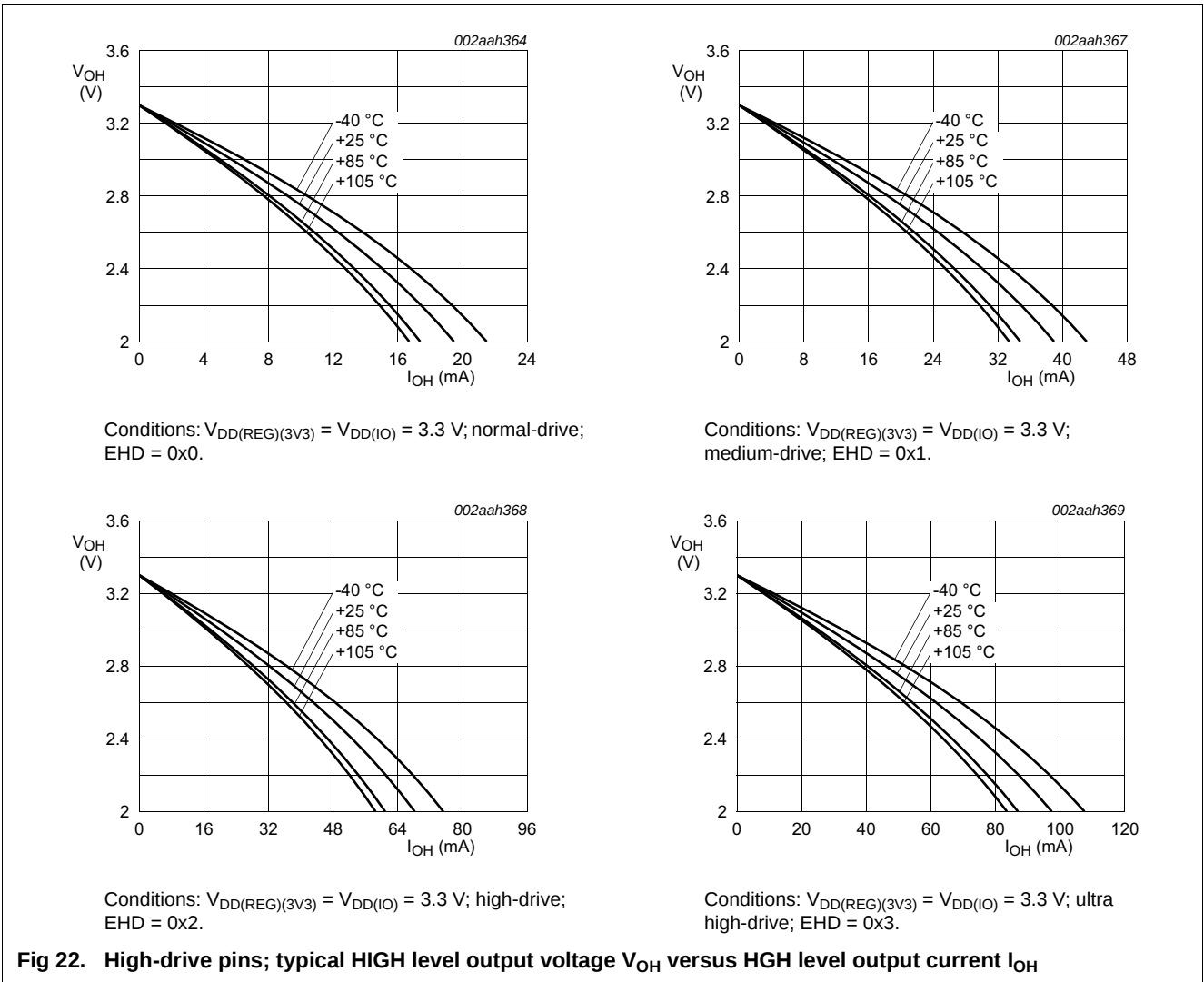


Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; ultra high-drive; EHD = 0x3.

Fig 21. High-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



11.16 SD/MMC

Table 34. Dynamic characteristics: SD/MMC

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$; $2.7\text{ V} \leq V_{DD(I/O)} \leq 3.6\text{ V}$; $C_L = 20\text{ pF}$. Simulated values. $SAMPLE_DELAY = 0x9$, $DRV_DELAY = 0x6$ in the $SDDELAY$ register sampled at 90 % and 10 % of the signal level, $EHS = 1$ for SD_CLK pin, $EHS = 0$ for SD_DATn and SD_CMD pins. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK ; data transfer mode	-	52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	5.2	-	ns
		on pins SD_CMD as inputs	7	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0.2	-	ns
		on pins SD_CMD as inputs	-1	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_DATn as outputs	-	15.7	ns
		on pins SD_CMD as outputs	-	15.9	ns
$t_{h(Q)}$	data output hold time	on pins SD_DATn as outputs	3.5	-	ns
		on pins SD_CMD as outputs	3.5	-	ns

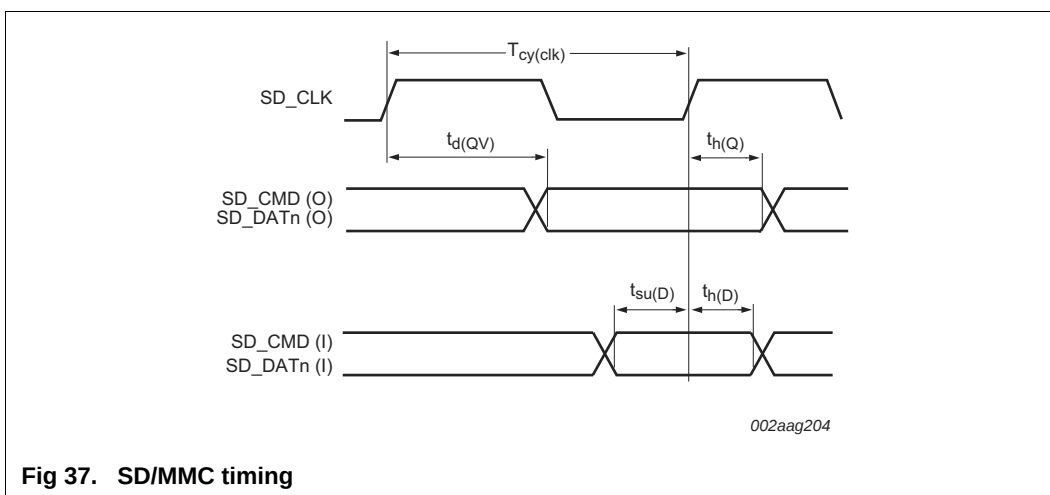


Fig 37. SD/MMC timing

11.17 LCD

Table 35. Dynamic characteristics: LCD

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$; $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$; $2.7\text{ V} \leq V_{DD(I/O)} \leq 3.6\text{ V}$; $C_L = 20\text{ pF}$. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time		-	-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-	-	ns

13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{RTCX1} and C_{RTCX2} need to be connected externally. Typical capacitance values for C_{RTCX1} and C_{RTCX2} are $C_{RTCX1/2} = 20$ (typical) ± 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)} = 100$ mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

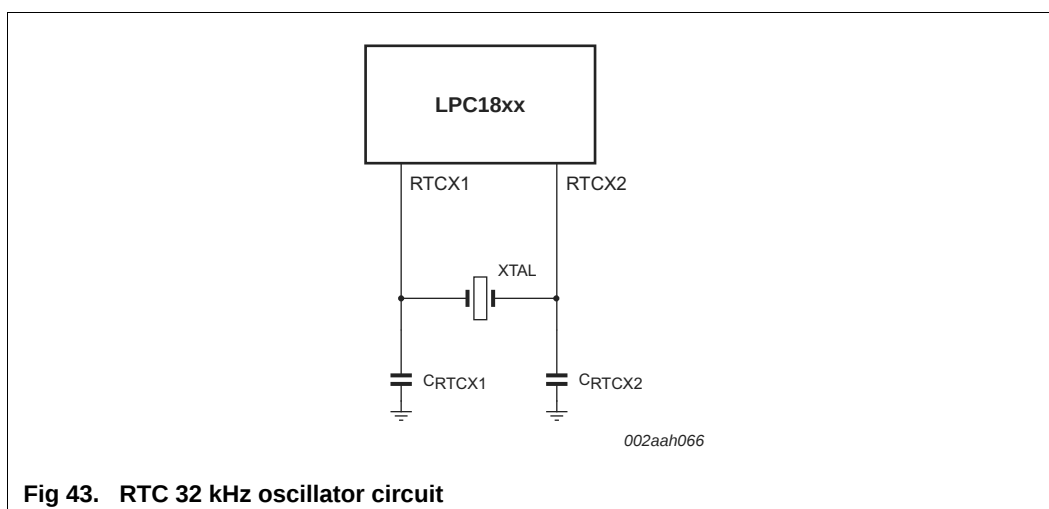


Fig 43. RTC 32 kHz oscillator circuit

13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1} , C_{X2} , and C_{X3} in case of third overtone crystal usage have a common ground plane. Also connect the external components to the ground plane. To keep the noise coupled in via the PCB as small as possible, make loops and parasitics as small as possible. Choose smaller values of C_{X1} and C_{X2} if parasitics increase in the PCB layout.

Ensure no high-speed or high-drive signals are near the RTCX1/2 signals.

13.5 Standard I/O pin configuration

Figure 44 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input buffer enabled/disabled
- Analog input

The default configuration for standard I/O pins is input buffer disabled and pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm

SOT459-1

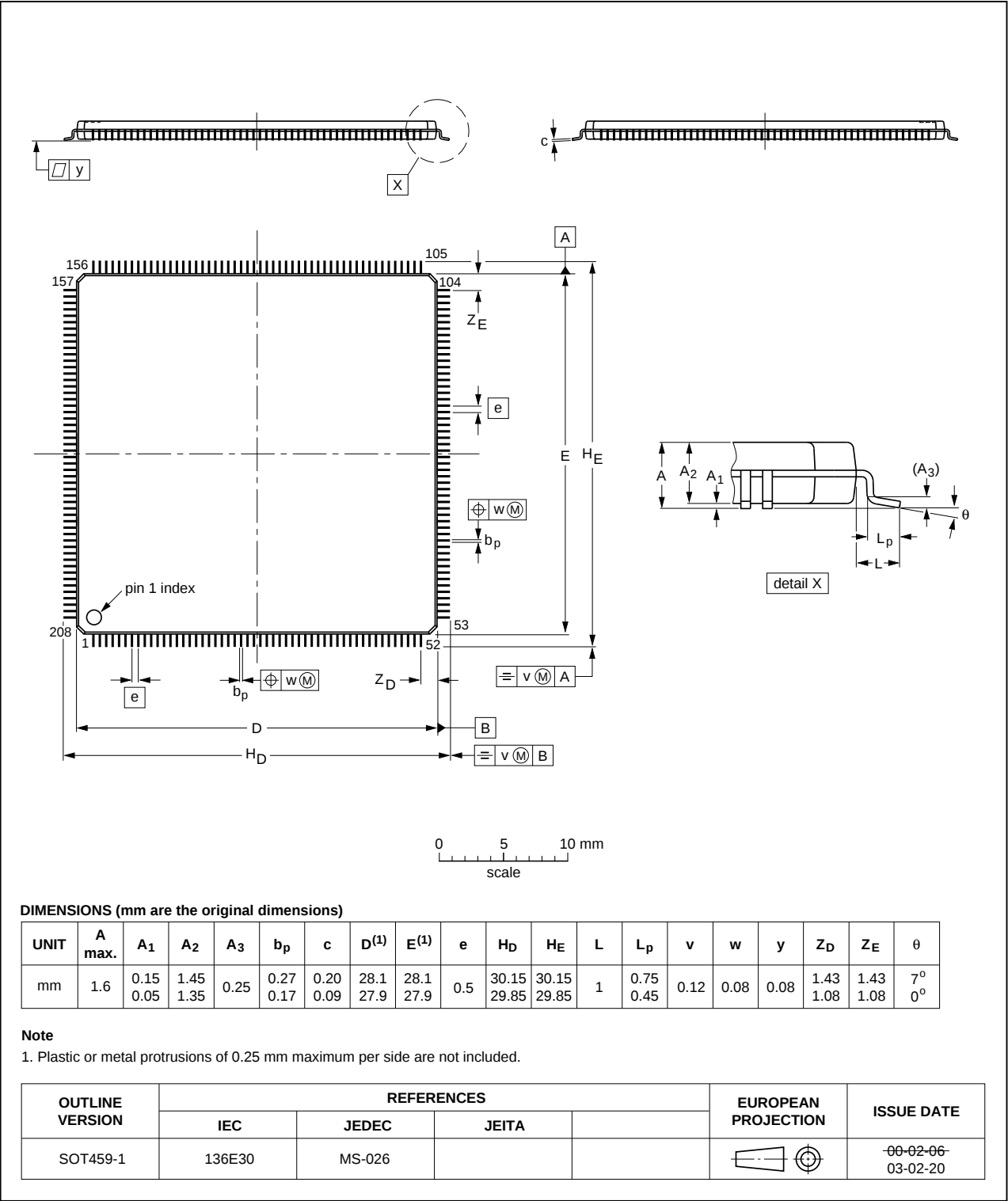
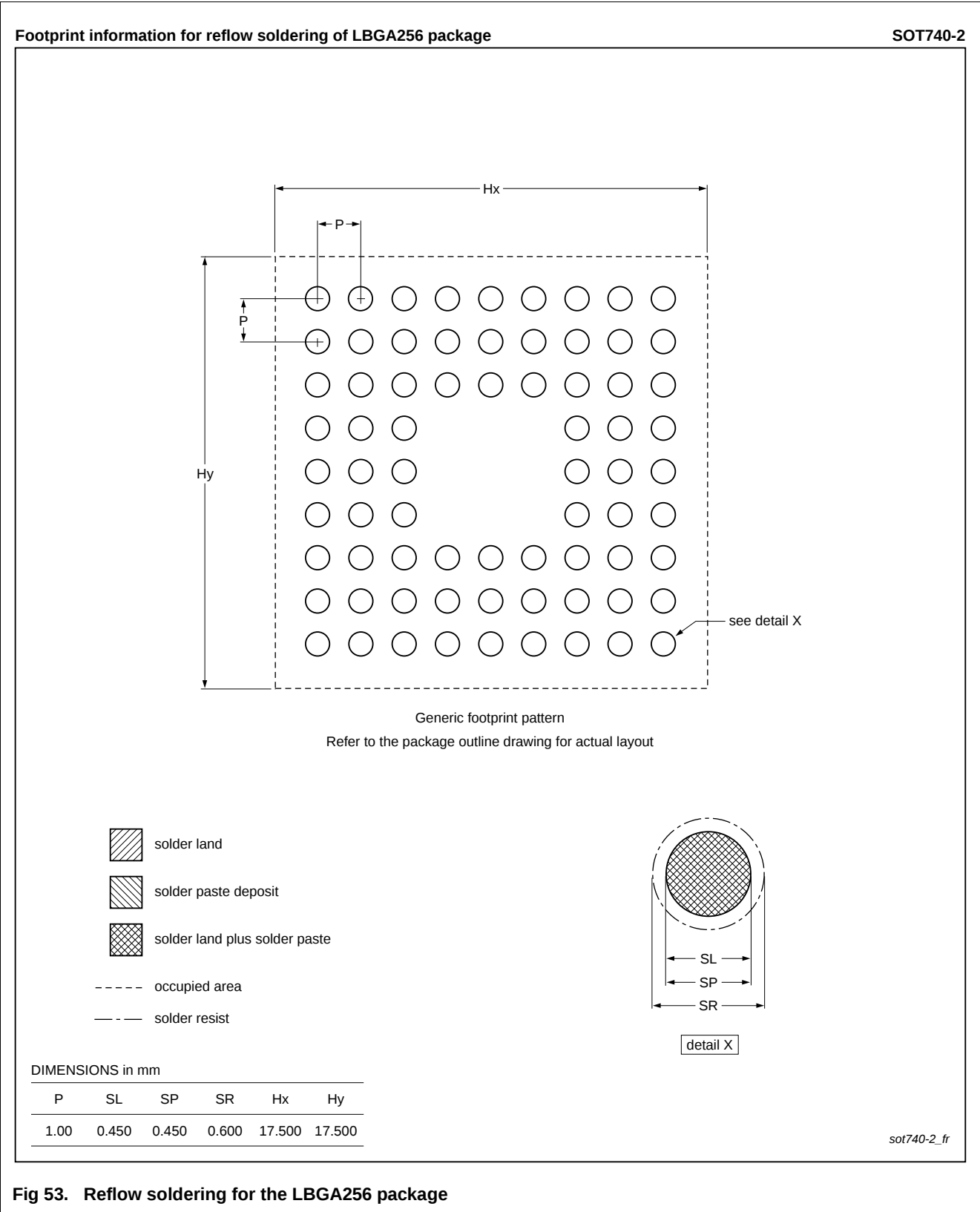


Fig 51. Package outline of the LQFP208 package

15. Soldering



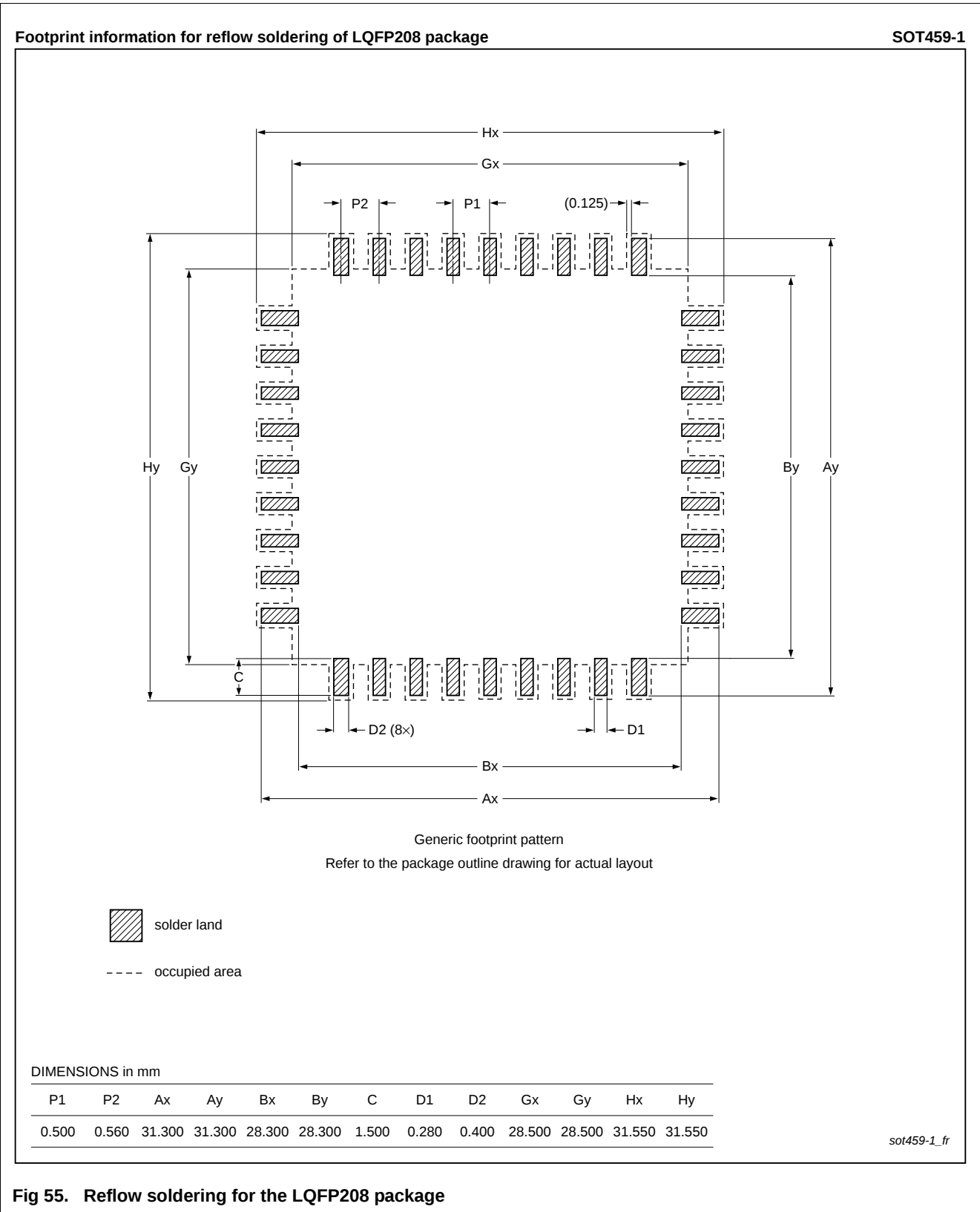


Fig 55. Reflow soldering for the LQFP208 package