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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1837jbd144e

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_1	R2	K2	42	58	[2]	N; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin. External boot pin (see Table 5).
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	**EMC_A6 —** External memory address line 6.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							I/O	**EMC_D13 —** External memory data line 13.
P1_2	R3	K1	43	60	[2]	N; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin. External boot pin (see Table 5).
							O	**CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1.
							I/O	**EMC_A7 —** External memory address line 7.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							I/O	**EMC_D14 —** External memory data line 14.
P1_3	P5	J1	44	61	[2]	N; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							-	**R —** Function reserved.
							O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
P1_4	T3	J2	47	64	[2]	N; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
							O	**CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							I/O	**EMC_D15 —** External memory data line 15.
							O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_12	R9	K7	56	78	[2]	N; PU	I/O	**GPIO1[5] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D5 —** External memory data line 5.
							I	**T0_CAP1 —** Capture input 1 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
P1_13	R10	H8	60	83	[2]	N; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D6 —** External memory data line 6.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**SD_CD —** SD/MMC card detect input.
P1_14	R11	J8	61	85	[2]	N; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D7 —** External memory data line 7.
							O	**T0_MAT2 —** Match output 2 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_15	T12	K8	62	87	[2]	N; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1 —** Match output 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_12	E15	B9	106	153	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A3 —** External memory address line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
P2_13	C16	A10	108	156	[2]	N; PU	I/O	**GPIO1[13] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							-	**R —** Function reserved.
							I/O	**EMC_A4 —** External memory address line 4.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
P3_0	F13	A8	112	161	[2]	N; PU	I/O	**I2S0_RX_SCK —** I^2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							O	**I2S0_RX_MCLK —** I^2S receive master clock.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							O	**I2S0_TX_MCLK —** I^2S transmit master clock.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P7_5	A7	-	133	191	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	-	134	194	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_7	B6	-	140	201	[5]	N; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							AI	**ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P8_0	E5	-	-	2	[3]	N; PU	I/O	**GPIO4[0] —** General purpose digital input/output pin.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**MCI2 —** Motor control PWM channel 2, input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT0 —** Match output 0 of timer 0.
P8_1	H5	-	-	34	[3]	N; PU	I/O	**GPIO4[1] —** General purpose digital input/output pin.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							-	**R —** Function reserved.
							I	**MCI1 —** Motor control PWM channel 1, input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT1 —** Match output 1 of timer 0.
P8_2	K4	-	-	36	[3]	N; PU	I/O	**GPIO4[2] —** General purpose digital input/output pin.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							-	**R —** Function reserved.
							I	**MCI0 —** Motor control PWM channel 0, input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT2 —** Match output 2 of timer 0.
P8_3	J3	-	-	37	[2]	N; PU	I/O	**GPIO4[3] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							O	**LCD_VD19 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT3 —** Match output 3 of timer 0.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PB_3	A13	-	-	178	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
							O	**LCD_VD20 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[23] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_4	B11	-	-	180	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[24] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_5	A12	-	-	181	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[25] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
PB_6	A6	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
							O	**LCD_VD13 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[26] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD19 —** LCD data.
							-	**R —** Function reserved.
							AI	**ADC0_6** and ADC1 **—** ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

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- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.6 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts.
- C_CAN0/1 and QEI interrupts.
- Ethernet, USB0, USB1 signals.
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3).

Remark: Any interrupt can wake up the ARM Cortex-M3 from sleep mode if enabled in the NVIC.

7.7 Global Input Multiplexer Array (GIMA)

The GIMA routes signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.

7.7.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.8 On-chip static RAM

The LPC185x/3x/2x/1x support up to 136 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

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7.12 Memory mapping

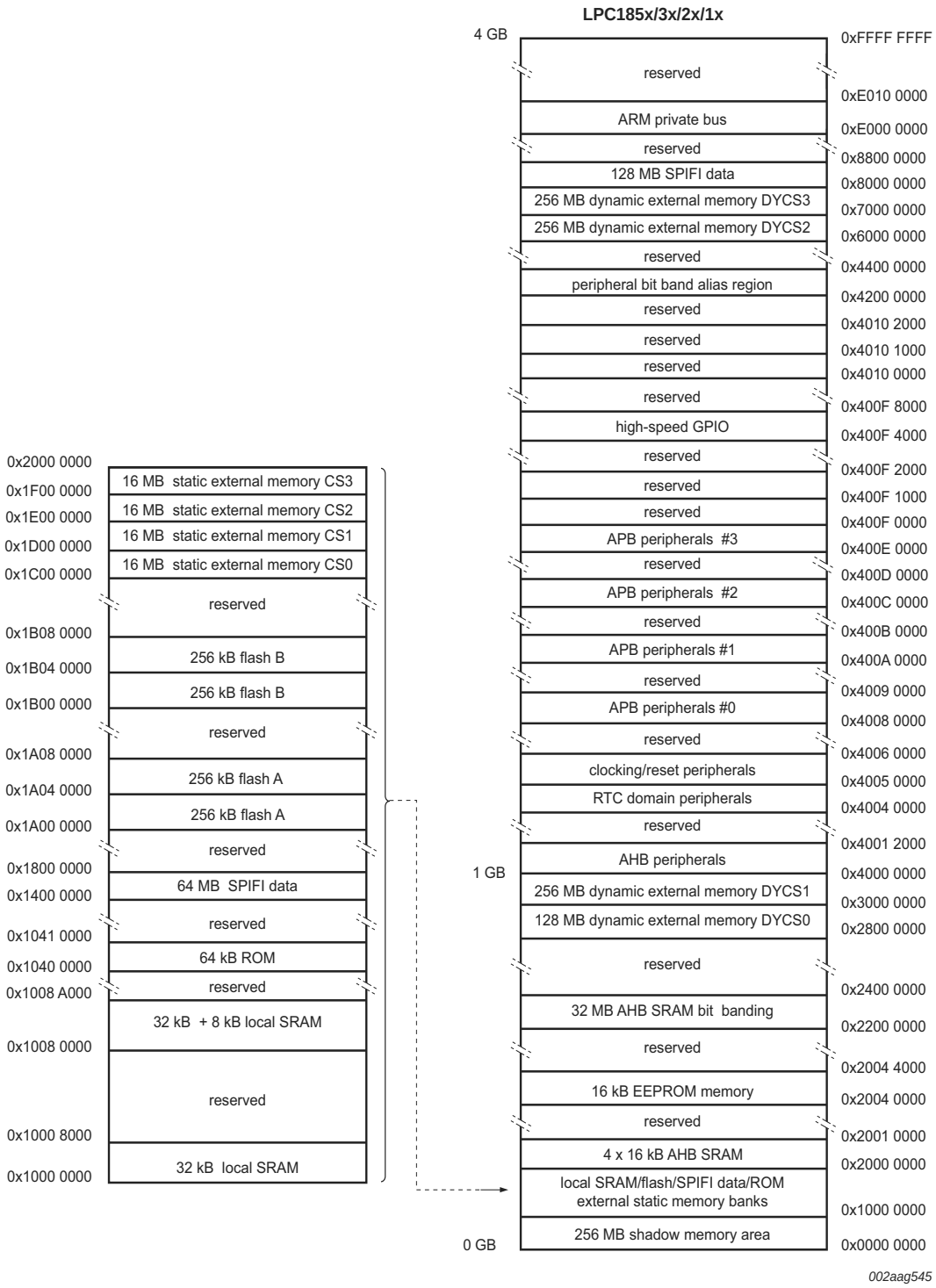

Fig 7. LPC185x/3x/2x/1x Memory mapping (overview)

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- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.15.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Events control outputs, interrupts, and DMA requests.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states
  - Match register 0 to 5 support a fractional component for the dither engine

7.15.2 General-Purpose DMA

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.15.2.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.

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7.15.4 SD/MMC card interface

The SD/MMC card interface supports the following modes:

- Secure Digital memory (SD version 3.0).
- Secure Digital I/O (SDIO version 2.0).
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1).
- Multimedia Cards (MMC version 4.4).

7.15.5 External Memory Controller (EMC)

Remark: The EMC is available on all LPC185x/3x/2x/1x parts. The following memory bus widths are supported:

- LBGA256 packages: 32 bit
- TFBGA100 packages: 8 bit
- LQFP208 packages: 16 bit
- LQFP144 packages: 16 bit

The LPC185x/3x/2x/1x EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

Table 6. EMC pinout for different packages

Function	LBGA256	TFBGA100	LQFP208	LQFP144
A	EMC_A[23:0]	EMC_A[13:0]	EMC_A[23:0]	EMC_A[15:0]
D	EMC_D[31:0]	EMC_D[7:0]	EMC_D[15:0]	EMC_D[15:0]
$\overline{BLS}$	$\overline{EMC\_BLS[3:0]}$	$\overline{EMC\_BLS0}$	$\overline{EMC\_BLS[1:0]}$	$\overline{EMC\_BLS[1:0]}$
$\overline{CS}$	$\overline{EMC\_CS[3:0]}$	$\overline{EMC\_CS0}$	$\overline{EMC\_CS[1:0]}$	$\overline{EMC\_CS[1:0]}$
$\overline{OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$
$\overline{WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$
CKEOUT	EMC_ CKEOUT[3:0]	EMC_ CKEOUT[1:0]	EMC_ CKEOUT[1:0]	EMC_ CKEOUT[1:0]
CLK	EMC_CLK[3:0]; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23
DQMOUT	EMC_ DQMOUT[3:0]	-	EMC_ DQMOUT[1:0]	EMC_ DQMOUT[1:0]
$\overline{DYCS}$	$\overline{EMC\_DYCS[3:0]}$	$\overline{EMC\_DYCS[1:0]}$	$\overline{EMC\_DYCS[1:0]}$	$\overline{EMC\_DYCS[1:0]}$
$\overline{CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$
$\overline{RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$

7.15.5.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.

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- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines-wide static memory support.
- 16-bit and 32-bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs.
- Software-controlled dynamic memory self-refresh mode.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts.
- Separate reset domains allow auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.15.6 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on the following parts: LPC185x, LPC183x, LPC182x. USB0 is not available on the LPC181x parts.

The USB OTG module allows the part to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode.

7.15.6.1 Features

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I/O pins - high drive strength: standard drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	65	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.7	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	70	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	63	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10]	-	-	110	mA

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Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns
SSP slave							
PCLK	Peripheral clock frequency			-	-	180	MHz
$T_{cy(clk)}$	clock cycle time		[2]	$1/(11 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		1.5	-	-	ns
t_{DH}	data hold time	in SPI mode		2	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	[4 × (1/PCLK)] + 1	ns
$t_{h(Q)}$	data output hold time	in SPI mode		4.5	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$	-	-	ns
		microwire frame format		$T_{cy(clk)}$	-	-	ns

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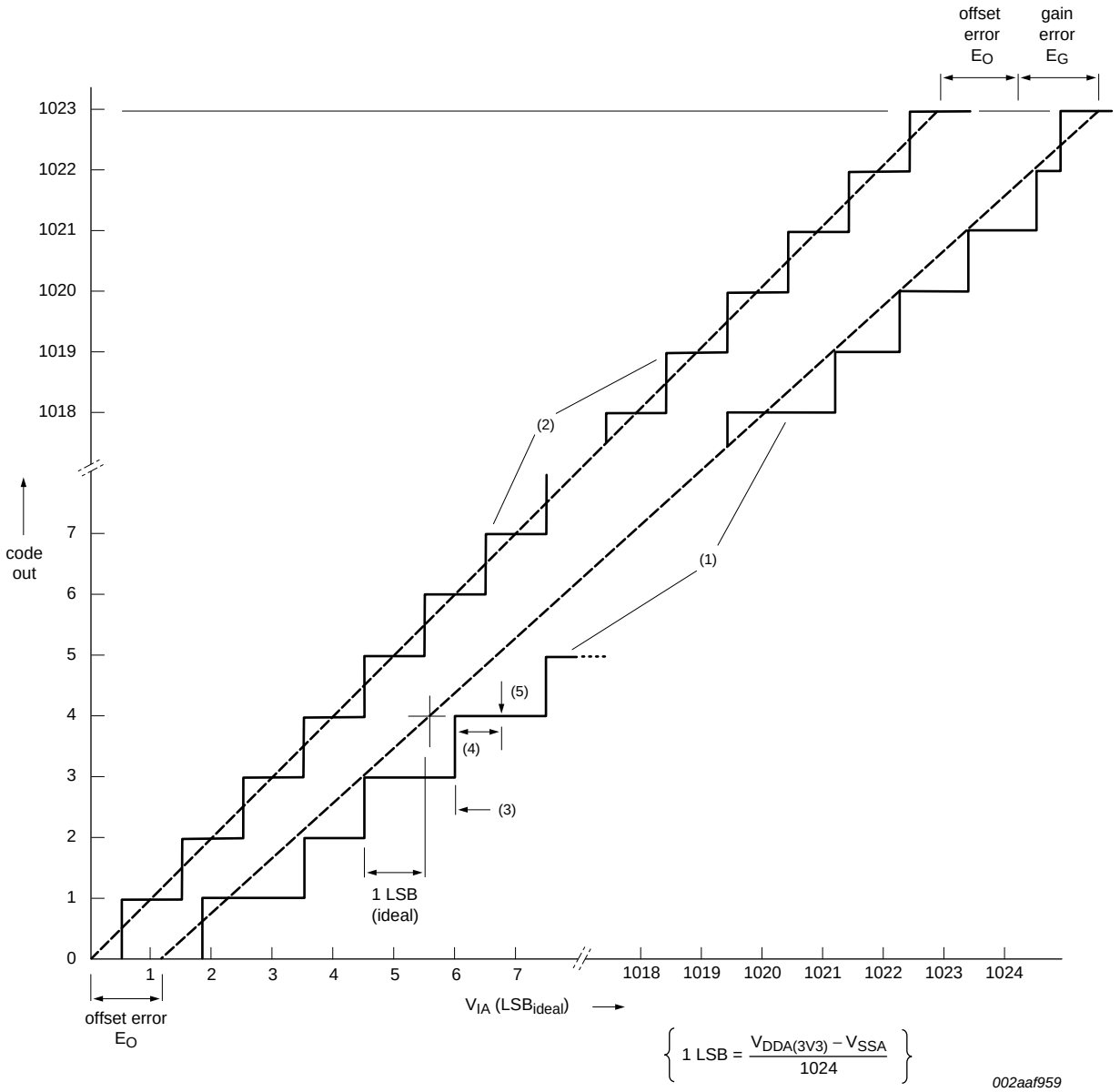

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 39. 10-bit ADC characteristics

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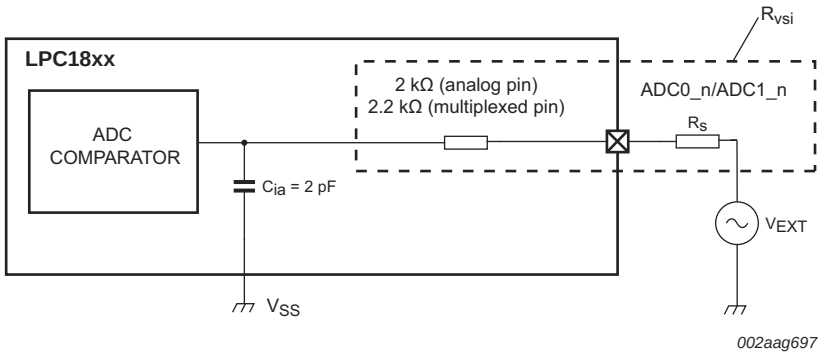

$R_s < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 40. ADC interface to pins

Table 38. DAC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±1.0	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.3	-	%
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[2]		0.4		μS

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC18xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

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13. Application information

13.1 LCD panel signal usage

Table 39. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:8]	-	-	-	-	-	-
LCD_VD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 40. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:16]	-	-	-	-	-	-
LCD_VD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCD_VD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCD_VD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCD_VD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCD_VD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCD_VD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCD_VD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCD_VD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCD_VD7	-	-		UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]

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Table 41. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD0	-	-	-	-	-	-	P4_1	RED0
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB /LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC18xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode, couple the input clock signal with a capacitor of 100 pF (C_C in Figure 41), with an amplitude of at least 200 mV (RMS). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 42, and in Table 42 and Table 43. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (L, C_L and R_S represent the fundamental frequency). Capacitance C_P in Figure 42 represents the parallel package capacitance and must not be larger than 7 pF. Parameters F_C, C_L, R_S and C_P are supplied by the crystal manufacturer.

Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF

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Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 43. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

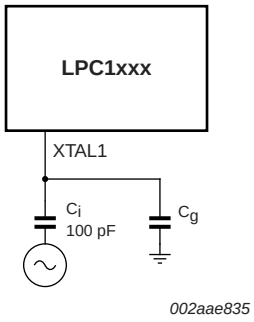

Fig 41. Slave mode operation of the on-chip oscillator

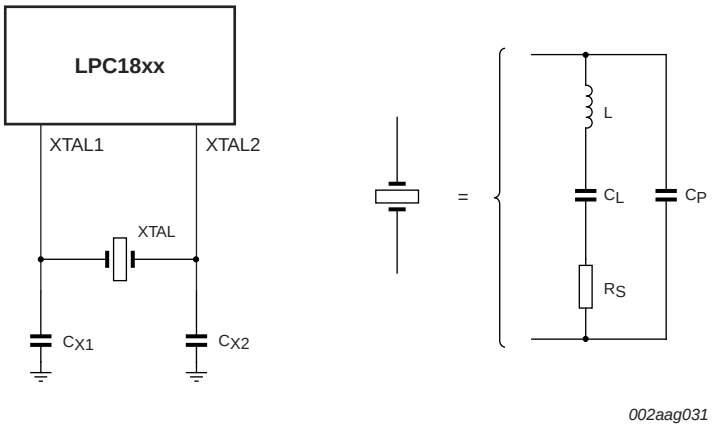

Fig 42. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation

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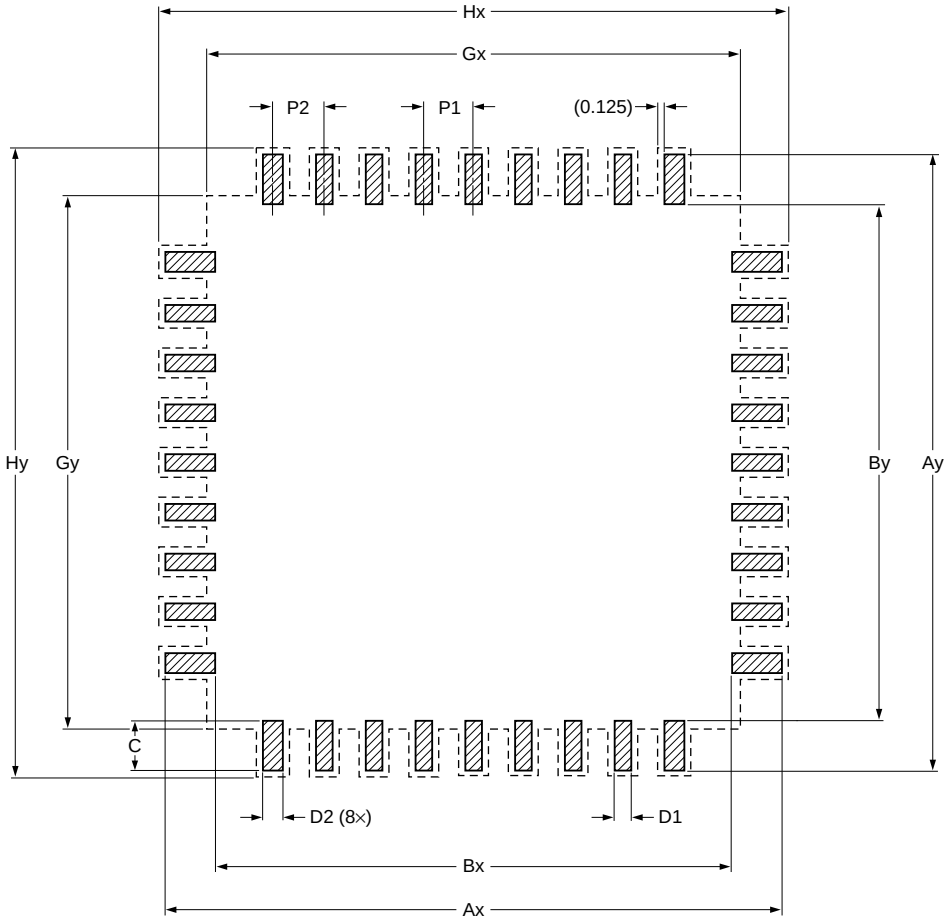
Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 56. Reflow soldering for the LQFP144 package

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Table 45. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Minimum operating voltage changed from 2.2 V to 2.4 V for $V_{DD(REG)(3V3)}$, $V_{DD(IO)}$, $V_{DDA(3V3)}$, V_{BAT} in Table 11. • Updated Dynamic characteristics: SSP pins in SPI mode. See Table 27. • Updated Dynamic characteristics: SD/MMC. See Table 34. • SPIFI timing data restated for CL = 20 pF in Table 36 “Dynamic characteristics: SPIFI”. • SPIFI timing diagram corrected and specified for mode 0. See Table 36 and Figure 38. • Table 23 “Dynamic characteristic: I/O pins[1]” added. • Parameter CI corrected for high-drive pins (changed from 2 pF to 5.2 pF). See Table 11. • Internal pull-up resistor configuration added for $\overline{\text{RESET}}$, WAKEUPn, and ALARM pins. See Table 3. • Description of DEBUG pin updated. • Input range for PLL1 corrected: 1 MHz to 25 MHz. See Section 7.20.7 “System PLL1”. • Signal polarity corrected for pins EMC_CKEOUT and EMC_DQMOUT. Both signals are active HIGH. • Updated USART timing figure. See Figure 29 “USART timing”. • Updated USART Dynamic characteristics table. See Table 26. • USB0_VBUS changed to input only. See Table 3 “Pin description” • SPIFI output timing parameters in Table 36 corrected to apply to Mode 0: – $t_{v(Q)}$ changed to 3.2 ns. – $t_{h(Q)}$ changed to 0.6 ns, • Parameter t_{CSLWEL} with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 28 “Dynamic characteristics: Static asynchronous external memory interface”. • Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 28 “Dynamic characteristics: Static asynchronous external memory interface”. • Removed restriction on C_CAN bus usage. See CAN.1 errata in Ref. 2. • Updated Figure 30, SSP master timing in SPI mode and Figure 31, SSP slave timing in SPI mode. • Changed the flash erase time (t_{er}) to 100ms. See Table 15. • Updated Dynamic characteristics: USB0 and USB1 pins (full-speed). See Table 31. • Updated Dynamic characteristics: SD/MMC table. See Table 34. • Updated Table 2: Motor control PWM instead of PWM. • Added a remark to Table 31. • Updated Table 13 “BOD static characteristics[1]”. Removed BOD interrupt levels 0 and 1; removed Reset levels 0 and 1. They are not applicable.			
LPC185X_3X_2X_1X v.4.1	<tbd>	Product data sheet	-	LPC185X_3X_2X_1X v.4

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