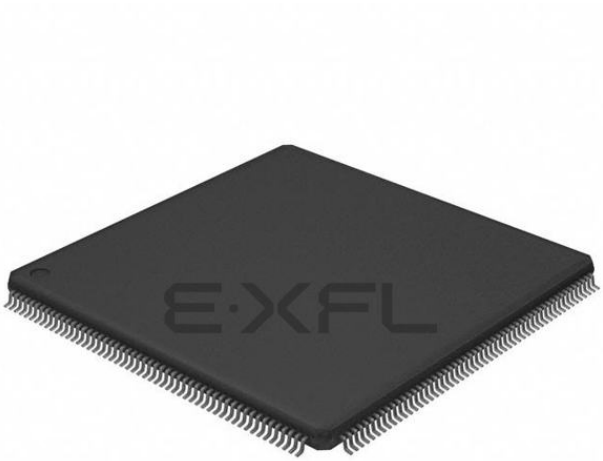

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	142
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1853jbd208e

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P5_3	T8	-	54	76	[2]	N; PU	I/O	**GPIO2[12] —** General purpose digital input/output pin.
							I	**MCI0 —** Motor control PWM channel 0, input.
							I/O	**EMC_D15 —** External memory data line 15.
							-	**R —** Function reserved.
							I	**U1_RI —** Ring Indicator input for UART1.
							I	**T1_CAP3 —** Capture input 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_4	P9	-	57	80	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**T1_MAT0 —** Match output 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_5	P10	-	58	81	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							I/O	**EMC_D9 —** External memory data line 9.
							-	**R —** Function reserved.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							O	**T1_MAT1 —** Match output 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_6	T13	-	63	89	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I/O	**EMC_D10 —** External memory data line 10.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART1.
							O	**T1_MAT2 —** Match output 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P6_3	P15	-	79	113	[2]	N; PU	I/O	**GPIO3[2] —** General purpose digital input/output pin.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	**R —** Function reserved.
							O	**EMC_CS1 —** LOW active Chip Select 1 signal.
							-	**R —** Function reserved.
							I	**T2_CAP2 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_4	R16	F6	80	114	[2]	N; PU	I/O	**GPIO3[3] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**U0_TXD —** Transmitter output for USART0.
							O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_5	P16	F9	82	117	[2]	N; PU	I/O	**GPIO3[4] —** General purpose digital input/output pin.
							O	**CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1.
							I	**U0_RXD —** Receiver input for USART0.
							O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_6	L14	-	83	119	[2]	N; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
							O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
							-	**R —** Function reserved.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**T2_CAP3 —** Capture input 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P6_11	H12	C9	101	143	[2]	N; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT0 —** SDRAM clock enable 0.
							-	**R —** Function reserved.
							O	**T2_MAT3 —** Match output 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_12	G15	-	103	145	[2]	N; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_0	B16	-	110	158	[2]	N; PU	I/O	**GPIO3[8] —** General purpose digital input/output pin.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_LE —** Line end signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_1	C14	-	113	162	[2]	N; PU	I/O	**GPIO3[9] —** General purpose digital input/output pin.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**LCD_VD19 —** LCD data.
							O	**LCD_VD7 —** LCD data.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P7_5	A7	-	133	191	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	-	134	194	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_7	B6	-	140	201	[5]	N; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							AI	**ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PA_0	L12	-	-	126	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_RX_MCLK —** I^2S1 receive master clock.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
PA_1	J14	-	-	134	[3]	N; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_2	K15	-	-	136	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_3	H11	-	-	147	[3]	N; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
							I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PD_0	N2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
							-	**R —** Function reserved.
							I/O	**GPIO6[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_1	P1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[15] —** General purpose digital input/output pin.
							O	**SD_POW —** SD/MMC power monitor output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_2	R1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	**EMC_D16 —** External memory data line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[16] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_3	P4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_6 —** SCTimer/PWM output 7. Match output 2 of timer 1.
							I/O	**EMC_D17 —** External memory data line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PD_16	R14	-	-	104	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A16 —** External memory address line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[30] —** General purpose digital input/output pin.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
PE_0	P14	-	-	106	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A18 —** External memory address line 18.
							I/O	**GPIO7[0] —** General purpose digital input/output pin.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_1	N14	-	-	112	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A19 —** External memory address line 19.
							I/O	**GPIO7[1] —** General purpose digital input/output pin.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_2	M14	-	-	115	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
							I	**CAN0_RD —** CAN receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_A20 —** External memory address line 20.
							I/O	**GPIO7[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PE_11	D16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**EMC_D30 —** External memory data line 30.
							I/O	**GPIO7[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**EMC_D31 —** External memory data line 31.
							I/O	**GPIO7[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I^2C pad).
							O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**GPIO7[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_14	C15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_DYCS3 —** SDRAM chip select 3.
							I/O	**GPIO7[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

7.4 AHB multilayer matrix

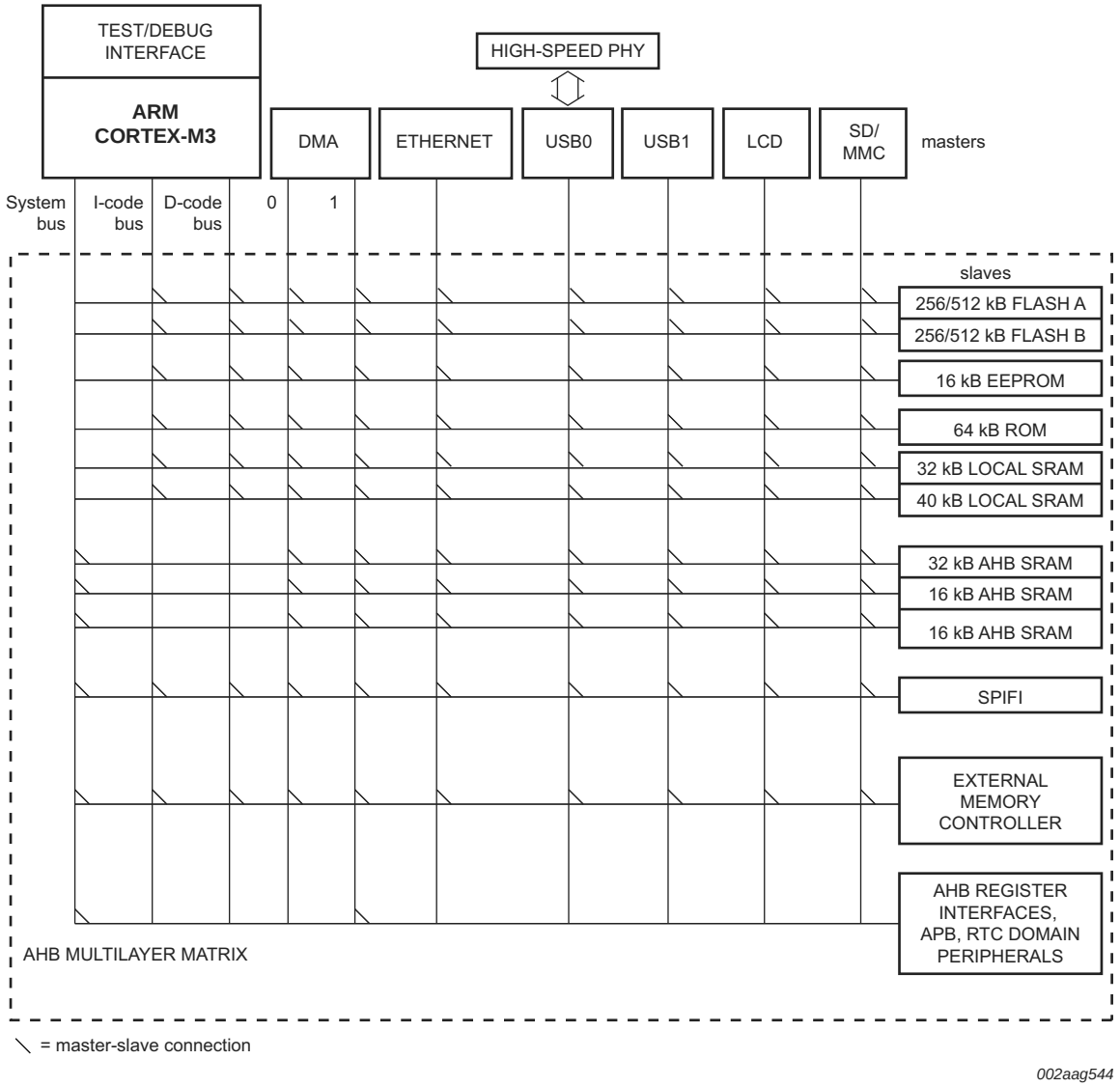


Fig 6. AHB multilayer matrix master and slave connections

7.5 Nested Vectored Interrupt Controller (NVIC)

The NVIC is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC185x/3x/2x/1x, the NVIC supports 53 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.

- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.6 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts.
- C_CAN0/1 and QEI interrupts.
- Ethernet, USB0, USB1 signals.
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3).

Remark: Any interrupt can wake up the ARM Cortex-M3 from sleep mode if enabled in the NVIC.

7.7 Global Input Multiplexer Array (GIMA)

The GIMA routes signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.

7.7.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.8 On-chip static RAM

The LPC185x/3x/2x/1x support up to 136 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.12 Memory mapping

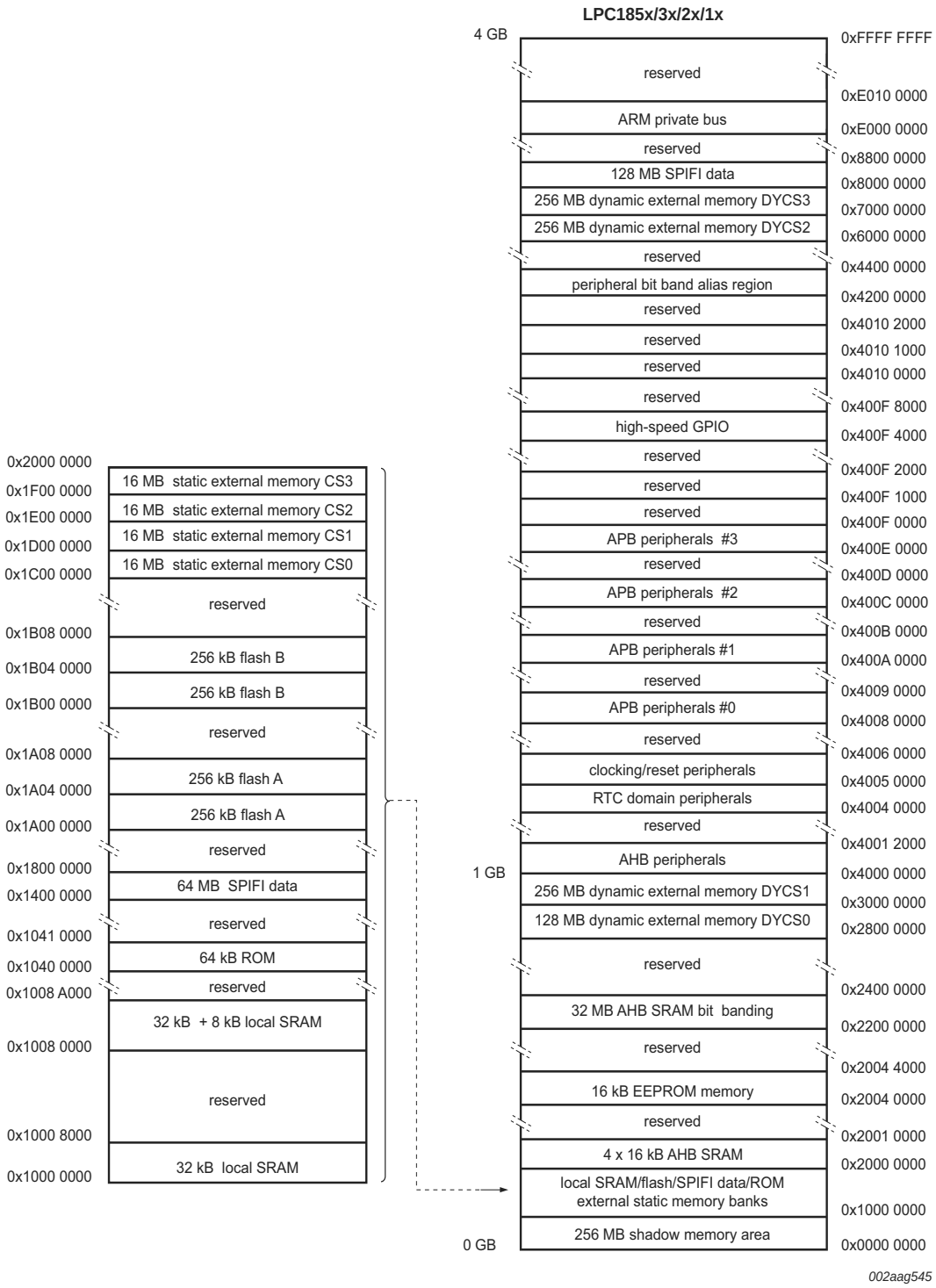


Fig 7. LPC185x/3x/2x/1x Memory mapping (overview)

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.
- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0. See Table 5.

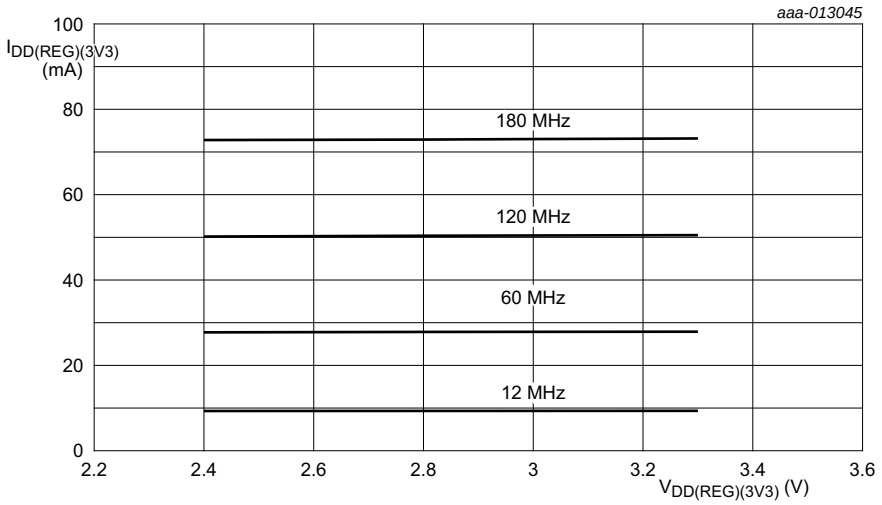
CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.21 Emulation and debugging

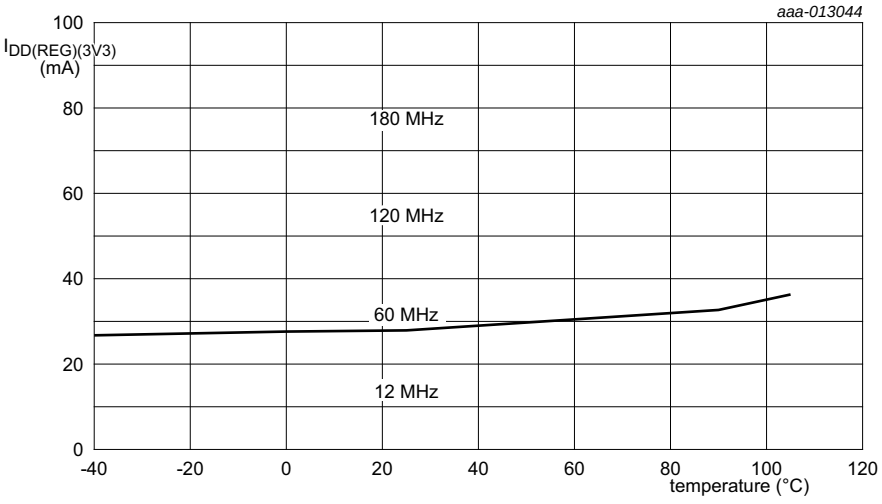
Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

10.1 Power consumption



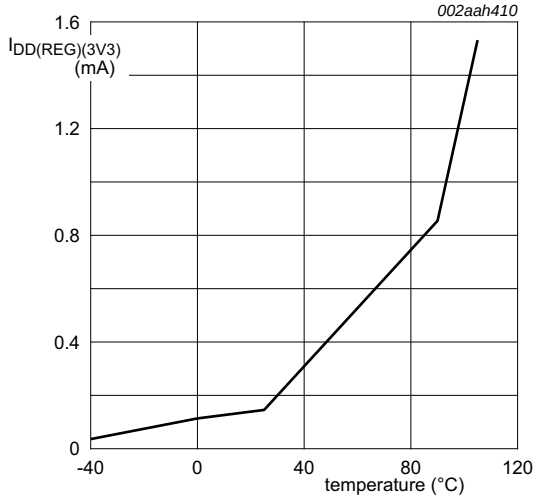
Conditions: T_{amb} = 25 °C; executing code while (1){} from SRAM; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 10. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode



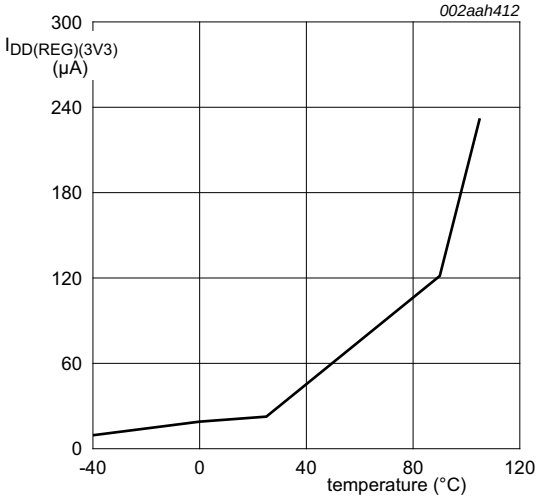
Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus temperature in active mode



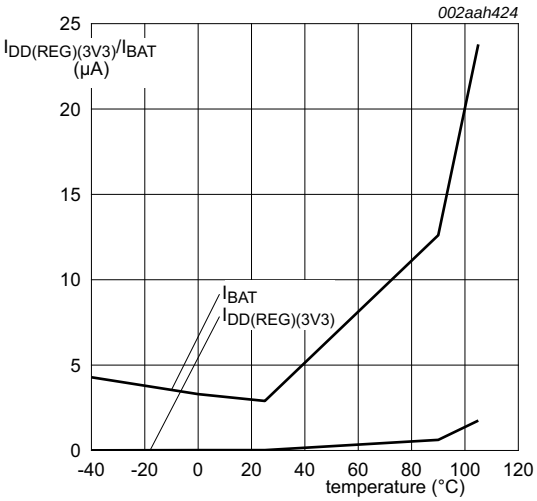
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 14. Typical supply current versus temperature in Deep-sleep mode



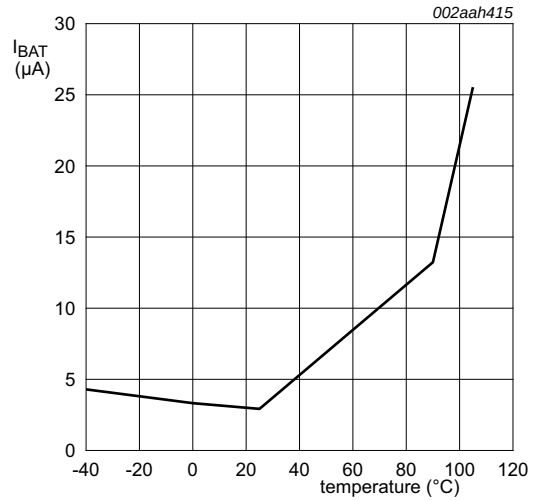
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 15. Typical supply current versus temperature in Power-down mode



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V. $V_{BAT} = V_{DD(REG)(3V3)} + 0.4$ V.

Fig 16. Typical supply current versus temperature in Deep power-down mode



Conditions: $V_{BAT} = 3.6$ V. $V_{DD(REG)(3V3)}$ not present.

Fig 17. Typical battery supply current versus temperature

11.7 GPCLKIN

Table 22. Dynamic characteristic: GPCLKIN

T_{amb} = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Min	Typ	Max	Unit
GP_CLKIN	input frequency	-	-	25	MHz

11.8 I/O pins

Table 23. Dynamic characteristic: I/O pins[1]

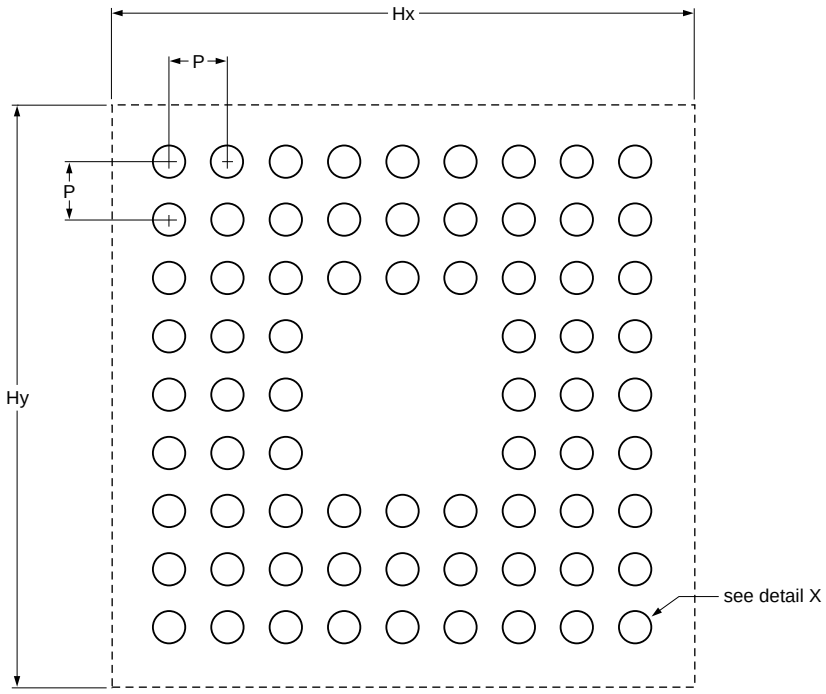
T_{amb} = −40 °C to +105 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; EHS = 1	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.3	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high drive strength							
t_r	rise time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.3	-	7.9	ns
t_f	fall time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.7	-	8.7	ns
t_r	rise time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.7	ns
t_f	fall time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.5	ns
t_r	rise time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.9	-	4.9	ns
t_f	fall time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.5	-	3.9	ns
t_r	rise time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.8	-	4.7	ns
t_f	fall time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.4	-	3.4	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high-speed							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	350	-	670	ps
t_f	fall time	pin configured as output; EHS = 1	[2][3]	450	-	730	ps
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.0	-	1.9	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.0	-	2.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

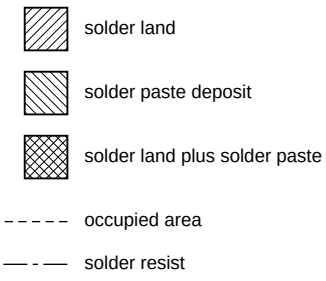
15. Soldering

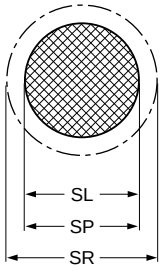
Footprint information for reflow soldering of LBGA256 package **SOT740-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

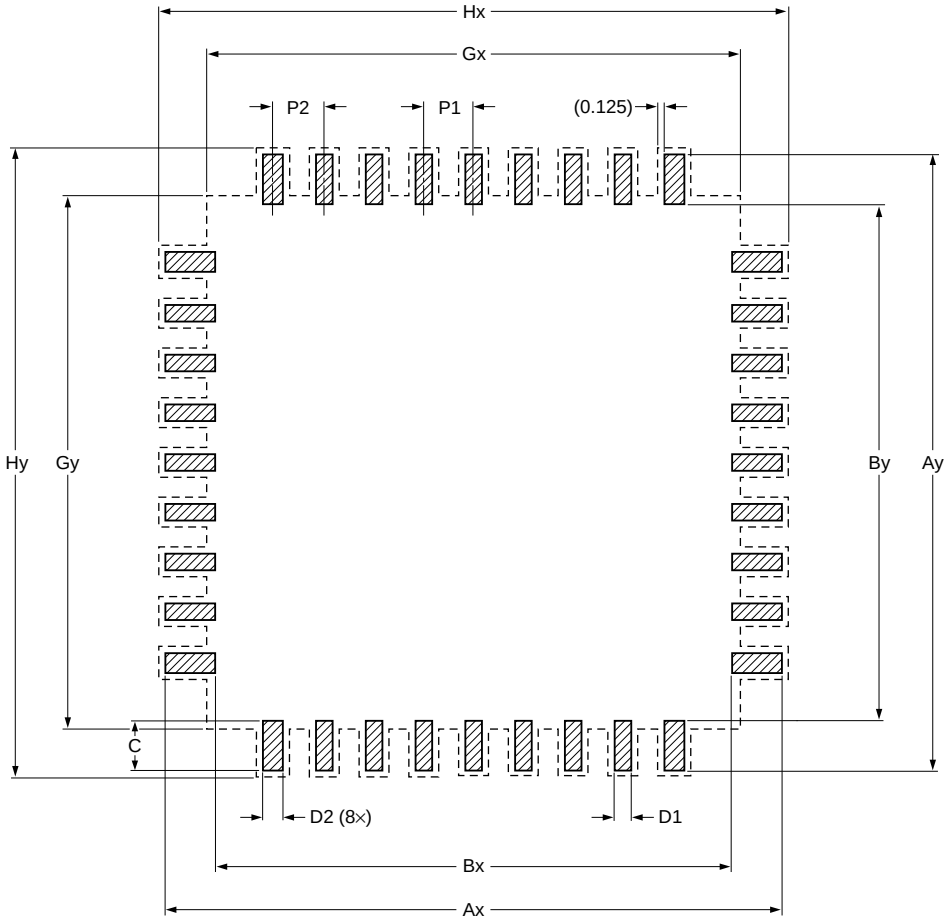
DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	17.500	17.500

sot740-2_fr

Fig 53. Reflow soldering for the LBGA256 package

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

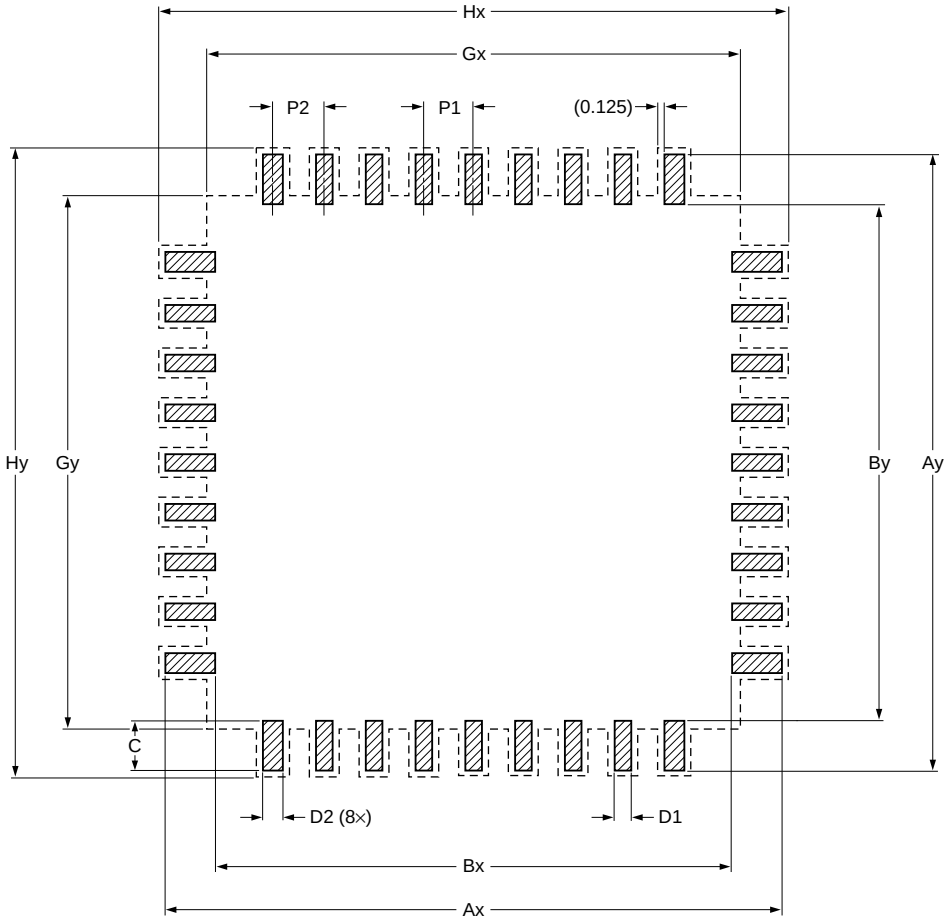
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 55. Reflow soldering for the LQFP208 package

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 56. Reflow soldering for the LQFP144 package

18. Revision history

Table 45. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC185X_3X_2X_1X v.5.2	20160308	Product data sheet	-	LPC185X_3X_2X_1X v.5.1
Modifications:	• Updated Table 29 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”.			
LPC185X_3X_2X_1X v.5.1	20151117	Product data sheet	2015110041	LPC185X_3X_2X_1X v.5
Modifications:	• Updated Table 2 “Ordering options”; TFBGA100 packages do not support ULPI interface. • Updated SSP slave and SSP master values in Table 27 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$. – removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode. – added units to t_d, delay time, for SSP slave and master mode. • Added GPCLKIN section and table. See Section 11.7 “GPCLKIN” and Table 22 “Dynamic characteristic: GPCLKIN”.			
LPC185X_3X_2X_1X v.5	20150429	Product data sheet	-	LPC185X_3X_2X_1X v.4.1

For more information, please visit: http://www.nxp.com
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Date of release: 8 March 2016
Document identifier: LPC185X_3X_2X_1X