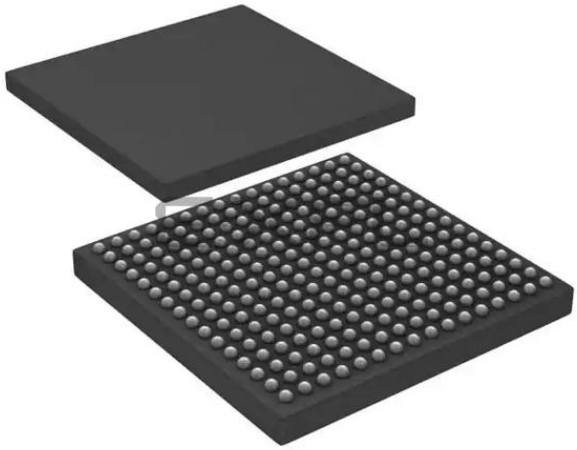

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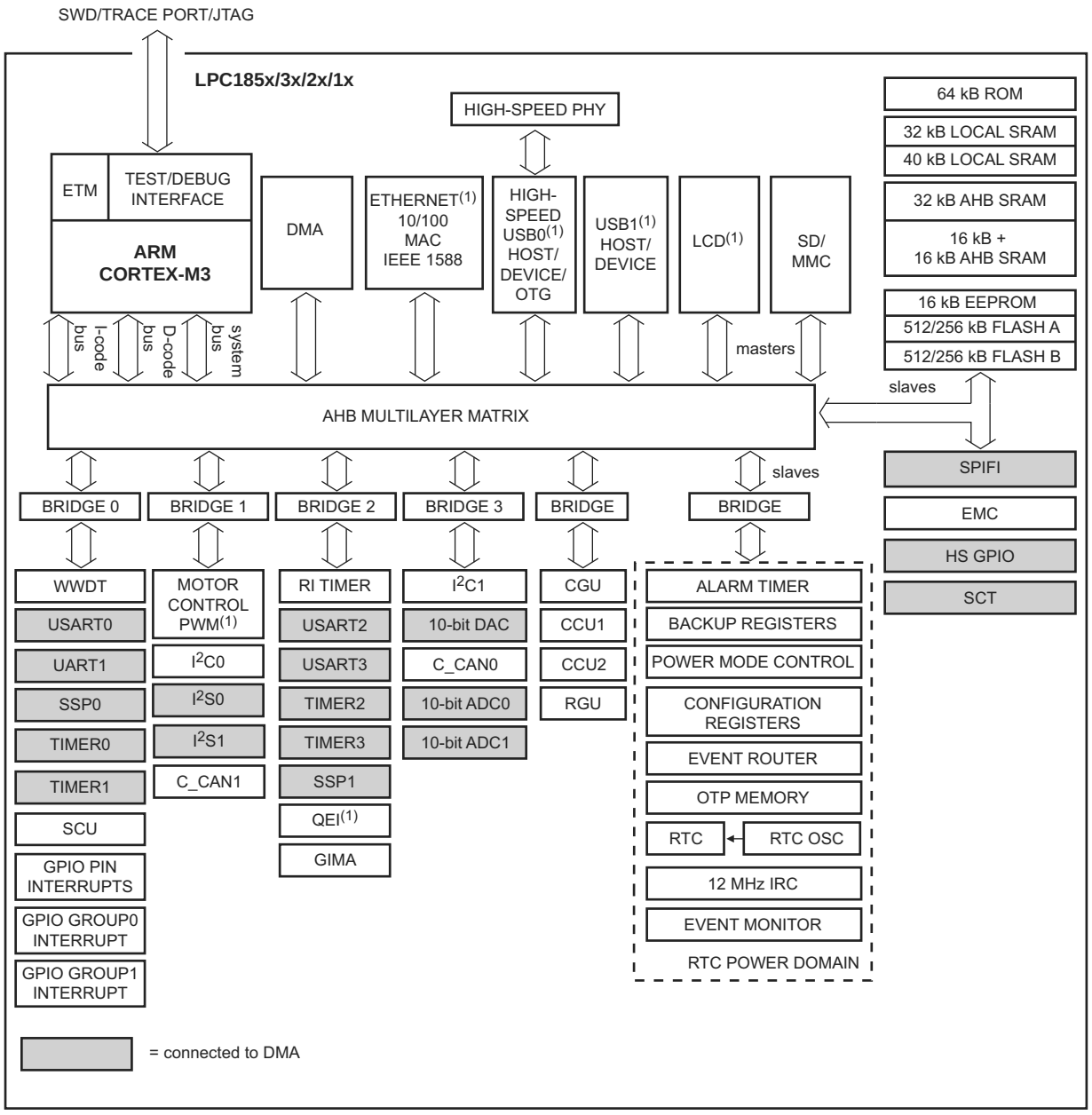
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	164
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1853jet256-551

5. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. LPC185x/3x/2x/1x block diagram

0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
Multiplexed digital pins								
P0_0	L3	G2	32	47	[2]	N; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P0_1	M2	G1	34	50	[2]	N; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**I2S1_TX_SDA —** I^2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P1_0	P2	H1	38	54	[2]	N; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							I/O	**EMC_A5 —** External memory address line 5.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							I/O	**EMC_D12 —** External memory data line 12.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_3	C2	-	7	10	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							O	**LCD_VD2 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD21 —** LCD data.
							I/O	**U3_BAUD —** Baud pin for USART3.
							-	**R —** Function reserved.
							AI	**ADC0_0 —** ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	-	9	14	[5]	N; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**LCD_VD1 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD20 —** LCD data.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							-	**R —** Function reserved.
							AO	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	10	15	[2]	N; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_6	C1	-	11	17	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P4_7	H4	-	14	21	[2]	O; PU	O	**LCD_DCLK —** LCD panel clock.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P4_8	E2	-	15	23	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							O	**LCD_VD9 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[12] —** General purpose digital input/output pin.
							O	**LCD_VD22 —** LCD data.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
P4_9	L2	-	33	48	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD11 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[13] —** General purpose digital input/output pin.
							O	**LCD_VD15 —** LCD data.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P7_2	A16	-	115	165	[2]	N; PU	I/O	**GPIO3[10] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							I/O	**I2S0_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							O	**LCD_VD18 —** LCD data.
							O	**LCD_VD6 —** LCD data.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
P7_3	C13	-	117	167	[2]	N; PU	I/O	**GPIO3[11] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							-	**R —** Function reserved.
							O	**LCD_VD17 —** LCD data.
							O	**LCD_VD5 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_4	C8	-	132	189	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD16 —** LCD data.
							O	**LCD_VD4 —** LCD data.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PA_0	L12	-	-	126	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_RX_MCLK —** I^2S1 receive master clock.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
PA_1	J14	-	-	134	[3]	N; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_2	K15	-	-	136	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_3	H11	-	-	147	[3]	N; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
							I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PD_8	P8	-	-	74	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							I/O	**EMC_D22 —** External memory data line 22.
							-	**R —** Function reserved.
							I/O	**GPIO6[22] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_9	T11	-	-	84	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D23 —** External memory data line 23.
							-	**R —** Function reserved.
							I/O	**GPIO6[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_10	P11	-	-	86	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							O	**$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
							-	**R —** Function reserved.
							I/O	**GPIO6[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_11	N9	-	-	88	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS3}}$ —** LOW active Chip Select 3 signal.
							-	**R —** Function reserved.
							I/O	**GPIO6[25] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PE_7	F15	-	-	149	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**EMC_D26 —** External memory data line 26.
							I/O	**GPIO7[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_8	F14	-	-	150	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							I	**U1_DSR —** Data Set Ready input for UART1.
							I/O	**EMC_D27 —** External memory data line 27.
							I/O	**GPIO7[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_9	E16	-	-	152	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							I/O	**EMC_D28 —** External memory data line 28.
							I/O	**GPIO7[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_10	E14	-	-	154	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**EMC_D29 —** External memory data line 29.
							I/O	**GPIO7[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC185x/3x/2x/1x use a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals. Flexible connections allow different bus masters to access peripherals that are on different slave ports of the matrix simultaneously.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and low-power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual.

7.3 System Tick timer (SysTick)

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.13 One-Time Programmable (OTP) memory

The OTP provides 64 bit+ 256 bit of memory for general-purpose use.

7.14 General-Purpose I/O (GPIO)

The LPC185x/3x/2x/1x provides 8 GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.14.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Two GPIO group interrupts can be triggered by any pin or pins in each port.

7.15 AHB peripherals

7.15.1 State Configurable Timer/PWM (SCTimer/PWM) subsystem

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

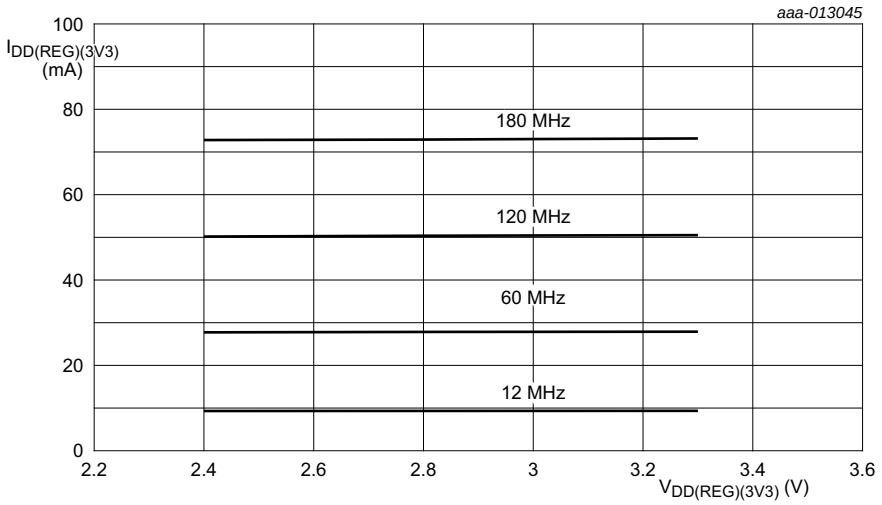
10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

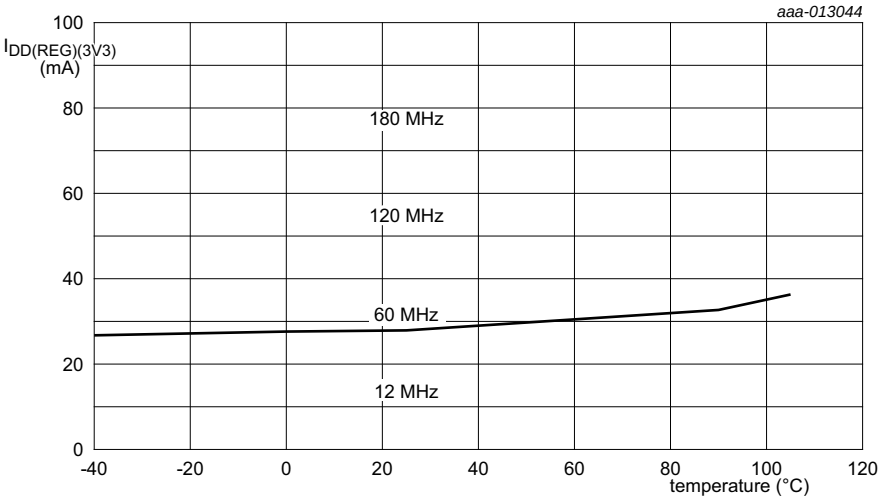
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_ DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	all peripherals disabled					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-	-	0.1	µA
I_{BAT}	battery supply current	Deep power-down mode; RTC running; $V_{DD(REG)(3V3)}$ floating; V_{BAT} = 3.3 V		-	3.0	-	µA
		$V_{DD(REG)(3V3)}$ = V_{BAT} = 3.3 V		-	1.5	-	µA

10.1 Power consumption



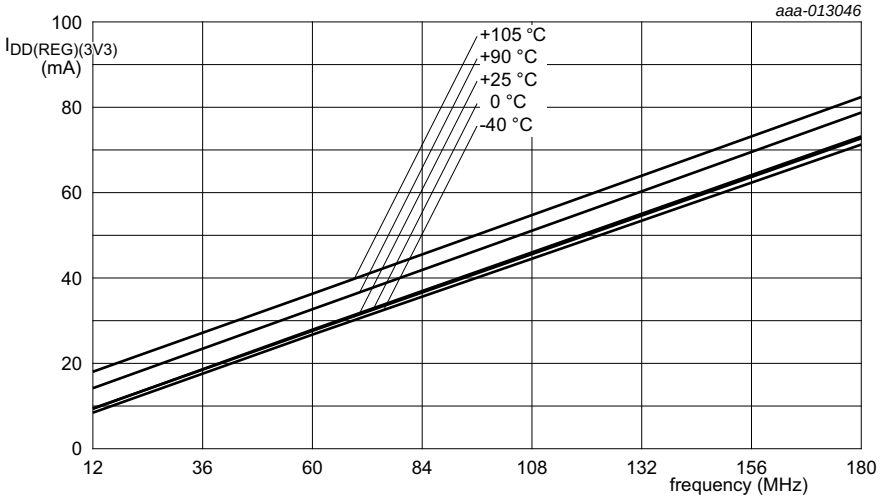
Conditions: T_{amb} = 25 °C; executing code while (1){} from SRAM; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 10. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode



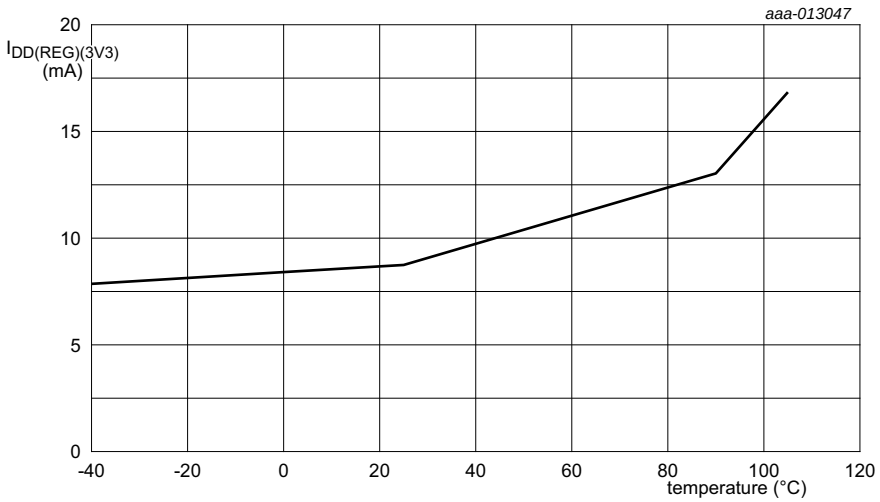
Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus temperature in active mode



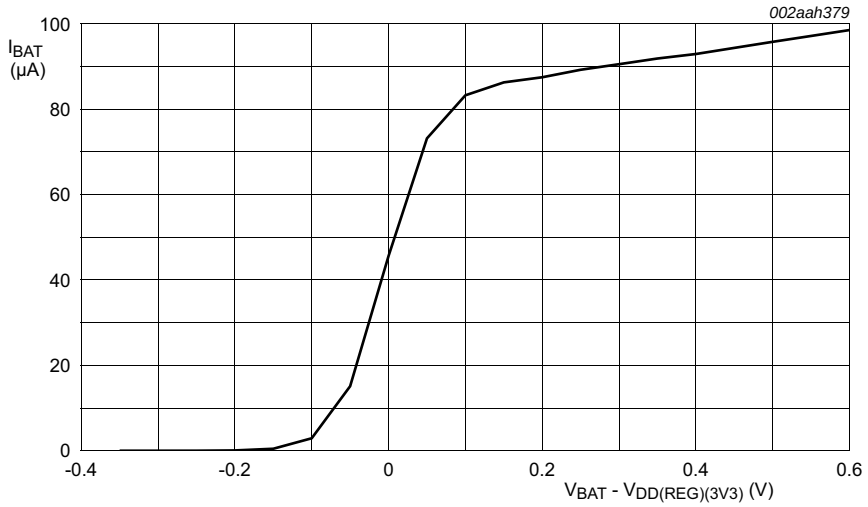
Conditions: active mode entered executing code while (1){} from SRAM; $V_{DD(REG)(3V3)}$ = 3.3 V; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 12. Typical supply current versus core frequency in active mode; code executed from SRAM



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; internal pull-up resistors disabled; system PLL disabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled. CCLK = 12 MHz.

Fig 13. Typical supply current versus temperature in sleep mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 2.6 V to 3.6 V; CCLK = 12 MHz.

Remark: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V.

Fig 18. Typical battery supply current in Active mode

10.2 Peripheral power consumption

The typical power consumption at T = 25 °C for each individual peripheral is measured as follows:

1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

Table 12. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
I2C1	CLK_APB3_I2C1	0.01	0.01
I2C0	CLK_APB1_I2C0	< 0.01	0.02
DAC	CLK_APB3_DAC	0.01	0.02
ADC0	CLK_APB3_ADC0	0.07	0.07
ADC1	CLK_APB3_ADC1	0.07	0.07
CAN0	CLK_APB3_CAN0	0.17	0.17
CAN1	CLK_APB1_CAN1	0.16	0.15
MOTOCON	CLK_APB1_MOTOCON	0.04	0.04
I2S	CLK_APB1_I2S	0.09	0.08
SPIFI	CLK_SPIFI, CLK_M3_SPIFI	1.14	2.29
GPIO	CLK_M3_GPIO	0.72	1.43

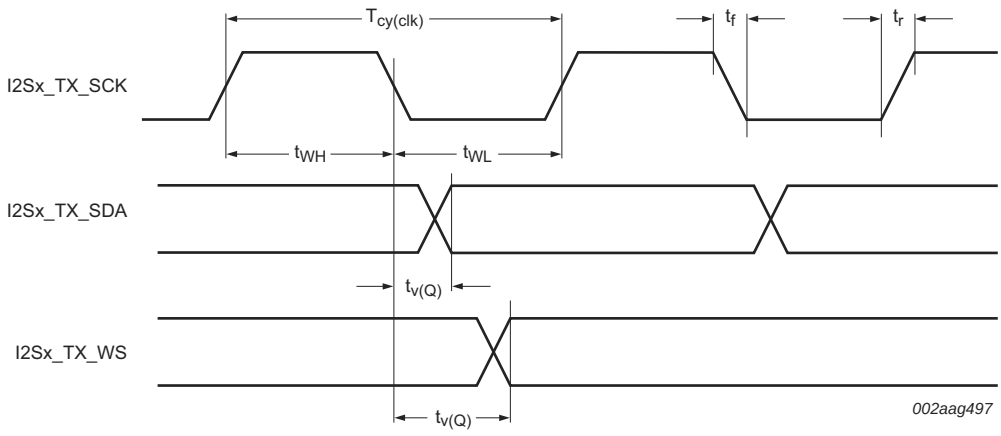


Fig 27. I²S-bus timing (transmit)

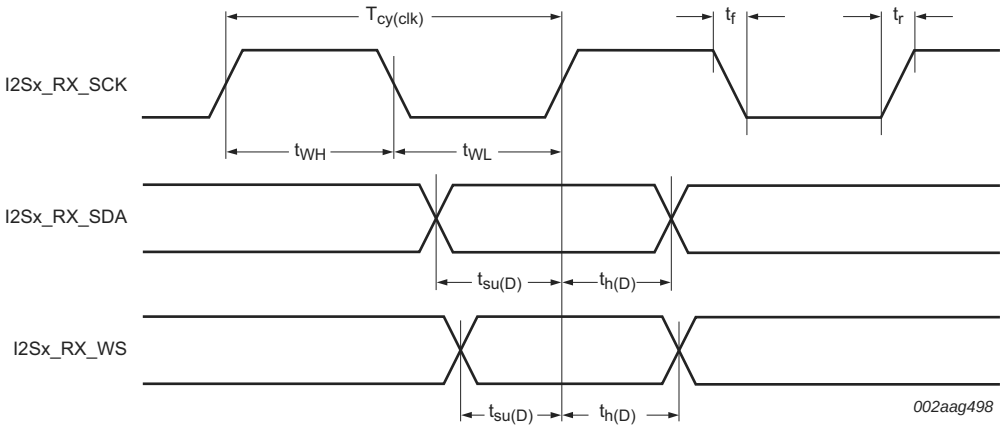


Fig 28. I²S-bus timing (receive)

11.11 USART interface

Table 26. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	26.6	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	0	10.4	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	2.4	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	4.3	24.3	ns

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		0.5 x $T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		0.5 × $T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$ + 1.5	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$ + 1.5	-	-	ns
		microwire frame format		0.5 × $T_{cy(clk)}$	-	-	ns
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

11.15 Ethernet

Table 33. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to +105 °C, 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

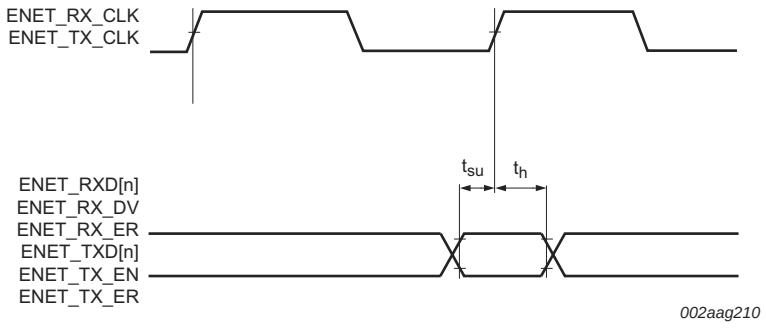


Fig 36. Ethernet timing

11.16 SD/MMC

Table 34. Dynamic characteristics: SD/MMC

T_{amb} = −40 °C to +105 °C, 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. Simulated values. SAMPLE_DELAY = 0x9, DRV_DELAY = 0x6 in the SDDELAY register sampled at 90 % and 10 % of the signal level, EHS = 1 for SD_CLK pin, EHS = 0 for SD_DATn and SD_CMD pins. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	5.2	-	ns
		on pins SD_CMD as inputs	7	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0.2	-	ns
		on pins SD_CMD as inputs	−1	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_DATn as outputs	-	15.7	ns
		on pins SD_CMD as outputs	-	15.9	ns
$t_{h(Q)}$	data output hold time	on pins SD_DATn as outputs	3.5	-	ns
		on pins SD_CMD as outputs	3.5	-	ns

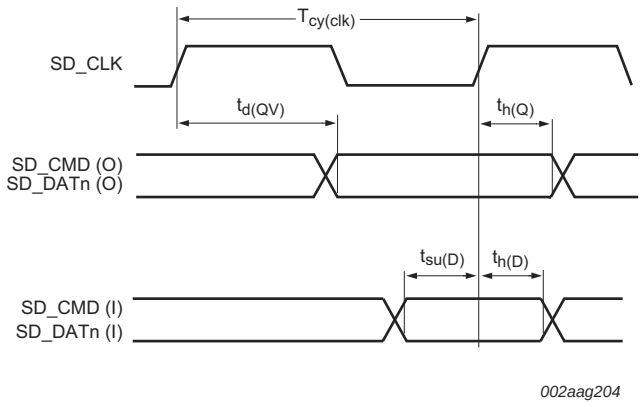


Fig 37. SD/MMC timing

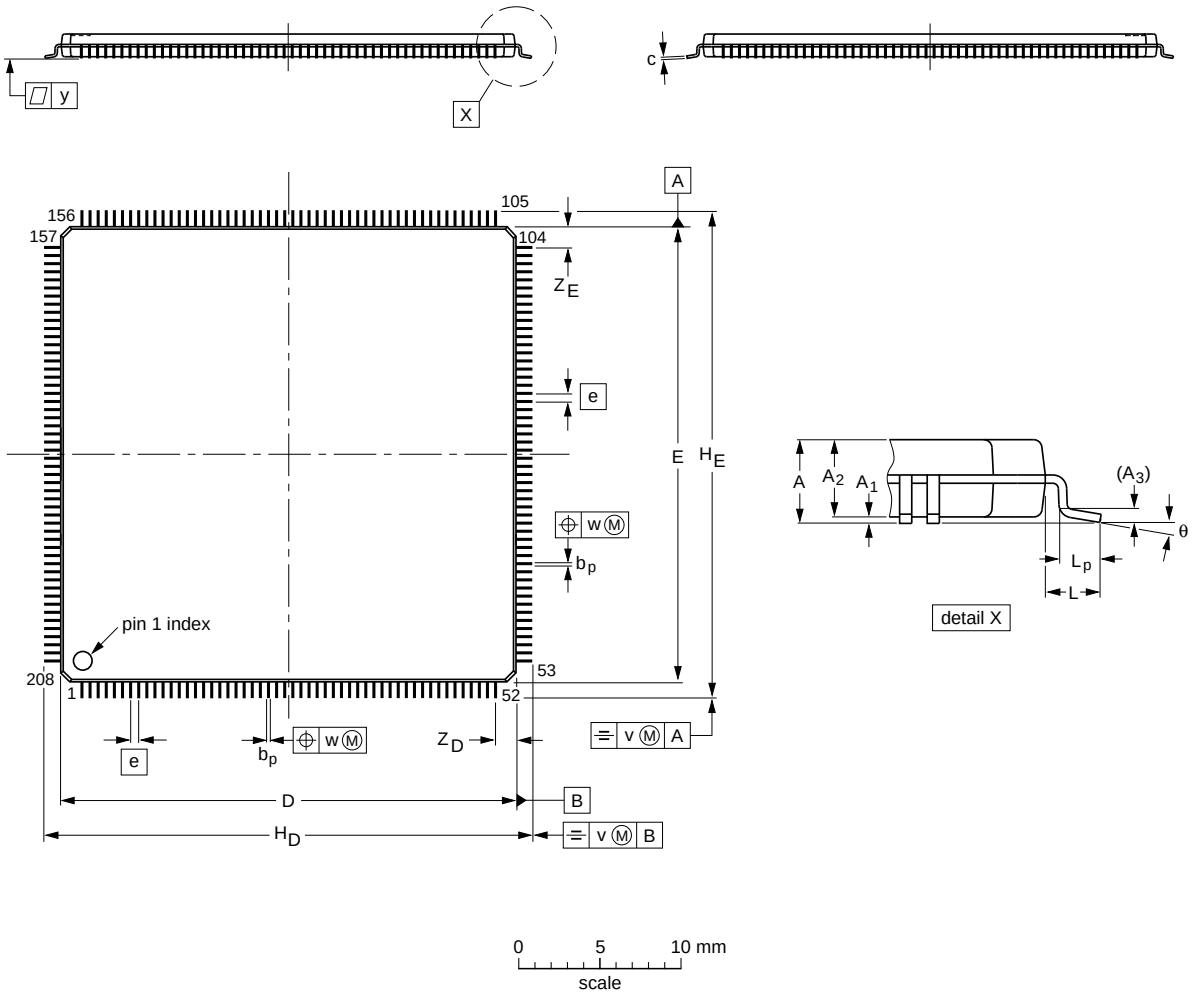
11.17 LCD

Table 35. Dynamic characteristics: LCD

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time		-	-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-	-	ns

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 51. Package outline of the LQFP208 package

Table 45. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1857_53 v.3.1	20120904	Preliminary data sheet	-	LPC1857_53 v.3
Modifications:	• SSP0 boot pin functions added in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • Peripheral power consumption data added in Table 12. • BOD de-assertion levels add in Table 13. • Minimum value for all supply voltages changed to -0.5 V n Table 7.			
LPC1857_53 v.3	20120711	Preliminary data sheet	-	LPC1857_53 v.2
Modifications:	• Data sheet status changed to preliminary. • AES removed. Available on parts LPC18Sxx only. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”, “USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Dynamic characteristics of the SD/MMC controller updated in Table 29. • Dynamic characteristics of the LCD controller updated in Table 30. • Dynamic characteristics of the SSP controller updated in Table 22. • Section 10.2 added. • Table 8 “Thermal resistance value (BGA packages)” added. • Description of pins USB1_DP and USB1_DM updated in Table 3. • Editorial updates. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 9.			
LPC1857_53 v.2	20120515	Objective data sheet	-	LPC1857_53 v.1
LPC1857_53 v.1	20111214	Objective data sheet	-	-