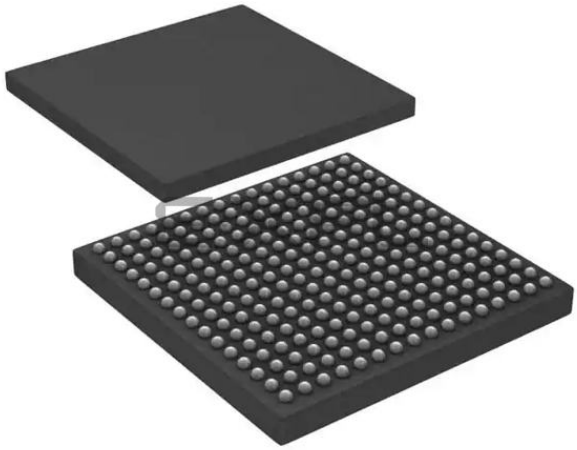

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	164
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1857jet256-551

- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 3 % accuracy over temperature and voltage (1.5 % accuracy for T_{amb} = 0 °C to 85 °C).
- Ultra-low power RTC crystal oscillator.
- Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL can be used with the High-speed USB, the third PLL can be used as audio PLL.
- Clock output.

- Configurable digital peripherals:
  - State Configurable Timer/PWM (SCTimer/PWM) subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces:
  - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to an external high-speed PHY (USB1).
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Up to two C_CAN 2.0B controllers with one channel each.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
  - One standard I^2C-bus interface with monitor mode and standard I/O pins.
  - Two I^2S interfaces with DMA support, each with one input and one output.
- Digital peripherals:
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024H × 768V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - SD/MMC card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_10	M3	-	35	51	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	**LCD_VD10 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[14] —** General purpose digital input/output pin.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_0	N3	-	37	53	[2]	N; PU	I/O	**GPIO2[9] —** General purpose digital input/output pin.
							O	**MCOB2 —** Motor control PWM channel 2, output B.
							I/O	**EMC_D12 —** External memory data line 12.
							-	**R —** Function reserved.
							I	**U1_DSR —** Data Set Ready input for UART1.
							I	**T1_CAP0 —** Capture input 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_1	P3	-	39	55	[2]	N; PU	I/O	**GPIO2[10] —** General purpose digital input/output pin.
							I	**MCI2 —** Motor control PWM channel 2, input.
							I/O	**EMC_D13 —** External memory data line 13.
							-	**R —** Function reserved.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	**T1_CAP1 —** Capture input 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_2	R4	-	46	63	[2]	N; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
							I	**MCI1 —** Motor control PWM channel 1, input.
							I/O	**EMC_D14 —** External memory data line 14.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	**T1_CAP2 —** Capture input 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P7_5	A7	-	133	191	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	-	134	194	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_7	B6	-	140	201	[5]	N; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							AI	**ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P9_3	M6	-	-	79	[2]	N; PU	I/O	**GPIO4[15] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							-	**R —** Function reserved.
							O	**U3_TXD —** Transmitter output for USART3.
P9_4	N10	-	-	92	[2]	N; PU	-	**R —** Function reserved.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							-	**R —** Function reserved.
							I/O	**GPIO5[17] —** General purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							-	**R —** Function reserved.
							I	**U3_RXD —** Receiver input for USART3.
P9_5	M9	-	69	98	[2]	N; PU	-	**R —** Function reserved.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							O	**USB1_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							I/O	**GPIO5[18] —** General purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
P9_6	L11	-	72	103	[2]	N; PU	I/O	**GPIO4[11] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I	**USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PC_7	G5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
							-	**R —** Function reserved.
							I	**ENET_RXD3 —** Ethernet receive data 3 (MII interface).
							I/O	**GPIO6[6] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
PC_8	N4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							-	**R —** Function reserved.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
							I/O	**GPIO6[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**SD_CD —** SD/MMC card detect input.
PC_9	K2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
							-	**R —** Function reserved.
							I	**ENET_RX_ER —** Ethernet receive error (MII interface).
							I/O	**GPIO6[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**SD_POW —** SD/MMC power monitor output.
PC_10	M5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
							I	**U1_DSR —** Data Set Ready input for UART1.
							-	**R —** Function reserved.
							I/O	**GPIO6[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							I/O	**SD_CMD —** SD/MMC command signal.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PC_11	L5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULP data line direction.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							-	**R —** Function reserved.
							I/O	**GPIO6[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							I/O	**GPIO6[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**GPIO6[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**GPIO6[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_DAT7 —** SD/MMC data bus line 7.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PE_7	F15	-	-	149	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**EMC_D26 —** External memory data line 26.
							I/O	**GPIO7[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_8	F14	-	-	150	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							I	**U1_DSR —** Data Set Ready input for UART1.
							I/O	**EMC_D27 —** External memory data line 27.
							I/O	**GPIO7[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_9	E16	-	-	152	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							I/O	**EMC_D28 —** External memory data line 28.
							I/O	**GPIO7[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_10	E14	-	-	154	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**EMC_D29 —** External memory data line 29.
							I/O	**GPIO7[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

7.12 Memory mapping

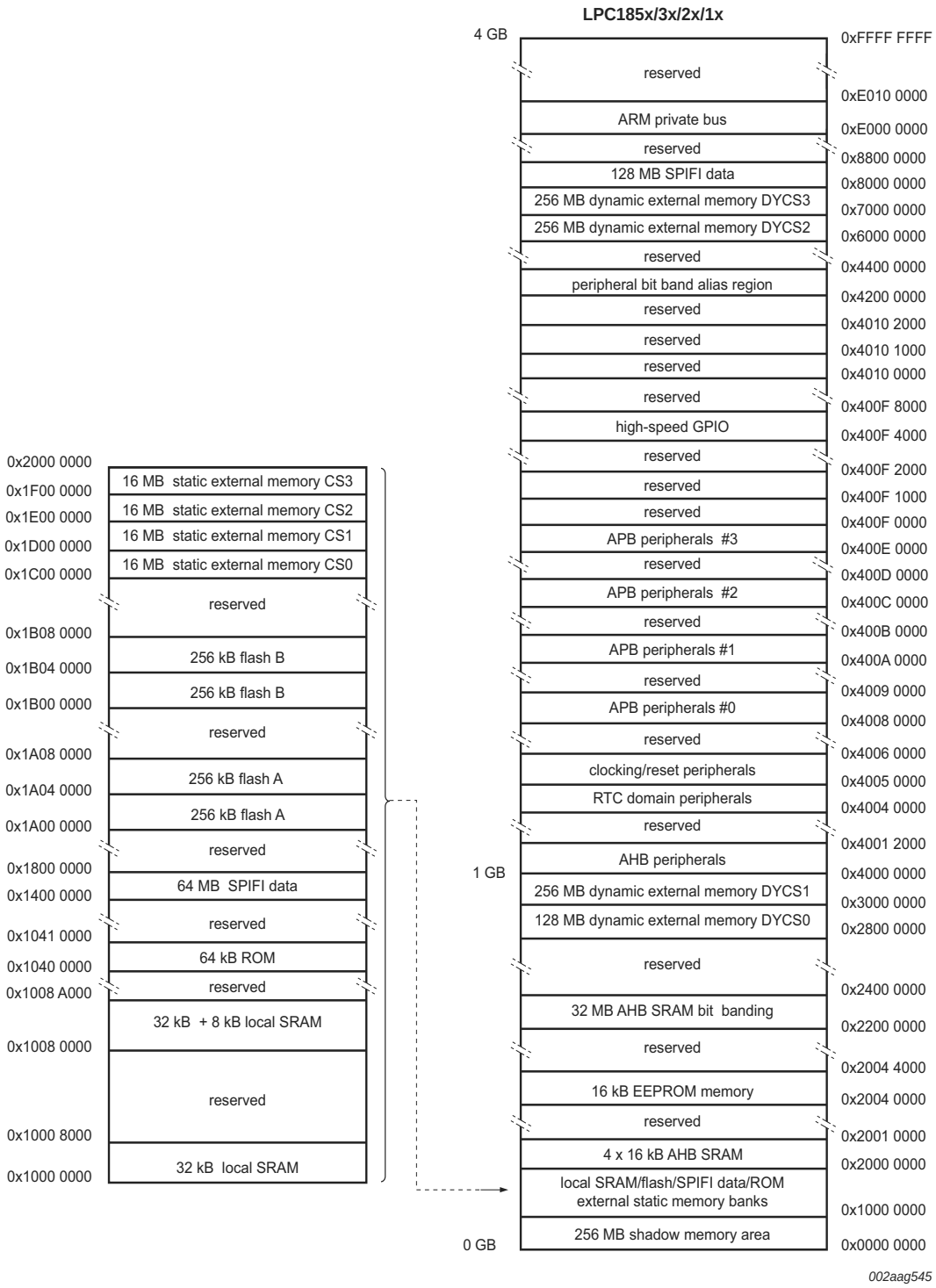


Fig 7. LPC185x/3x/2x/1x Memory mapping (overview)

transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.16.3.1 Features

- Maximum SSP speed in full-duplex mode of 25 Mbit/s; for transmit only 50 Mbit/s (master) and 15 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- Eight-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.
- Connected to the GPDMA.

7.16.4 I^2C-bus interface

Remark: The LPC185x/3x/2x/1x contain two I^2C-bus interfaces.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus interface is a multi-master bus and can be controlled by more than one bus master connected to it.

7.16.4.1 Features

- I^2C0 is a standard I^2C-bus compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- All I^2C-bus controllers support multiple address recognition and a bus monitor mode.

7.16.5 I^2S interface

Remark: The LPC185x/3x/2x/1x contain two I^2S interfaces.

7.17 Counter/timers and motor control

7.17.1 General purpose 32-bit timers/external event counter

Remark: The LPC185x/3x/2x/1x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.17.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.17.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.17.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.17.3.1 Features

- Tracks encoder position.

- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

7.19.2 Event monitor/recorder

The event monitor/recorder allows recording and creating a time stamp of events related to the WAKEUP pins. Sensors report changes to the state of the WAKEUP pins, and the event monitor/recorder stores records of such events. The event recorder can be powered by the backup battery.

The event monitor/recorder can monitor the integrity of the device and record any tampering events.

7.19.2.1 Features

- Supports three digital event inputs in the VBAT power domain.
- An event is defined as a level change at the digital event inputs.
- For each event channel, two timestamps mark the first and the last occurrence of an event. Each channel also has a dedicated counter tracking the total number of events. Timestamp values are taken from the RTC.
- Runs in VBAT power domain, independent of system power supply. The event/recorder/monitor can therefore operate in Deep power-down mode.
- Low power consumption.
- Interrupt available if system is running.
- A qualified event can be used as a wake-up trigger.
- State of event interrupts accessible by software through GPIO.

7.19.3 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt, if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

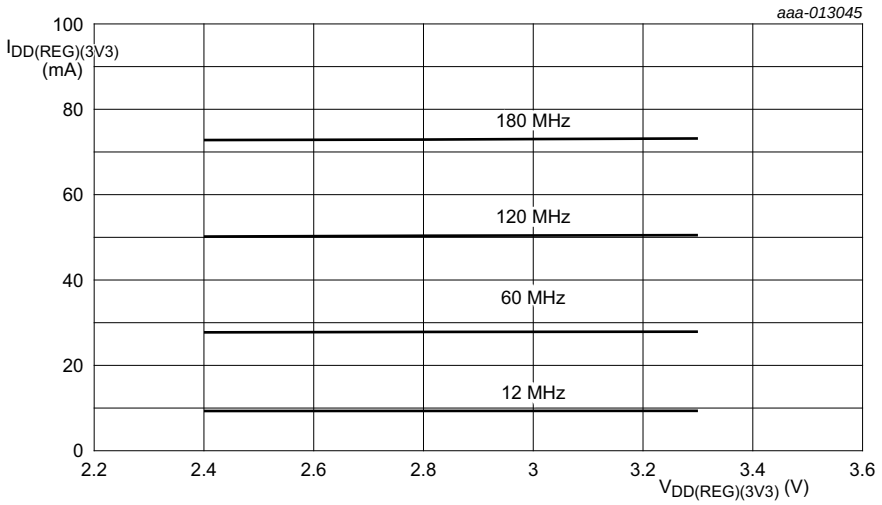
7.20 System control

7.20.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

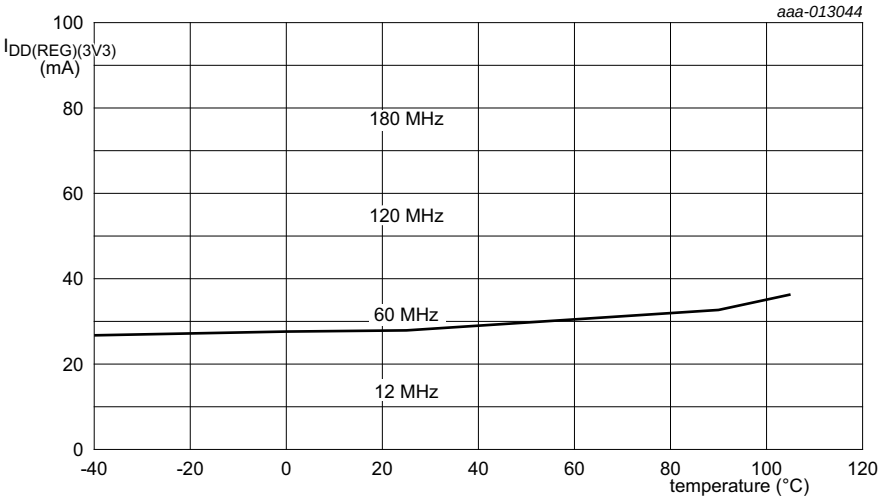
- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping

10.1 Power consumption



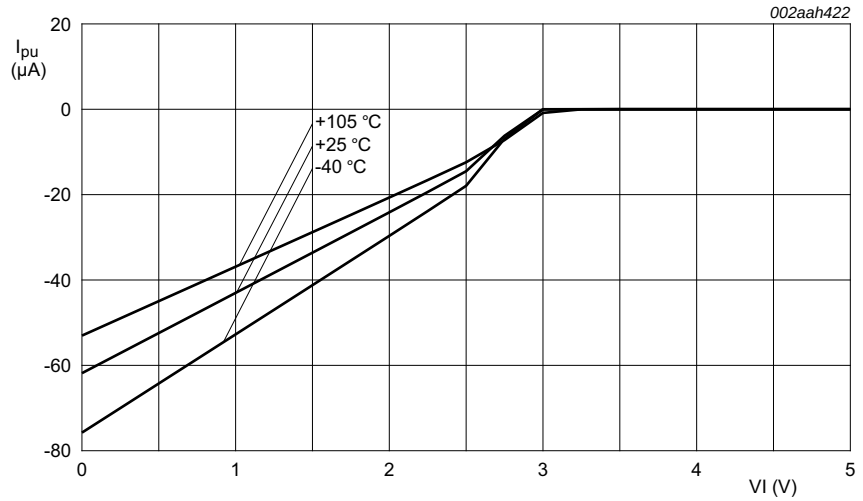
Conditions: T_{amb} = 25 °C; executing code while (1){} from SRAM; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 10. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode



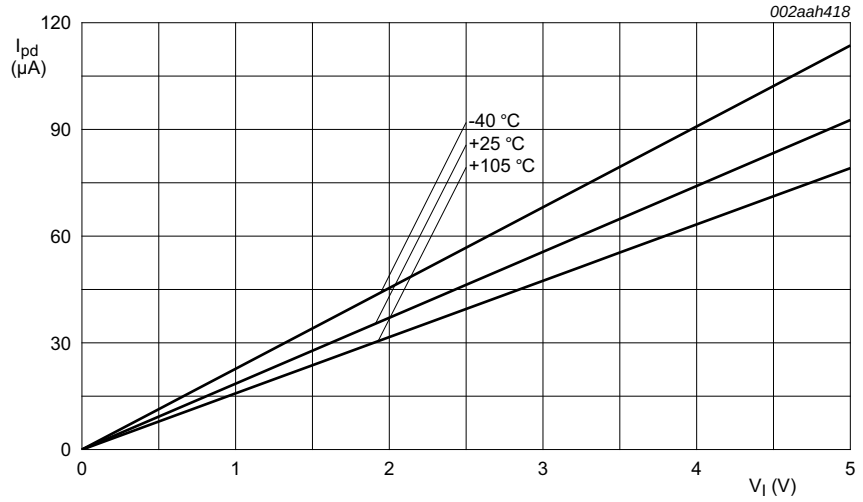
Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus temperature in active mode



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

Fig 23. Pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

Fig 24. Pull-down current I_{pd} versus input voltage V_I

11.2 Wake-up times

Table 17. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +105 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2]	$3 \times T_{cy(clk)}$	$5 \times T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode		12	51	-	µs
		from Deep power-down mode		-	200	-	µs
		after reset		-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

Table 18. Dynamic characteristic: external clock

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Max	Unit
f_{osc}	oscillator frequency			1	25	MHz
$T_{cy(clk)}$	clock cycle time			40	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

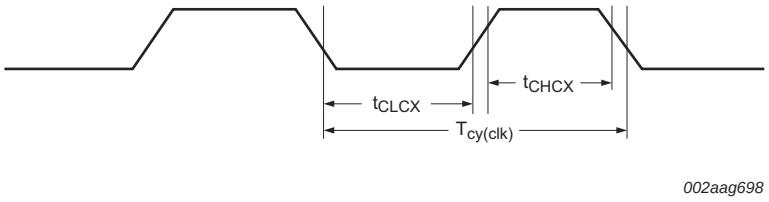


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

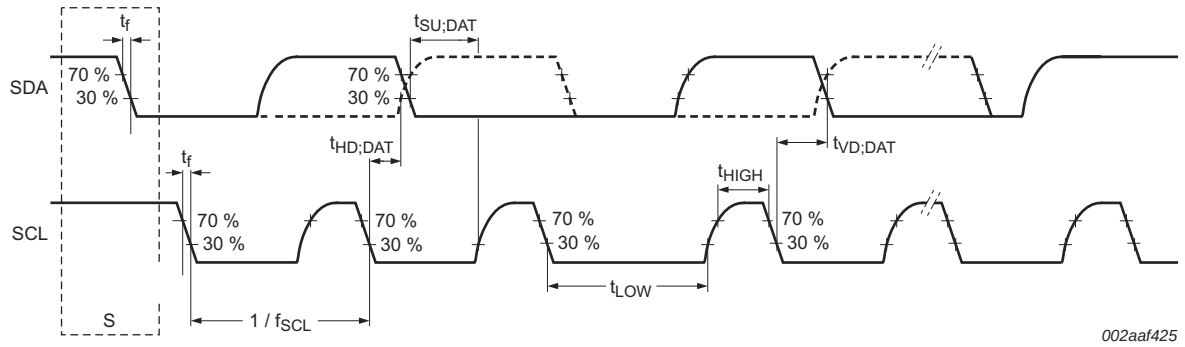


Fig 26. I^2C-bus pins clock timing

11.10 I^2S-bus interface

Table 25. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns, corresponds to the SCK signal in the *I^2S-bus specification*.

Table 28. Dynamic characteristics: Static asynchronous external memory interface *…continued*

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register.Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted which results in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	PB = 0	[2] [5]	−1.9 + $T_{cy(clk)}$	-	−0.5 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 0	[2]	−2.5 + $T_{cy(clk)}$	-	1.4 + $T_{cy(clk)}$	ns
t_{CSHEOW}	$\overline{CS}$ HIGH to end of write time		[5]	−2.0	-	0	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		−2.5	-	1.4	ns
t_{WEHANV}	WE HIGH to address invalid time	PB = 1		−0.9 + $T_{cy(clk)}$	-	2.4 + $T_{cy(clk)}$	ns

[1] Parameters specified for 40 % of $V_{DD(IO)}$ for rising edges and 60 % of $V_{DD(IO)}$ for falling edges.

[2] $T_{cy(clk)}$ = 1/CCLK (see *LPC18xx User manual*).

[3] End Of Read (EOR): longest of t_{CSHOEH}, t_{OEHANV}, $t_{CSHBLSH}$.

[4] Start Of Read (SOR): longest of t_{CSLAV}, t_{CSLOEL}, $t_{CSLBLSL}$.

[5] End Of Write (EOW): earliest of address not valid or $\overline{EMC\_BLSn}$ HIGH.

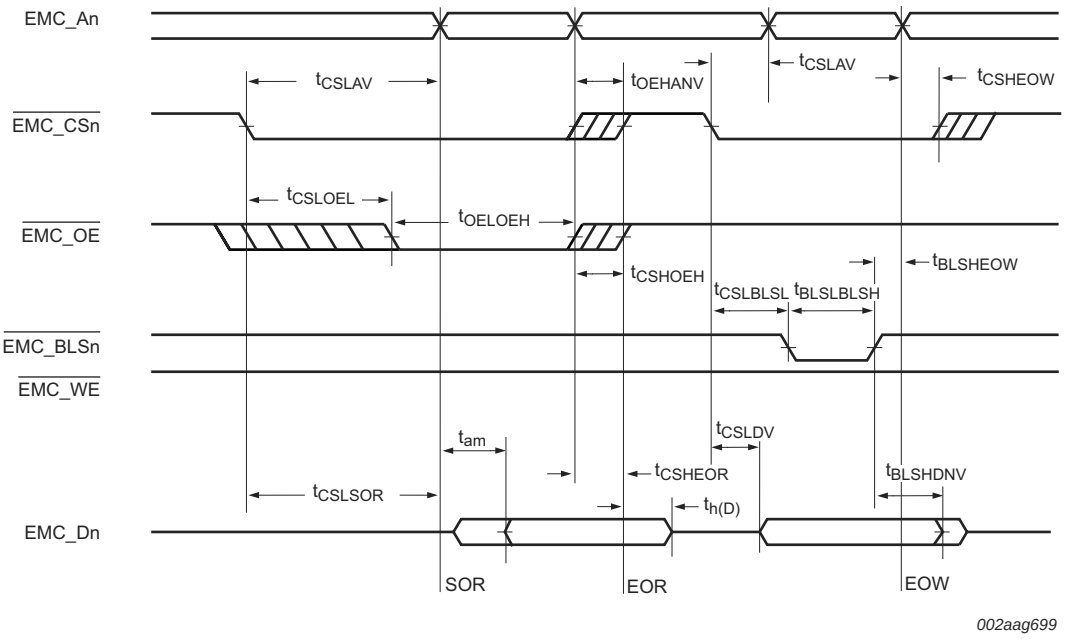


Fig 32. External static memory read/write access (PB = 0)

Table 32. Static characteristics: USB0 PHY pins[1]

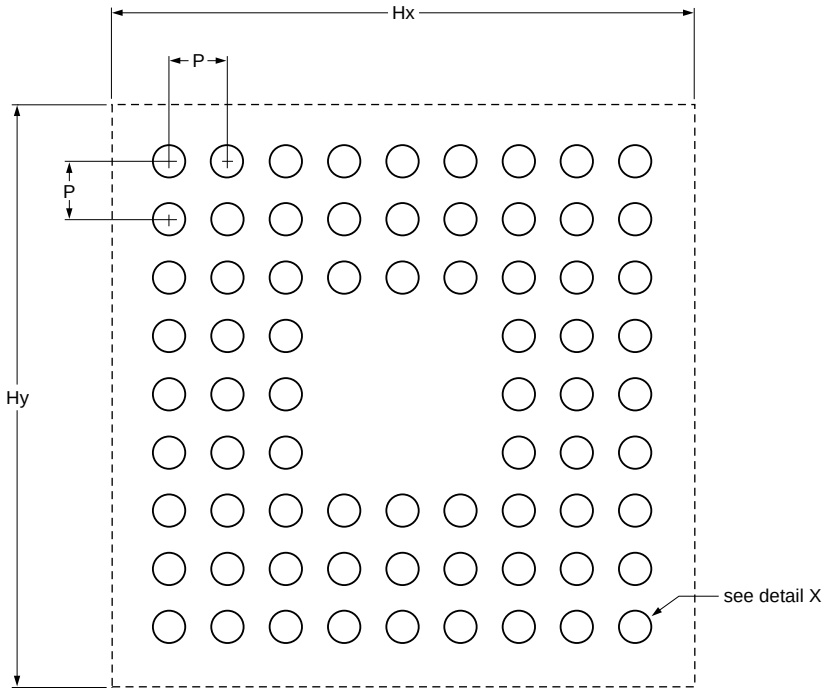
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

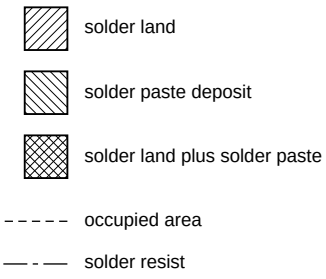
[3] The driver is active only 20 % of the time.

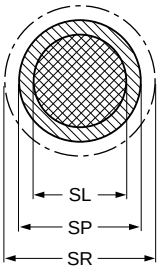
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 54. Reflow soldering for the TFBGA100 package

Table 45. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1857_53 v.3.1	20120904	Preliminary data sheet	-	LPC1857_53 v.3
Modifications:	• SSP0 boot pin functions added in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • Peripheral power consumption data added in Table 12. • BOD de-assertion levels add in Table 13. • Minimum value for all supply voltages changed to -0.5 V n Table 7.			
LPC1857_53 v.3	20120711	Preliminary data sheet	-	LPC1857_53 v.2
Modifications:	• Data sheet status changed to preliminary. • AES removed. Available on parts LPC18Sxx only. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”, “USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Dynamic characteristics of the SD/MMC controller updated in Table 29. • Dynamic characteristics of the LCD controller updated in Table 30. • Dynamic characteristics of the SSP controller updated in Table 22. • Section 10.2 added. • Table 8 “Thermal resistance value (BGA packages)” added. • Description of pins USB1_DP and USB1_DM updated in Table 3. • Editorial updates. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 9.			
LPC1857_53 v.2	20120515	Objective data sheet	-	LPC1857_53 v.1
LPC1857_53 v.1	20111214	Objective data sheet	-	-

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