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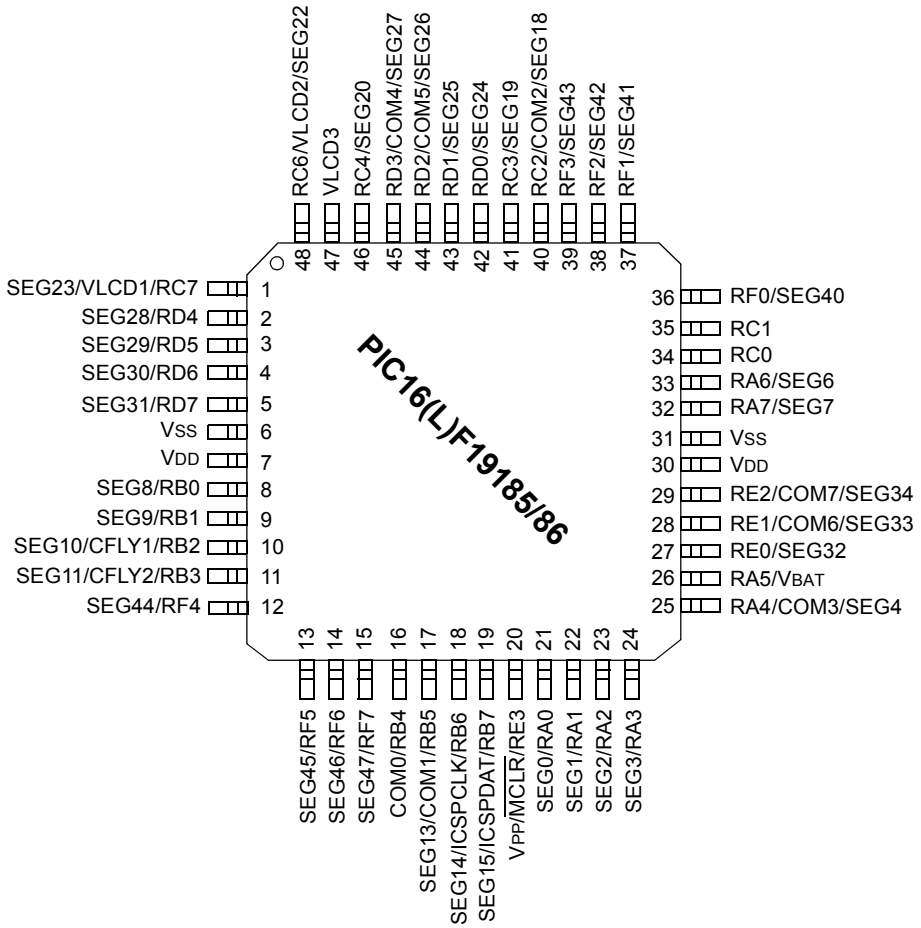
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19155-e-ss

FIGURE 6: 48-PIN TQFP/UQFN PIN DIAGRAM FOR PIC16(L)F19185/86



Note 1: See Table 5 for location of all peripheral functions.

2: QFN package orientation is the same. No leads are present on the QFN package.

4.3.3 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes of the data banks 0-59 and 100 bytes of the data banks 60-63, after the core registers.

The SFRs associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

4.3.4 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank.

TABLE 4-4: GENERAL PURPOSE RAM SIZE AND BANK LOCATION

Bank	PIC16(L)F19155, PIC16(L)F19175, PIC16(L)F19185		PIC16(L)F19156, PIC16(L)F19176, PIC16(L)F19186	
	Address	Size (Bytes)	Address	Size (Bytes)
0	020h-07Fh	96	020h-07Fh	96
1	0A0h-0EFh	80	0A0h-0EFh	80
2	120h-16Fh	80	120h-16Fh	80
3	1A0h-1EFh	80	1A0h-1EFh	80
4	220h-26Fh	80	220h-26Fh	80
5	2A0h-2EFh	80	2A0h-2EFh	80
6	320h-36Fh	80	320h-36Fh	80
7	3A0h-3EFh	80	3A0h-EFh	80
8	420h-46Fh	80	420h-46Fh	80
9	4A0h-4EFh	80	4A0h-4EFh	80
10	520h-560h	80	520h-560h	80
11	5A0h-5EFh	80	5A0h-5EFh	80
12	620h-64Fh	48	620h-64Fh	80
13			6A0h-6EFh	80
14			720h-76Fh	80
15			7A0h-7EFh	80
16			820h-96Fh	80
17			8A0h-8EFh	80
18			920h-96Fh	80
19			9A0h-9EFh	80
20			A20h-A6Fh	80
21			AA0h-AEFh	80
22			B20h-B6Fh	80
23			BA0h-BEFh	80
24			C20h-C6Fh	80
25			CA0h-CBFh	32

Legend: = Unimplemented GPR locations

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 58 (continued)											
1D2Ah	LCDDATA18	S15C3	S14C3	S13C3	—	SE11C3	S10C3	S09C3	S08C3	0000 0000	0000 0000
1D2Bh	LCDDATA19	S23C3	S22C3	—	S20C3	S19C3	S18C3	—	—	0000 0000	0000 0000
1D2Ch	LCDDATA20	S31C3	S30C3	S29C3	S28C3	S27C3	S26C3	S25C3	S24C3	0000 0000	0000 0000
1D2Dh	LCDDATA21	—	—	—	—	—	S34C3	S33C3	S32C3	0000 0000	0000 0000
1D2Eh	LCDDATA22	S47C3	S46C3	S45C3	S44C3	S43C3	S42C3	S41C3	S40C3	0000 0000	0000 0000
1D2Fh	LCDDATA23	S07C4	S06C4	—	S04C4	S03C4	S02C4	S01C4	S00C4	0000 0000	0000 0000
1D30h	LCDDATA24	S15C4	S14C4	S13C4	—	S11C4	S10C4	S09C4	S08C4	0000 0000	0000 0000
1D31h	LCDDATA25	S23C4	S22C4	—	S20C4	S19C4	S18C4	—	—	0000 0000	0000 0000
1D32h	LCDDATA26	S31C4	S30C4	S29C4	S28C4	S27C4	S26C4	S25C4	S24C4	0000 0000	0000 0000
1D33h	LCDDATA27	—	—	—	—	—	S34C4	S33C4	S32C4	0000 0000	0000 0000
1D34h	LCDDATA28	S47C4	S46C4	S45C4	S44C4	S43C4	S42C4	S41C4	S40C4	0000 0000	0000 0000
1D35h	LCDDATA29	S07C5	S06C5	—	S04C5	S03C5	S02C5	S01C5	S00C5	0000 0000	0000 0000
1D36h	LCDDATA30	S15C5	S14C5	S13C5	—	S11C5	S10C5	S09C5	S08C5	0000 0000	0000 0000
1D37h	LCDDATA31	S23C5	S22C5	—	S20C5	S19C5	S18C5	—	—	0000 0000	0000 0000
1D38h	LCDDATA32	S31C5	S30C5	S29C5	S28C5	S27C5	S26C5	S25C5	S24C5	0000 0000	0000 0000
1D39h	LCDDATA33	—	—	—	—	—	S34C5	S33C5	S32C5	0000 0000	0000 0000
1D3Ah	LCDDATA34	S47C5	S46C5	S45C5	S44C5	S43C5	S42C5	S41C5	S40C5	0000 0000	0000 0000
1D3Bh	LCDDATA35	S07C6	S06C6	—	S04C6	S03C6	S02C6	S01C6	S00C6	0000 0000	0000 0000
1D3Ch	LCDDATA36	S15C6	S14C6	S13C6	—	S11C6	S10C6	S09C6	S08C6	0000 0000	0000 0000
1D3Dh	LCDDATA37	S23C6	S22C6	—	S20C6	S19C6	S18C6	—	—	0000 0000	0000 0000
1D3Eh	LCDDATA38	S31C6	S30C6	S29C6	S28C6	S27C6	S26C6	S25C6	S24C6	0000 0000	0000 0000
1D3Fh	LCDDATA39	—	—	—	—	—	S34C6	S33C6	S32C6	0000 0000	0000 0000
1D40h	LCDDATA40	S47C6	S46C6	S45C6	S44C6	S43C6	S42C6	S41C6	S40C6	0000 0000	0000 0000
1D41h	LCDDATA41	S07C7	S06C7	—	S04C7	S03C7	S02C7	S01C7	S00C7	0000 0000	0000 0000
1D42h	LCDDATA42	S15C7	S14C7	S13C7	—	S11C7	S10C7	S09C7	S08C7	0000 0000	0000 0000
1D43h	LCDDATA43	S23C7	S22C7	—	S20C7	S19C7	S18C7	—	—	0000 0000	0000 0000
1D44h	LCDDATA44	S31C7	S30C7	S29C7	S28C7	S27C7	S26C7	S25C7	S24C7	0000 0000	0000 0000
1D45h	LCDDATA45	—	—	—	—	—	S34C7	S33C7	S32C7	0000 0000	0000 0000
1D46h	LCDDATA46	S47C7	S46C7	S45C7	S44C7	S43C7	S42C7	S41C7	S40C7	0000 0000	0000 0000
1D47h	LCDDATA47	S07C0	S06C0	—	S04C0	S03C0	S02C0	S01C0	S00C0	0000 0000	0000 0000

9.6 Register Definitions: Oscillator Control

REGISTER 9-1: OSCCON1: OSCILLATOR CONTROL REGISTER1

U-0	R/W-f/f(1)	R/W-f/f(1)	R/W-f/f(1)	R/W-q/q	R/W-q/q	R/W-q/q	R/W-q/q
—	NOSC<2:0>(2,3)			NDIV<3:0>(2,3,4)			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	f = determined by fuse setting

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **NOSC<2:0>:** New Oscillator Source Request bits
The setting requests a source oscillator and PLL combination per Table 9-1.
POR value = RSTOSC (Register 5-1).

bit 3-0 **NDIV<3:0>:** New Divider Selection Request bits
The setting determines the new postscaler division ratio per Table 9-1.

Note 1: The default value (f/f) is set equal to the RSTOSC Configuration bits.
2: If NOSC is written with a reserved value (Table 9-1), the operation is ignored and neither NOSC nor NDIV is written.
3: When CSWEN = 0, this register is read-only and cannot be changed from the POR value.
4: When NOSC = 110 (HFINTOSC 4 MHz), the NDIV bits will default to '0010' upon Reset; for all other NOSC settings the NDIV bits will default to '0000' upon Reset.

REGISTER 9-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2(1)

U-0	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)
—	COSC<2:0>			CDIV<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **COSC<2:0>:** Current Oscillator Source Select bits (read-only)
Indicates the current source oscillator and PLL combination per Table 9-1.

bit 3-0 **CDIV<3:0>:** Current Divider Select bits (read-only)
Indicates the current postscaler division ratio per Table 9-1.

Note 1: The POR value is the value present when user code execution begins.
2: The Reset value (n/n) is the same as the NOSC/NDIV bits.

EXAMPLE 13-3: ERASING ONE ROW OF PROGRAM FLASH MEMORY (PFM)

```
; This sample row erase routine assumes the following:
; 1.A valid address within the erase row is loaded in variables ADDRH:ADDRL
; 2.ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)

BANKSEL         NVMADRL
MOVF            ADDRL,W
MOVWF           NVMADRL                 ; Load lower 8 bits of erase address boundary
MOVF            ADDRH,W
MOVWF           NVMADRH                 ; Load upper 6 bits of erase address boundary
BCF             NVMCON1,NVMREGS         ; Choose PFM memory area
BSF             NVMCON1,FREE            ; Specify an erase operation
BSF             NVMCON1,WREN            ; Enable writes
BCF             INTCON,GIE              ; Disable interrupts during unlock sequence

; ------------------------------REQUIRED UNLOCK SEQUENCE:------------------------------

MOVLW           55h                     ; Load 55h to get ready for unlock sequence
MOVWF           NVMCON2                 ; First step is to load 55h into NVMCON2
MOVLW           AAh                     ; Second step is to load AAh into W
MOVWF           NVMCON2                 ; Third step is to load AAh into NVMCON2
BSF             NVMCON1,WR              ; Final step is to set WR bit

; -------------------------------------------------------------------------------------

BSF             INTCON,GIE              ; Re-enable interrupts, erase is complete
BCF             NVMCON1,WREN            ; Disable writes
```

REGISTER 13-6: NVMCON2: NONVOLATILE MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
NVMCON2<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **NVMCON2<7:0>:** Flash Memory Unlock Pattern bits

To unlock writes, a 55h must be written first followed by an AAh before setting the WR bit of the NVMCON1 register. The value written to this register is used to unlock the writes.

TABLE 13-5: SUMMARY OF REGISTERS ASSOCIATED WITH NONVOLATILE MEMORY (NVM)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	172
PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	181
NVMCON1	—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	217
NVMCON2	NVMCON2<7:0>								218
NVMADRL	NVMADR<7:0>								216
NVMADRH	—(1)	NVMADR<14:8>							216
NVMDATL	NVMDAT<7:0>								216
NVMDATH	—	—	NVMDAT<13:8>						216

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by NVM.

Note 1: Unimplemented, read as '1'.

REGISTER 14-7: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRA7	SLRA6	—	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **SLRA<7:6>:** PORTA Slew Rate Enable bits
For RA<7:6> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

bit 5 **Unimplemented:** Read as ‘0’.

bit 4-0 **SLRA<4:0>:** PORTA Slew Rate Enable bits
For RA<4:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 14-8: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **INLVLA<7:0>:** PORTA Input Level Select bits
For RA<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

23.2 ZCD Logic Output

The ZCD module includes a Status bit, which can be read to determine whether the current source or sink is active. The OUT bit of the ZCDxCON register is set when the current sink is active, and cleared when the current source is active. The OUT bit is affected by the polarity even if the module is disabled.

23.3 ZCD Logic Polarity

The POL bit of the ZCDxCON register inverts the ZCDxOUT bit relative to the current source and sink output. When the POL bit is set, a OUT high indicates that the current source is active, and a low output indicates that the current sink is active.

The POL bit affects the ZCD interrupts. See **Section 23.4 "ZCD Interrupts"**.

23.4 ZCD Interrupts

An interrupt will be generated upon a change in the ZCD logic output when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in the ZCD for this purpose.

The ZCDIF bit of the PIR2 register will be set when either edge detector is triggered and its associated enable bit is set. The INTP enables rising edge interrupts and the INTN bit enables falling edge interrupts. Both are located in the ZCDxCON register.

To fully enable the interrupt, the following bits must be set:

- ZCDIE bit of the PIE2 register
- INTP bit of the ZCDxCON register (for a rising edge detection)
- INTN bit of the ZCDxCON register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

Changing the POL bit can cause an interrupt, regardless of the level of the EN bit.

The ZCDIF bit of the PIR2 register must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

23.5 Correcting for V_{CPINV} offset

The actual voltage at which the ZCD switches is the reference voltage at the noninverting input of the ZCD op amp. For external voltage source waveforms other than square waves, this voltage offset from zero causes the zero-cross event to occur either too early or too late.

23.5.1 CORRECTION BY AC COUPLING

When the external voltage source is sinusoidal then the effects of the V_{CPINV} offset can be eliminated by isolating the external voltage source from the ZCD pin with a capacitor in addition to the voltage reducing resistor. The capacitor will cause a phase shift resulting in the ZCD output switch in advance of the actual zero-crossing event. The phase shift will be the same for both rising and falling zero crossings, which can be compensated for by either delaying the CPU response to the ZCD switch by a timer or other means, or selecting a capacitor value large enough that the phase shift is negligible.

To determine the series resistor and capacitor values for this configuration, start by computing the impedance, Z, to obtain a peak current of 300 uA. Next, arbitrarily select a suitably large non-polar capacitor and compute its reactance, Xc, at the external voltage source frequency. Finally, compute the series resistor, capacitor peak voltage, and phase shift by the formulas shown in Equation 23-2.

REGISTER 26-4: T1GATE TIMER1 GATE SELECT REGISTER

U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	GSS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **GSS<4:0>:** Timer1 Gate Select bits

11111-10001 = Reserved
10000 = RTCC second output
01111 = ZCD1 output
01110 = C2OUT output
01101 = C1OUT output
01100 = LC4 out
01011 = LC3 out
01010 = LC2 out
01001 = LC1 out
01000 = PWM4 out
00111 = PWM3 out
00110 = CCP2 out
00101 = CCP1 out
00100 = SMT1 overflow output
00011 = TMR4 postscaled
00010 = TMR2 postscaled
00001 = Timer0 overflow output
00000 = T1GPPS

FIGURE 28-1: SMTx BLOCK DIAGRAM

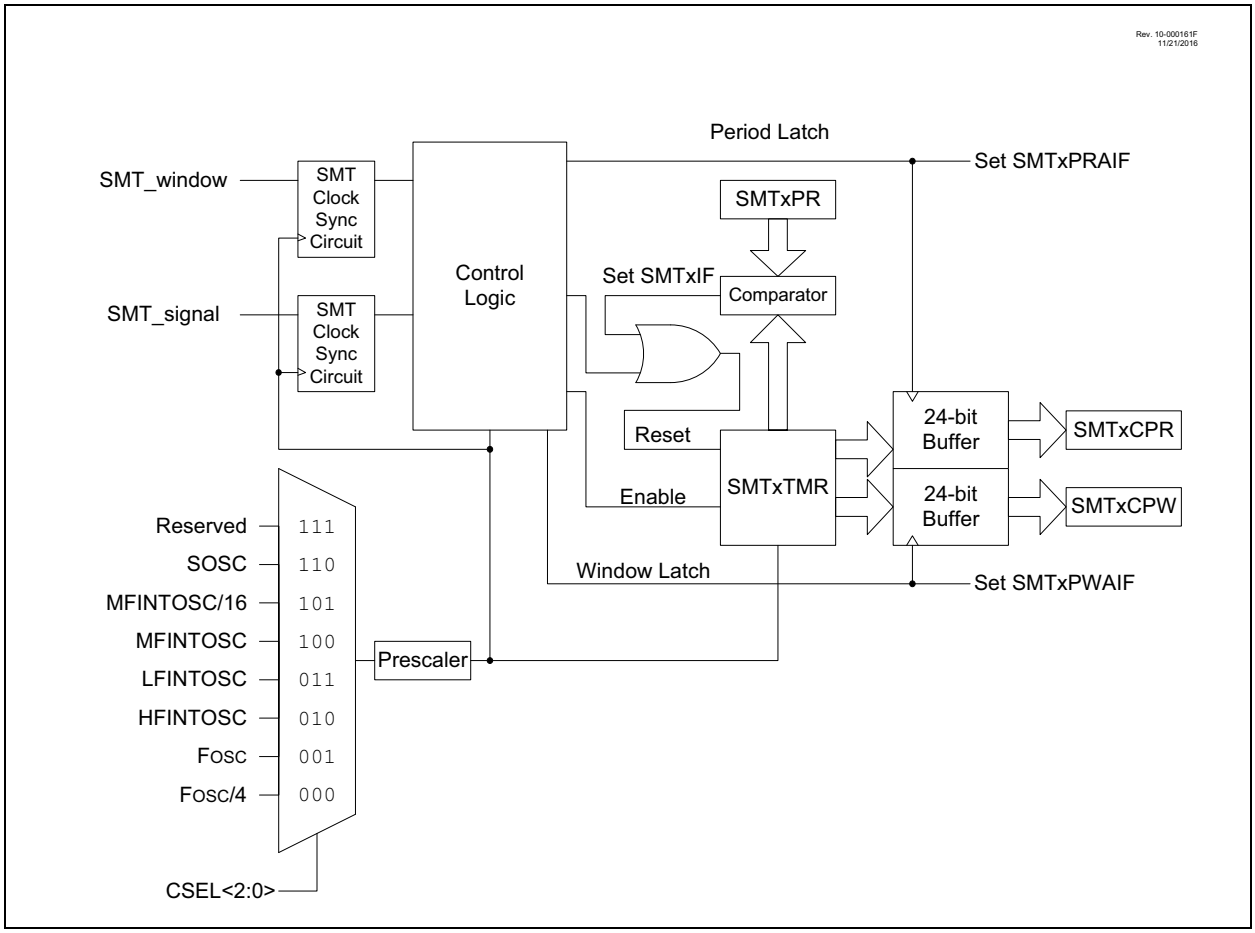


FIGURE 28-2: SMTx SIGNAL AND WINDOW BLOCK DIAGRAM

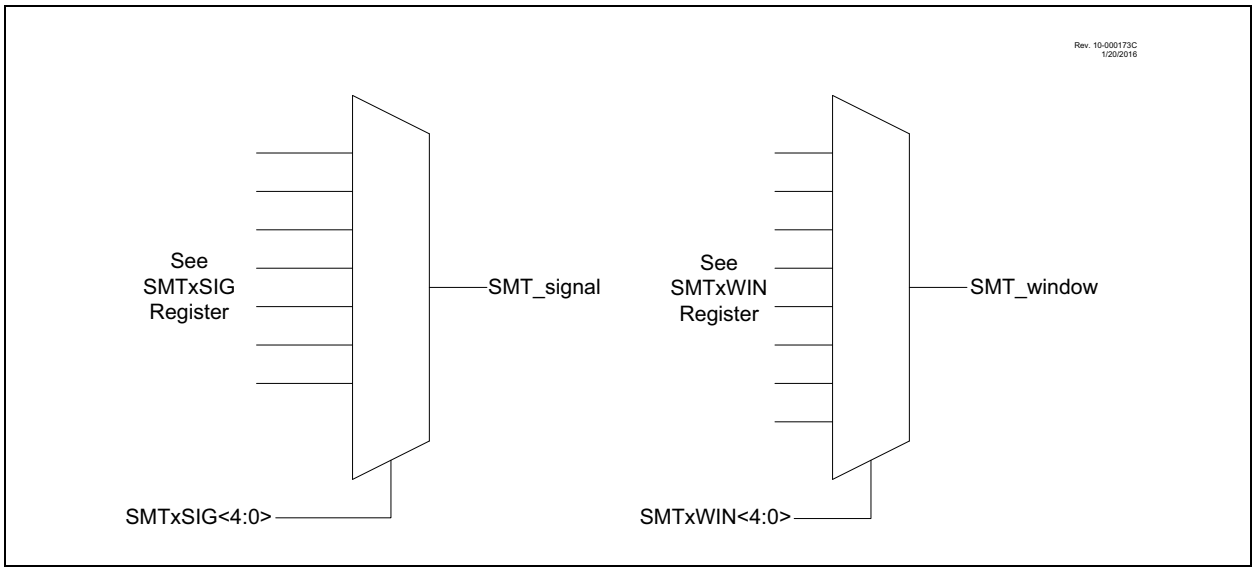
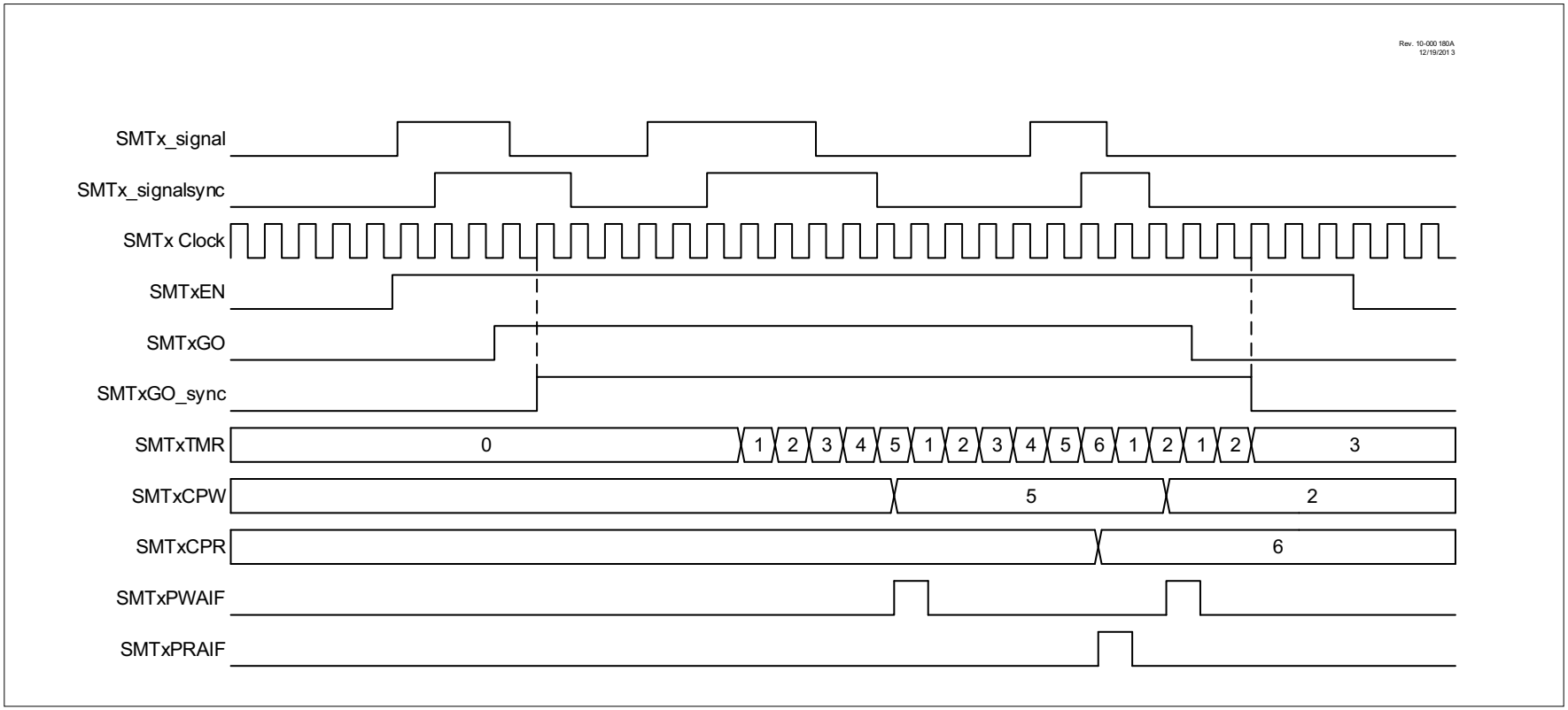


FIGURE 28-8: HIGH AND LOW-MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM



31.10 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in Figure 31-12.

31.10.1 SHUTDOWN

The shutdown state can be entered by either of the following two methods:

- Software generated
- External input

31.10.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit of the CWG1AS0 register will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event.

31.10.2 EXTERNAL INPUT SOURCE

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the selected override levels without software delay. Several input sources can be selected to cause a shutdown condition. All input sources are active-low. The sources are:

- Comparator C1OUT_sync
- Comparator C2OUT_sync
- Timer2 – TMR2_postscaled
- CWG1IN input pin

Shutdown inputs are selected using the CWG1AS1 register (Register 31-6).

Note:	Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

31.11 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep when all the following conditions are met:

- CWG module is enabled
- Input source is active
- HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, then the CPU will go idle during Sleep, but the HFINTOSC will remain active and the CWG will continue to operate. This will have a direct effect on the Sleep mode current.

REGISTER 32-11: CLCDATA: CLC DATA OUTPUT

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

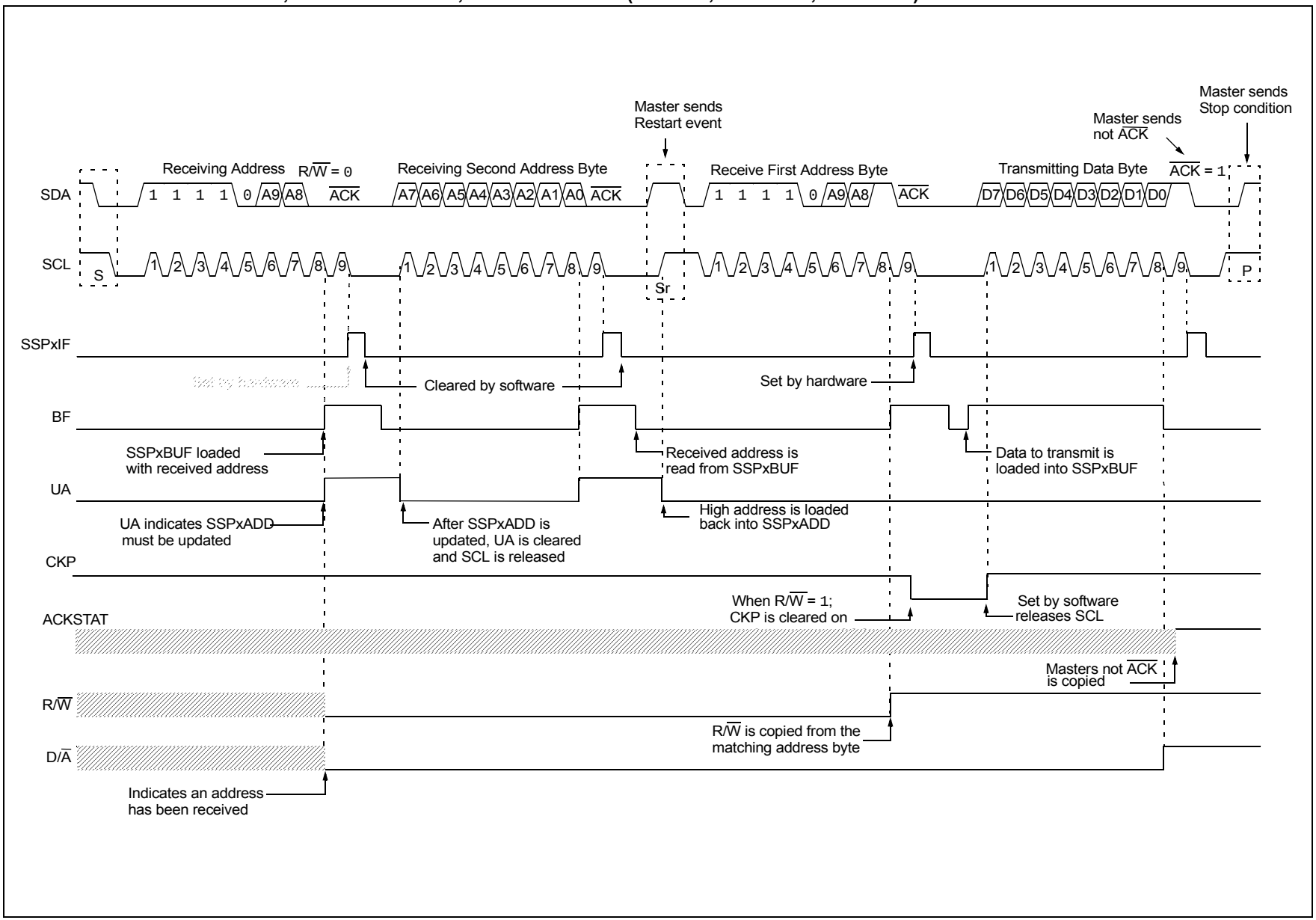
bit 3 **MLC4OUT:** Mirror copy of LC4OUT bit

bit 2 **MLC3OUT:** Mirror copy of LC3OUT bit

bit 1 **MLC2OUT:** Mirror copy of LC2OUT bit

bit 0 **MLC1OUT:** Mirror copy of LC1OUT bit

FIGURE 33-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)



33.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

33.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/$\overline{W}$ bit of SSPxSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

33.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPxADD.

33.5.6.3 Byte NACKing

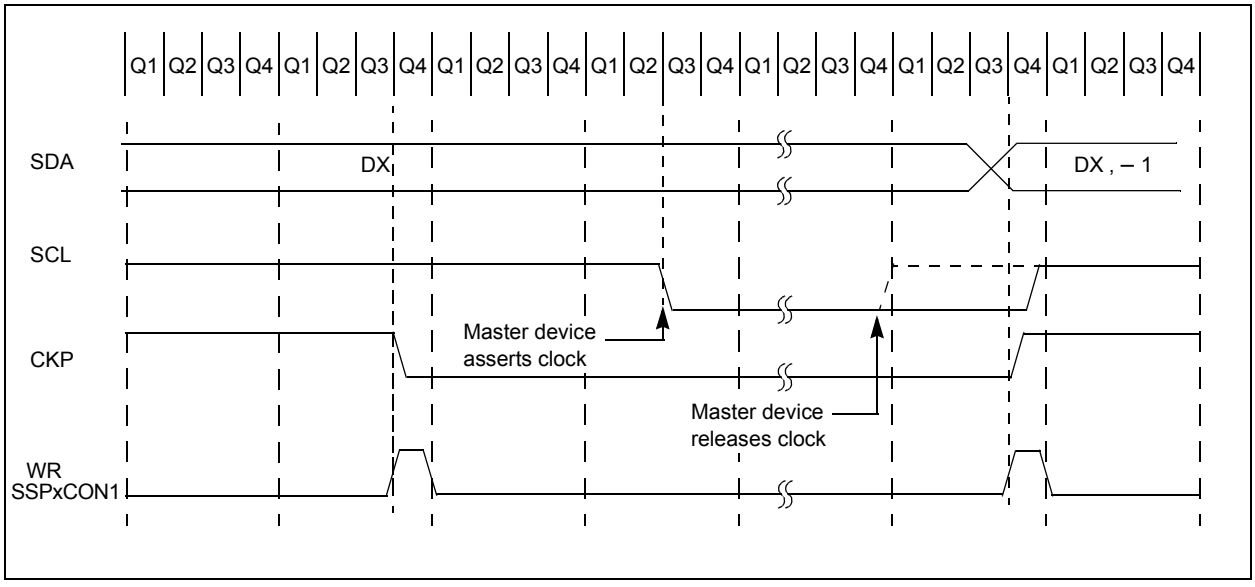
When AHEN bit of SSPxCON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSPxCON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

33.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 33-23).

FIGURE 33-23: CLOCK SYNCHRONIZATION TIMING



35.7.4 35.6.4 INTERNAL RESISTOR WITH EXTERNAL CAPACITORS

In this configuration, the user can use the internal resistor ladders to generate the LCD bias levels, and use external capacitors to guard again burst currents. It is recommend the user utilize the external capacitors when driving large glass panels with a large pixels and a high pixel count. The external capacitors will help dampen current spikes during segment switching. Contrast is adjusted using the LCDCST<2:0> bits. The CFLYx pins are available as a GPIO. See Figure 35-7 for supported connections.

External capacitors can be used when voltage to the internal resistor ladder is supplied by VDD (LCDVSRC<3:0> = 0101) or an external source (LCDVSRC<3:0> = 0100). When supplying an external voltage to internal resistor ladder the external capacitors should be limited to VLCD2, and VLCD3.

REGISTER 35-5: LCDVCON1: LCD VOLTAGE CONTROL 1 BITS

R/W-0/0	R/W-0/0	R-0	R-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0
LPEN	EN5V	—	—	—	BIAS2	BIAS1	BIAS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **LPEN**: LCD Charge Pump Low Power Enable (Low-Current (LC) mode enable)
1 = LCD Charge Pump is operating in Low-Current mode
0 = LCD Charge Pump is operating in Normal-Current mode

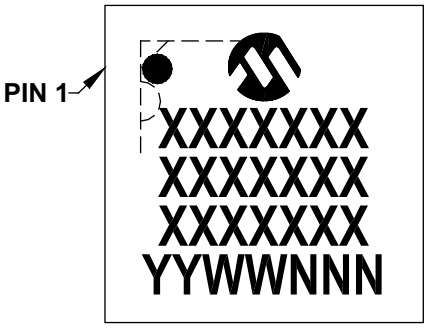
bit 6 **EN5V:** 5V Range Enable bit
1 = The pump generates 5.0V voltage range
0 = The pump generates 3.5V voltage range

bit 5-3 **Reserved**: Read as '0'

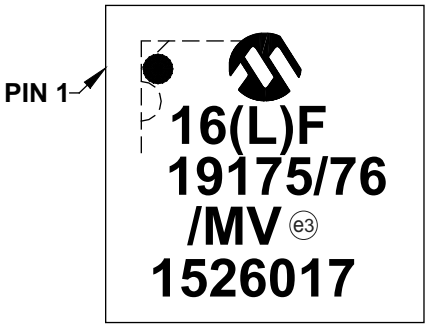
bit 2-0 **BIAS<2:0>:** Boost Pump Voltage Output Control bits (Only valid when LCDVSRC<2:0> = 100, 101, 110)
When EN5V = 0
111 = Set boost pump output to 3.50V
110 = Set boost pump output to 3.40V
101 = Set boost pump output to 3.30V
100 = Set boost pump output to 3.20V
011 = Set boost pump output to 3.10V
010 = Set boost pump output to 3.00V
001 = Set boost pump output to 2.90V
000 = Set boost pump output to 2.80V
When EN5V = 1
111 = Set boost pump output to 5.01V
110 = Set boost pump output to 4.83V
101 = Set boost pump output to 4.66V
100 = Set boost pump output to 4.48V
011 = Set boost pump output to 4.31V
010 = Set boost pump output to 4.13V
001 = Set boost pump output to 3.95V
000 = Set boost pump output to 3.78V

42.1 Package Marking Information (Continued)

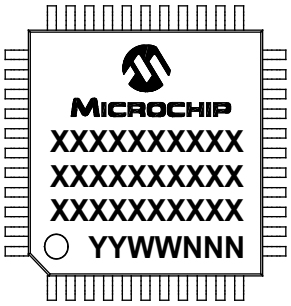
40-Lead UQFN (5x5x0.5 mm)



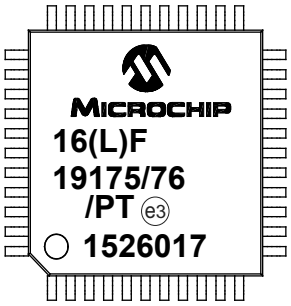
Example



44-Lead TQFP (10x10x1 mm)



Example

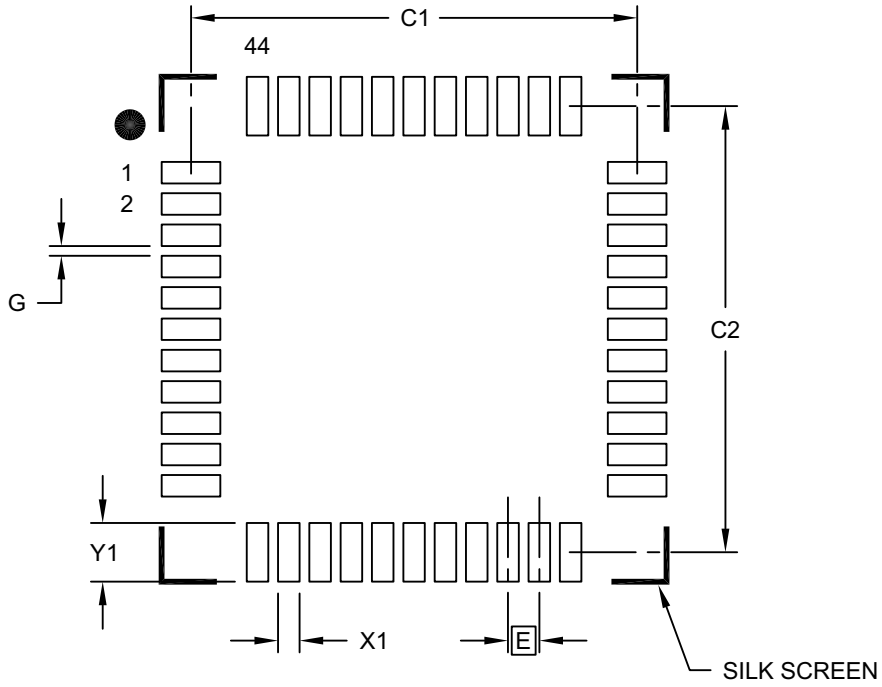


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

44-Lead Plastic Thin Quad Flatpack (PT) - 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F19155, PIC16(L)F19155 PIC16F19156, PIC16(L)F19156 PIC16F19175, PIC16(L)F19175 PIC16F19176, PIC16(L)F19176 PIC16F19185, PIC16(L)F19185 PIC16F19186, PIC16(L)F19186	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:(2)	SS SO SP MV P MV PT MV PT	= 28-lead SSOP = 28-lead SOIC = 28-lead SPDIP = 28-lead UQFN = 40-lead PDIP = 40-lead UQFN = 44-lead TQFP = 48-lead UQFN = 48-lead TQFP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16(L)F19185/86 - I/PT
Industrial temperature
TQFP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.