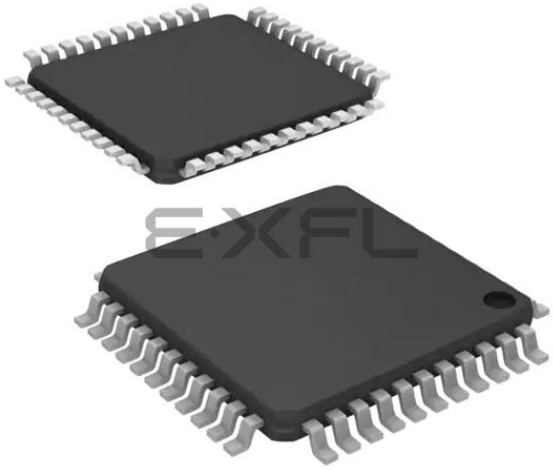

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TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RA0	2	17	19	19	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG0	IOCA0	—	Y	—
RA1	3	18	20	20	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	SEG1	IOCA1	—	Y	—
RA2	4	19	21	21	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG2	IOCA2	—	Y	—
RA3	5	20	22	22	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	SEG3	IOCA3	—	Y	—
RA4	6	21	23	23	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG4 COM3	IOCA4	—	Y	—
RA5	7	22	24	24	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	—	IOCA5	—	—	VBAT
RA6	14	29	31	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG6	IOCA6	—	Y	CLKOUT OSC2
RA7	13	28	30	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	SEG7	IOCA7	—	Y	OSC1 CLKIN
RB0	33	8	8	9	ANB0	—	C2IN1+	ZCD	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG8	IOCB0	—	Y	INTPPS
RB1	34	9	9	10	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG9	IOCB1	HIB1	Y	—
RB2	35	10	10	11	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG10 CFLY1	IOCB2	—	Y	—
RB3	36	11	11	12	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG11 CFLY2	IOCB3	—	Y	—
RB4	37	12	14	14	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM0	IOCB4	—	Y	—
RB5	38	13	15	15	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG13 COM1	IOCB5	—	Y	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	SEG14	IOCB6	—	Y	ICDCLK/ ICSPCLK
RB7	40	15	17	17	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	SEG15	IOCB7	—	Y	ICDDAT/ ICSPDAT

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

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TABLE 1-4: PIC16(L)F19185/86 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Types	Output Types	Description
RD7/AND7/SEG31	RD7	TTL/ST	CMOS/OD	General purpose I/O.
	AND7	AN	—	ADC Channel input.
	SEG31	AN	—	LCD Analog output.
RE0/ANE0/SEG32	RE0	TTL/ST	CMOS/OD	General purpose I/O.
	ANE0	AN	—	ADC Channel input.
	SEG32	—	AN	LCD Analog output.
RE1/ANE2/SEG33/COM6	RE1	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel input.
	SEG33	—	AN	LCD analog input
	COM6	—	AN	LCD Driver Common Outputs.
RE2/ANE2/SEG34/COM7	RE2	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel input.
	SEG34	—	AN	LCD analog input
	COM7	—	AN	LCD Driver Common Outputs.
RE3/IOCE3/MCLR	RE3	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	MCLR	ST	—	Master clear input with internal weak pull up resistor.
RF0/ANF0/SEG40	RF0	TTL/ST	CMOS/OD	General purpose I/O.
	ANF0	AN	—	ADC Channel input.
	SEG40	—	AN	LCD Analog output.
RF1/ANF1/SEG41	RF1	TTL/ST	CMOS/OD	General purpose I/O.
	ANF1	AN	—	ADC Channel input.
	SEG41	—	AN	LCD Analog output.
RF2/ANF2/SEG42	RF2	TTL/ST	CMOS/OD	General purpose I/O.
	ANF2	AN	—	ADC Channel input.
	SEG42	—	AN	LCD Analog output.
RF3/ANF3/SEG43	RF3	TTL/ST	CMOS/OD	General purpose I/O.
	ANF3	AN	—	ADC Channel input.
	SEG43	—	AN	LCD Analog output.
RF4/ANF4/SEG44	RF4	TTL/ST	CMOS/OD	General purpose I/O.
	ANF4	AN	—	ADC Channel input.
	SEG44	—	AN	LCD Analog output.
RF5/ANF5/SEG45	RF5	TTL/ST	CMOS/OD	General purpose I/O.
	ANF5	AN	—	ADC Channel input.
	SEG45	—	AN	LCD Analog output.
RF6/ANF6/SEG46	RF6	TTL/ST	CMOS/OD	General purpose I/O.
	ANF6	AN	—	ADC Channel input.
	SEG46	—	AN	LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

1D3Bh	LCDDATA35	1DBBh	—	1E3Bh	RF3PPS(3)	1EBBh	CLCIN0PPS	1F3Bh	SLRCONA	1FBBh	—
1D3Ch	LCDDATA36	1DBCh	—	1E3Ch	RF4PPS(3)	1EBCh	CLCIN1PPS	1F3Ch	INLVLA	1FBCh	—
1D3Dh	LCDDATA37	1DBDh	—	1E3Dh	RF5PPS(3)	1EBDh	CLCIN2PPS	1F3Dh	IOCAP	1FBDh	—
1D3Eh	LCDDATA38	1DBEh	—	1E3Eh	RF6PPS(3)	1EBEh	CLCIN3PPS	1F3Eh	IOCAN	1FBEh	—
1D3Fh	LCDDATA39	1DBFh	—	1E3Fh	RF7PPS(3)	1EBFh	—	1F3Fh	IOCAF	1FBFh	—
1D40h	LCDDATA40	1DC0h	—	1E40h	—	1EC0h	—	1F40h	—	1FC0h	—
1D41h	LCDDATA41	1DC1h	—	1E41h	—	1EC1h	—	1F41h	—	1FC1h	—
1D42h	LCDDATA42	1DC2h	—	1E42h	—	1EC2h	—	1F42h	—	1FC2h	—
1D43h	LCDDATA43	1DC3h	—	1E43h	—	1EC3h	ADCACTPPS	1F43h	ANSELB	1FC3h	—
1D44h	LCDDATA44	1DC4h	—	1E44h	—	1EC4h	—	1F44h	WPUB	1FC4h	—
1D45h	LCDDATA45	1DC5h	—	1E45h	—	1EC5h	SSP1CLKPPS	1F45h	ODCONB	1FC5h	—
1D46h	LCDDATA46	1DC6h	—	1E46h	—	1EC6h	SSP1DATPPS	1F46h	SLRCONB	1FC6h	—
1D47h	LCDDATA47	1DC7h	—	1E47h	—	1EC7h	SSP1SSPPS	1F47h	INLVLB	1FC7h	—
1D48h	—	1DC8h	—	1E48h	—	1EC8h	—	1F48h	IOCBP	1FC8h	—
1D49h	—	1DC9h	—	1E49h	—	1EC9h	—	1F49h	IOCBN	1FC9h	—
1D4Ah	—	1DCAh	—	1E4Ah	—	1ECAh	—	1F4Ah	IOCBF	1FCAh	—
1D4Bh	—	1DCBh	—	1E4Bh	—	1ECBh	RX1PPS	1F4Bh	—	1FCBh	—
1D4Ch	—	1DCCh	—	1E4Ch	—	1ECCh	TX1PPS	1F4Ch	—	1FCCh	—
1D4Dh	—	1DCDh	—	1E4Dh	—	1ECDh	RX2PPS	1F4Dh	—	1FCDh	—
1D4Eh	—	1DCEh	—	1E4Eh	—	1ECEh	TX2PPS	1F4Eh	ANSELC	1FCEh	—
1D4Fh	—	1DCFh	—	1E4Fh	—	1ECFh	—	1F4Fh	WPUC	1FCFh	—
1D50h	—	1DD0h	—	1E50h	ANSELF(3)	1ED0h	—	1F50h	ODCONC	1FD0h	—
1D51h	—	1DD1h	—	1E51h	WPUF(3)	1ED1h	—	1F51h	SLRCONC	1FD1h	—
1D52h	—	1DD2h	—	1E52h	ODCONF(3)	1ED2h	—	1F52h	INLVLC	1FD2h	—
1D53h	—	1DD3h	—	1E53h	SLRCONF(3)	1ED3h	—	1F53h	IOCCP	1FD3h	—
1D54h	—	1DD4h	—	1E54h	INLVLF(3)	1ED4h	—	1F54h	IOCCN	1FD4h	—
1D55h	—	1DD5h	—	1E55h	—	1ED5h	—	1F55h	IOCCF	1FD5h	—
1D56h	—	1DD6h	—	1E56h	—	1ED6h	—	1F56h	—	1FD6h	—
1D57h	—	1DD7h	—	1E57h	—	1ED7h	—	1F57h	—	1FD7h	—
1D58h	—	1DD8h	—	1E58h	—	1ED8h	—	1F58h	—	1FD8h	—
1D59h	—	1DD9h	—	1E59h	—	1ED9h	—	1F59h	ANSELD	1FD9h	—
1D5Ah	—	1DDAh	—	1E5Ah	—	1EDAh	—	1F5Ah	WPUD	1FDAh	—
1D5Bh	—	1DDBh	—	1E5Bh	—	1EDBh	—	1F5Bh	ODCOND	1FDBh	—
1D5Ch	—	1DDCh	—	1E5Ch	—	1EDCh	—	1F5Ch	SLRCOND	1FDCh	—
1D5Dh	—	1DDDh	—	1E5Dh	—	1EDDh	—	1F5Dh	INLVLD	1FDDh	—
1D5Eh	—	1DDEh	—	1E5Eh	—	1EDEh	—	1F5Eh	—	1FDEh	—
1D5Fh	—	1DDFh	—	1E5Fh	—	1EDFh	—	1F5Fh	—	1FDFh	—
1D60h	—	1DE0h	—	1E60h	—	1EE0h	—	1F60h	—	1FE0h	—
1D61h	—	1DE1h	—	1E61h	—	1EE1h	—	1F61h	—	1FE1h	—
1D62h	—	1DE2h	—	1E62h	—	1EE2h	—	1F62h	—	1FE2h	—
1D63h	—	1DE3h	—	1E63h	—	1EE3h	—	1F63h	—	1FE3h	—
1D64h	—	1DE4h	—	1E64h	—	1EE4h	—	1F64h	ANSELE	1FE4h	STATUS_SHAD
1D65h	—	1DE5h	—	1E65h	—	1EE5h	—	1F65h	WPUE	1FE5h	WREG_SHAD
1D66h	—	1DE6h	—	1E66h	—	1EE6h	—	1F66h	ODCONE	1FE6h	BSR_SHAD
1D67h	—	1DE7h	—	1E67h	—	1EE7h	—	1F67h	SLRCONE	1FE7h	PCLATH_SHAD
1D68h	—	1DE8h	—	1E68h	—	1EE8h	—	1F68h	INLVLE	1FE8h	FSR0L_SHAD
1D69h	—	1DE9h	—	1E69h	—	1EE9h	—	1F69h	IOCEP	1FE9h	FSR0H_SHAD
1D6Ah	—	1DEAh	—	1E6Ah	—	1EEAh	—	1F6Ah	IOCEN	1FEAh	FSR1L_SHAD
1D6Bh	—	1DEBh	—	1E6Bh	—	1EEBh	—	1F6Bh	IOCEF	1FEBh	FSR1H_SHAD
1D6Ch	—	1DECh	—	1E6Ch	—	1EECh	—	1F6Ch	—	1FECh	—
1D6Dh	—	1DEDh	—	1E6Dh	—	1EEDh	—	1F6Dh	—	1FEDh	STKPTR

Note 1: Unimplemented locations read as '0'.
2: Present only on PIC16(L)F19156/76/86.
3: Present only on PIC16(L)F19185/86.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 62 (Continued)											
1F64h	ANSELE	ANSE7	ANSE6	ANSE5	ANSE4	ANSE3	—	ANSE1	ANSE0	1111 1-11	1111 1-11
1F65h	WPUE	WPUE7	WPUE6	WPUE5	WPUE4	WPUE3	—	WPUE1	WPUE0	0000 0-00	0000 0-00
1F66h	ODCONE	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	—	ODCE1	ODCE0	0000 0-00	0000 0-00
1F67h	SLRCONE	SLRE7	SLRE6	SLRE5	SLRE4	SLRE3	—	SLRE1	SLRE0	1111 1-11	1111 1-11
1F68h	INLVLE	INLVLE7	INLVLE6	INLVLE5	INLVLE4	INLVLE3	—	INLVLE1	INLVLE0	1111 1-11	1111 1-11
1F69h	IOCEP	—	—	—	—	IOCEP3	—	—	—	0000 0000	0000 0000
1F6Ah	IOCEN	—	—	—	—	IOCEN3	—	—	—	0000 0000	0000 0000
1F6Bh	IOCEF	—	—	—	—	IOCEF3	—	—	—	0000 0000	0000 0000
1F6Ch	—	Unimplemented								---- ----	---- ----
1F6Dh	—	Unimplemented								---- ----	---- ----
1F6Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

Preliminary

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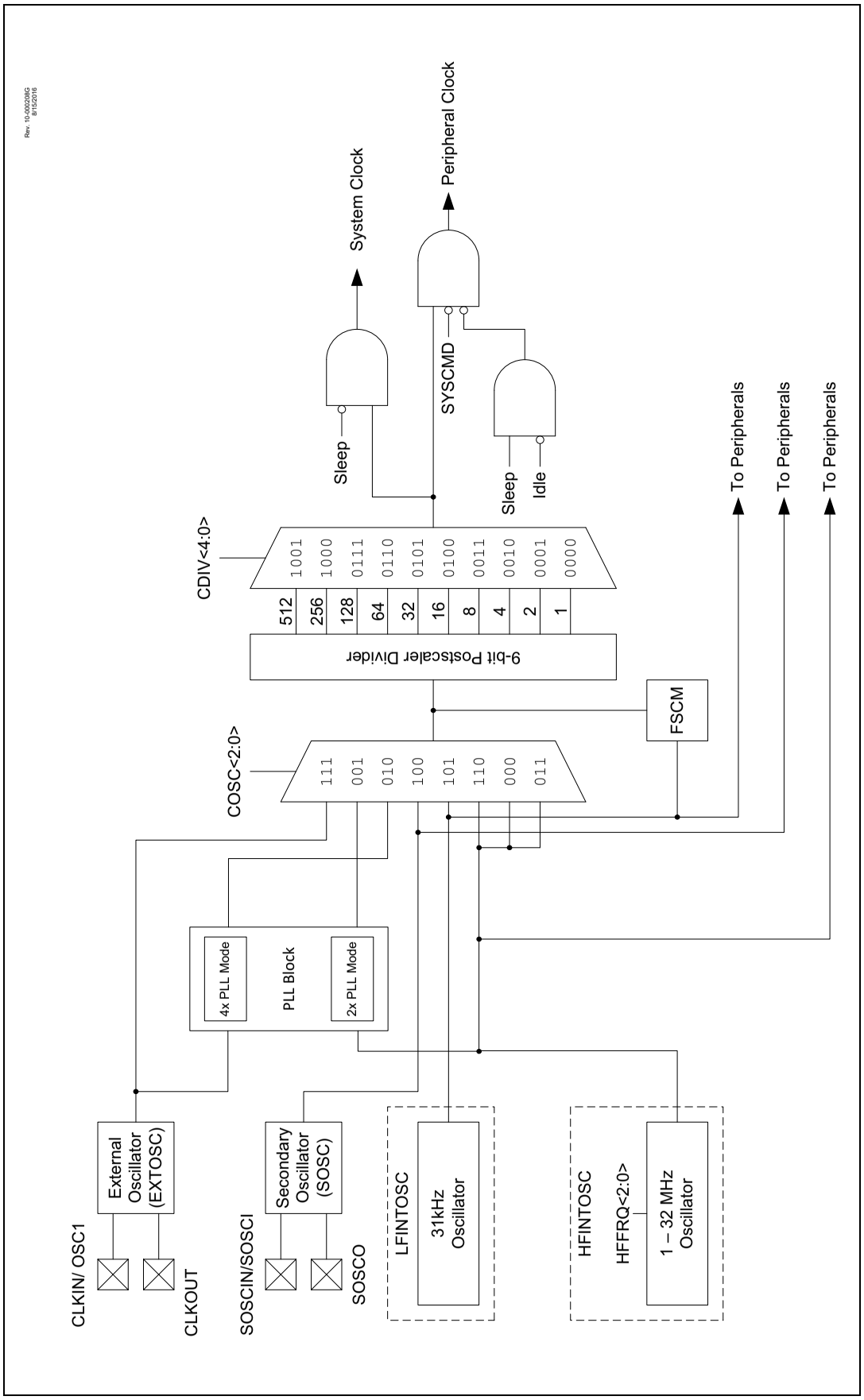
FIGURE 9-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



14.10.6 ANALOG CONTROL

The ANSELE register (Register 14-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELE bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELE bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELE bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.10.7 WEAK PULL-UP CONTROL

The WPUE register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.10.8 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each PORTE pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

TABLE 14-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTE	RE7	RE6	RE5	RE4	RE3	—	RE1	RE0	248
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	—	TRISE1	TRISE0	248
LATE	LATE7	LATE6	LATE5	LATE4	LATE3	—	LATE1	LATE0	249
ANSELE	ANSE7	ANSE6	ANSE5	ANSE4	ANSE3	—	ANSE1	ANSE0	249
WPUE	WPUE7	WPUE6	WPUE5	WPUE4	WPUE3	—	WPUE1	WPUE0	250
ODCONE	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	—	ODCE1	ODCE0	250
SLRCONE	SLRE7	SLRE6	SLRE5	SLRE4	SLRE3	—	SLRE1	SLRE0	251
INLVLE	INLVLE7	INLVLE6	INLVLE5	INLVLE4	INLVLE3	—	INLVLE1	INLVLE0	251

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE.

19.1.5 INTERRUPTS

The ADC module allows the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2:	The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the ADIE bit of the PIEx register and the PEIE bit of the INTCON register must both be set and the GIE bit of the INTCON register must be cleared. If all these bits are set, the PC will jump to the Interrupt Service Routine.

19.1.6 RESULT FORMATTING

The 12-bit ADC conversion result can be supplied in two formats, left justified or right justified. The FM bits of the ADCON0 register controls the output format.

Figure 19-3 shows the two output formats.

Writes to the ADRES register pair are always right justified regardless of the selected format mode. Therefore, data read after writing to ADRES when ADFRM0 = 0 will be shifted left four places.

FIGURE 19-3: 12-BIT ADC CONVERSION RESULT FORMAT

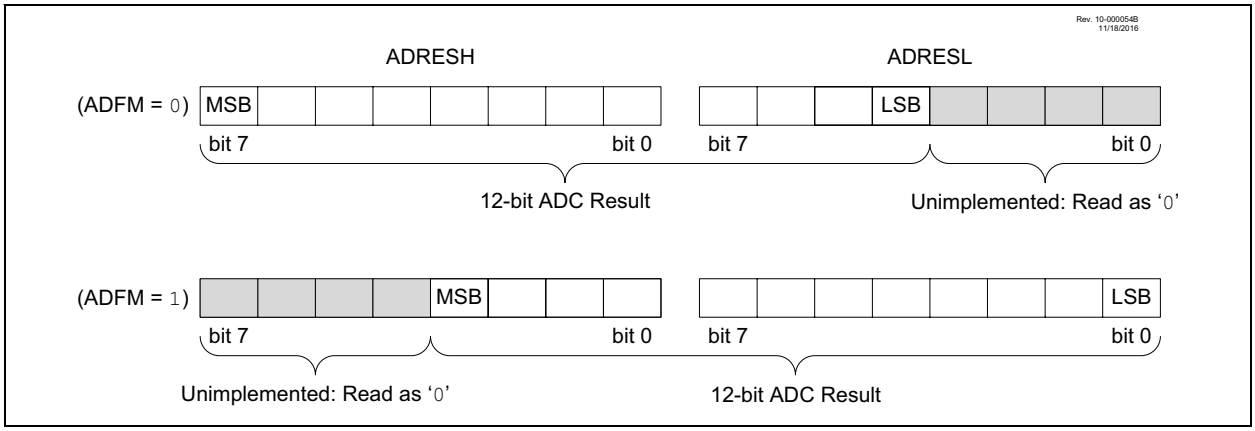
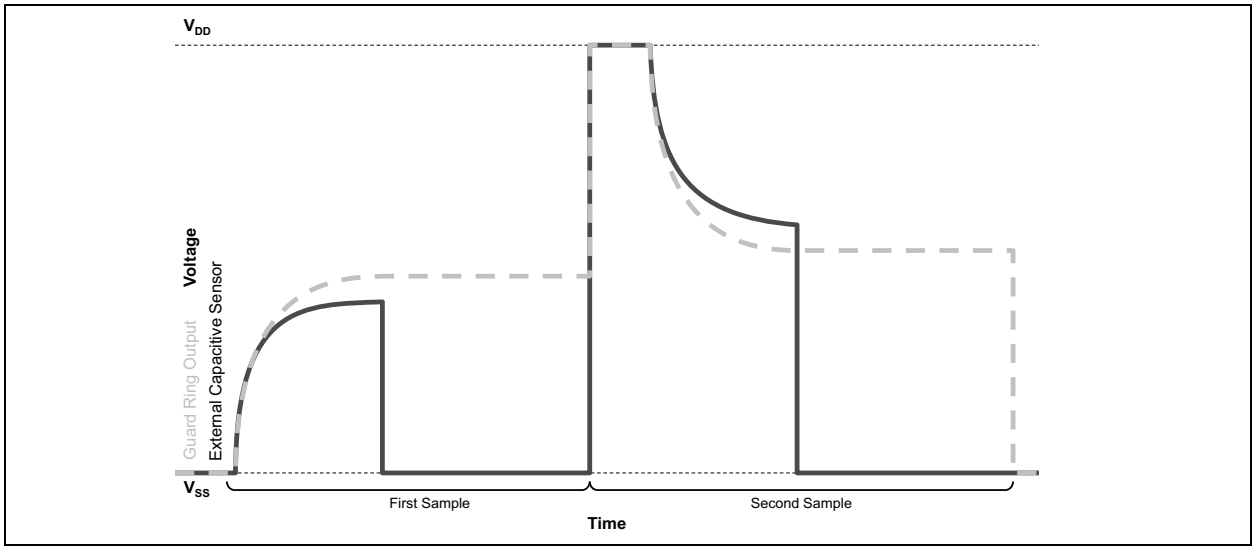


FIGURE 19-9: DIFFERENTIAL CVD WITH GUARD RING OUTPUT WAVEFORM



19.4.5 ADDITIONAL SAMPLE AND HOLD CAPACITANCE

Additional capacitance can be added in parallel with the internal sample and hold capacitor (CHOLD) by using the ADCAP register. This register selects a digitally programmable capacitance which is added to the ADC conversion bus, increasing the effective internal capacitance of the sample and hold capacitor in the ADC module. This is used to improve the match between internal and external capacitance for a better sensing performance. The additional capacitance does not affect analog performance of the ADC because it is not connected during conversion. See Figure 19-10.

REGISTER 19-4: ADCON3: ADC CONTROL REGISTER 3

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0	R/W-0/0	R/W-0/0	R/W-0/0
—	CALC<2:0>			SOI	TMD<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **CALC<2:0>:** ADC Error Calculation Mode Select bits

CALC	DSEN = 0 Single-Sample Mode	DSEN = 1 CVD Double-Sample Mode(1)	Application
111	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
101	FLTR-STPT	FLTR-STPT	Average/filtered value vs. setpoint
100	PREV-FLTR	PREV-FLTR	First derivative of filtered value(3) (negative)
011	Reserved	Reserved	Reserved
010	RES-FLTR	(RES-PREV)-FLTR	Actual result vs. averaged/filtered value
001	RES-STPT	(RES-PREV)-STPT	Actual result vs.setpoint
000	RES-PREV	RES-PREV	First derivative of single measurement(2)
			Actual CVD result in CVD mode(2)

bit 3 **SOI:** ADC Stop-on-Interrupt bit

If CONT = 1:
1 = GO is cleared when the threshold conditions are met, otherwise the conversion is retriggered
0 = GO is not cleared by hardware, must be cleared by software to stop retriggers

bit 2-0 **TMD<2:0>:** Threshold Interrupt Mode Select bits

111 = Interrupt regardless of threshold test results
110 = Interrupt if ERR>UTH
101 = Interrupt if ERR≤UTH
100 = Interrupt if ERR<LTH or ERR>UTH
011 = Interrupt if ERR>LTH and ERR<UTH
010 = Interrupt if ERR≥LTH
001 = Interrupt if ERR<LTH
000 = Never interrupt

Note 1: When PSIS = 0, the value of (RES-PREV) is the value of (S2-S1) from Table 19-2.
2: When ADPSIS = 0.
3: When ADPSIS = 1.

TABLE 19-6: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	166
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
ADCON0	ON	CONT	—	CS	—	FM	—	GO	305
ADCON1	PPOL	IPEN	GPOL	—	—	—	—	DSEN	306
ADCON2	PSIS	CRS<2:0>			ACLR	MD<2:0>			307
ADCON3	—	CALC<2:0>			SOI	TMD<2:0>			308
ADACT	—	—	—	ACT<4:0>					307
ADRESH	ADRESH<7:0>								316, 317
ADRESL	ADRESL<7:0>								316, 317
ADPREVH	PREV<15:8>								318
ADPREVL	PREV<7:0>								318
ADACCU	—	—	—	—	—	—	ACC<16:17>		319
ADACCH	ACC<15:8>								319
ADACCL	ACC<7:0>								319
ADSTPTH	STPT<15:8>								320
ADSTPT	STPT<7:0>								320
ADERRL	ERR<7:0>								321
ADLTHH	LTH<15:8>								321
ADLTHL	LTH<7:0>								321
ADUTHH	UTH<15:8>								322
ADUTHL	UTH<7:0>								322
ADSTAT	OV	UTHR	LTHR	MATH	—	STAT<2:0>			309
ADCLK	—	—	CS<5:0>						310
ADREF	—	—	—	—	—	—	PREF<1:0>		310
ADPCH	—	—	ADPCH<5:0>						311
PRE	PRE<7:0>								312
ADACQ	ADACQ<7:0>								312
ADCAP	—	—	—	ADCAP<4:0>					314
ADRPT	RPT<7:0>								314
ADCNT	CNT<7:0>								315
ADFLTRH	FLTR<15:8>								315
ADFLTRL	FLTR<7:0>								315
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		285
DAC1CON1	—	—	—	DAC1R<4:0>					332
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	155

Legend: – = unimplemented read as '0'. Shaded cells are not used for the ADC module.

25.2 Clock Source Selection

The T0CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 25-2 displays the clock source selections.

25.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

25.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.

25.3 Programmable Prescaler

A software programmable prescaler is available for exclusive use with Timer0. There are 16 prescaler options for Timer0 ranging in powers of two from 1:1 to 1:32768. The prescaler values are selected using the T0CKPS<3:0> bits of the T0CON1 register.

The prescaler is not directly readable or writable. Clearing the prescaler register can be done by writing to the TMR0L register or the T0CON1 register.

25.4 Programmable Postscaler

A software programmable postscaler (output divider) is available for exclusive use with Timer0. There are 16 postscaler options for Timer0 ranging from 1:1 to 1:16. The postscaler values are selected using the T0OUTPS<3:0> bits of the T0CON0 register.

The postscaler is not directly readable or writable. Clearing the postscaler register can be done by writing to the TMR0L register or the T0CON0 register.

25.5 Operation during Sleep

When operating synchronously, Timer0 will halt. When operating asynchronously, Timer0 will continue to increment and wake the device from Sleep (if Timer0 interrupts are enabled) provided that the input clock source is active.

25.6 Timer0 Interrupts

The Timer0 Interrupt Flag bit (TMR0IF) is set when either of the following conditions occur:

- 8-bit TMR0L matches the TMR0H value
- 16-bit TMR0 rolls over from ‘FFFFh’

When the postscaler bits (T0OUTPS<3:0>) are set to 1:1 operation (no division), the T0IF flag bit will be set with every TMR0 match or rollover. In general, the TMR0IF flag bit will be set every T0OUTPS +1 matches or rollovers.

If Timer0 interrupts are enabled (TMR0IE bit of the PIE0 register = 1), the CPU will be interrupted and the device may wake from sleep (see **Section 25.2 “Clock Source Selection”** for more details).

25.7 Timer0 Output

The Timer0 output can be routed to any I/O pin via the RxyPPS output selection register (see **Section 15.0 “Peripheral Pin Select (PPS) Module”** for additional information). The Timer0 output can also be used by other peripherals, such as the Auto-conversion Trigger of the Analog-to-Digital Converter. Finally, the Timer0 output can be monitored through software via the Timer0 output bit (T0OUT) of the T0CON0 register (Register 25-1).

TMR0_out will be one postscaled clock period when a match occurs between TMR0L and TMR0H in 8-bit mode, or when TMR0 rolls over in 16-bit mode. The Timer0 output is a 50% duty cycle that toggles on each TMR0_out rising clock edge.

28.2 SMT Operation

The core of the module is the 24-bit counter, SMTxTMR combined with a complex data acquisition front-end. Depending on the mode of operation selected, the SMT can perform a variety of measurements summarized in Table .

28.2.1 CLOCK SOURCES

Clock sources available to the SMT include:

- FOSC
- FOSC/4
- HFINTOSC
- MFINTOSC (500 kHz and 31.25 kHz)
- LFINTOSC
- SOSC

The SMT clock source is selected by configuring the CSEL<2:0> bits in the SMTxCLK register. The clock source can also be prescaled using the PS<1:0> bits of the SMTxCON0 register. The prescaled clock source is used to clock both the counter and any synchronization logic used by the module.

28.2.2 PERIOD MATCH INTERRUPT

Similar to other timers, the SMT triggers an interrupt when SMTxTMR rolls over to '0'. This happens when SMTxTMR = SMTxPR, regardless of mode. Hence, in any mode that relies on an external signal or a window to reset the timer, proper operation requires that SMTxPR be set to a period larger than that of the expected signal or window.

28.3 Basic Timer Function Registers

The SMTxTMR time base and the SMTxCPW/SMTxPR/SMTxCPR buffer registers serve several functions and can be manually updated using software.

28.3.1 TIME BASE

The SMTxTMR is the 24-bit counter that is the center of the SMT. It is used as the basic counter/timer for measurement in each of the modes of the SMT. It can be reset to a value of 24'h00_0000 by setting the RST bit of the SMTxSTAT register. It can be written to and read from software, but it is not guarded for atomic access, therefore reads and writes to the SMTxTMR should only be made when the GO = 0, or the software should have other measures to ensure integrity of SMTxTMR reads/writes.

28.3.2 PULSE-WIDTH LATCH REGISTERS

The SMTxCPW registers are the 24-bit SMT pulse width latch. They are used to latch in the value of the SMTxTMR when triggered by various signals, which are determined by the mode the SMT is currently in.

The SMTxCPW registers can also be updated with the current value of the SMTxTMR value by setting the CPWUP bit of the SMTxSTAT register.

28.3.3 PERIOD LATCH REGISTERS

The SMTxCPR registers are the 24-bit SMT period latch. They are used to latch in values of the SMTxTMR when triggered by various other signals, which are determined by the mode the SMT is currently in.

The SMTxCPR registers can also be updated with the current value of the SMTxTMR value by setting the CPRUP bit in the SMTxSTAT register.

28.4 Halt Operation

The counter can be prevented from rolling-over using the STP bit in the SMTxCON0 register. When halting is enabled, the period match interrupt persists until the SMTxTMR is reset (either by a manual Reset, **Section 28.3.1 "Time Base"**) or by clearing the SMTxGO bit of the SMTxCON1 register and writing the SMTxTMR values in software.

28.5 Polarity Control

The three input signals for the SMT have polarity control to determine whether or not they are active high/positive edge or active low/negative edge signals.

The following bits apply to Polarity Control:

- WSEL bit (Window Polarity)
- SSEL bit (Signal Polarity)
- CSEL bit (Clock Polarity)

These bits are located in the SMTxCON0 register.

28.6 Status Information

The SMT provides input status information for the user without requiring the need to deal with the polarity of the incoming signals.

28.6.1 WINDOW STATUS

Window status is determined by the WS bit of the SMTxSTAT register. This bit is only used in Windowed Measure, Gated Counter and Gated Window Measure modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

28.6.2 SIGNAL STATUS

Signal status is determined by the AS bit of the SMTxSTAT register. This bit is used in all modes except Window Measure, Time of Flight and Capture modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

REGISTER 31-7: CWG1STR: CWG1 STEERING CONTROL REGISTER(1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OVRD	OVRC	OVRB	OVRA	STRD(2)	STRC(2)	STRB(2)	STRA(2)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **OVRD:** Steering Data D bit

bit 6 **OVRC:** Steering Data C bit

bit 5 **OVRB:** Steering Data B bit

bit 4 **OVRA:** Steering Data A bit

bit 3 **STRD:** Steering Enable D bit(2)

1 = CWG1D output has the CWG1_data waveform with polarity control from POLD bit
0 = CWG1D output is assigned the value of OVRD bit

bit 2 **STRC:** Steering Enable C bit(2)

1 = CWG1C output has the CWG1_data waveform with polarity control from POLC bit
0 = CWG1C output is assigned the value of OVRC bit

bit 1 **STRB:** Steering Enable B bit(2)

1 = CWG1B output has the CWG1_data waveform with polarity control from POLB bit
0 = CWG1B output is assigned the value of OVRB bit

bit 0 **STRA:** Steering Enable A bit(2)

1 = CWG1A output has the CWG1_data waveform with polarity control from POLA bit
0 = CWG1A output is assigned the value of OVRA bit

Note 1: The bits in this register apply only when MODE<2:0> = 00x.

2: This bit is effectively double-buffered when MODE<2:0> = 001.

33.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level (Case 1).
b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 33-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 33-37.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 33-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

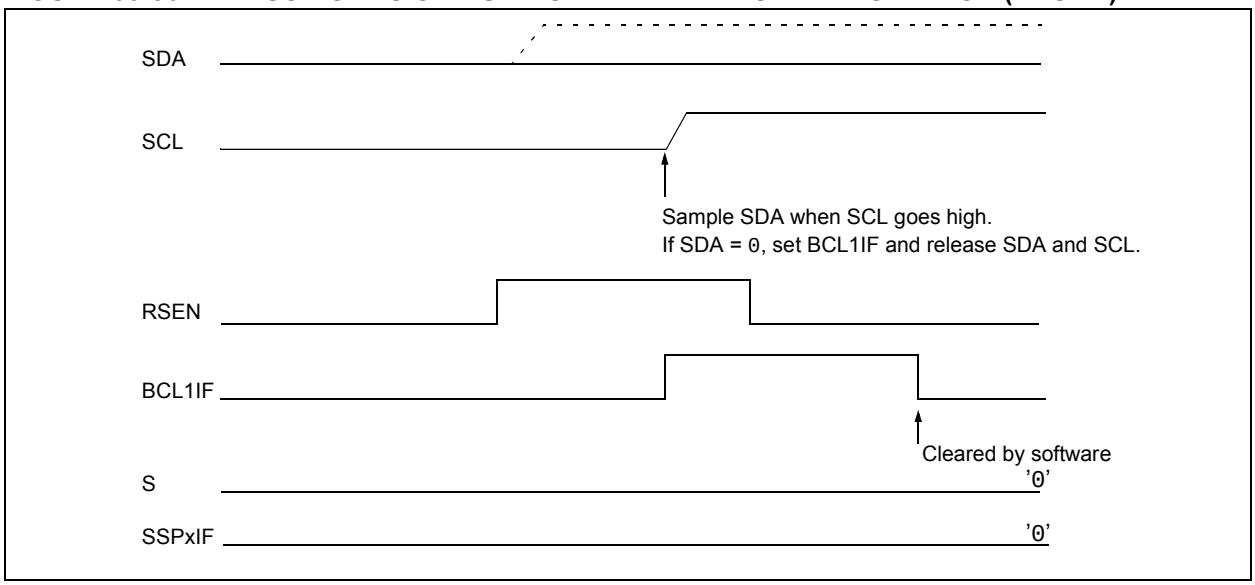
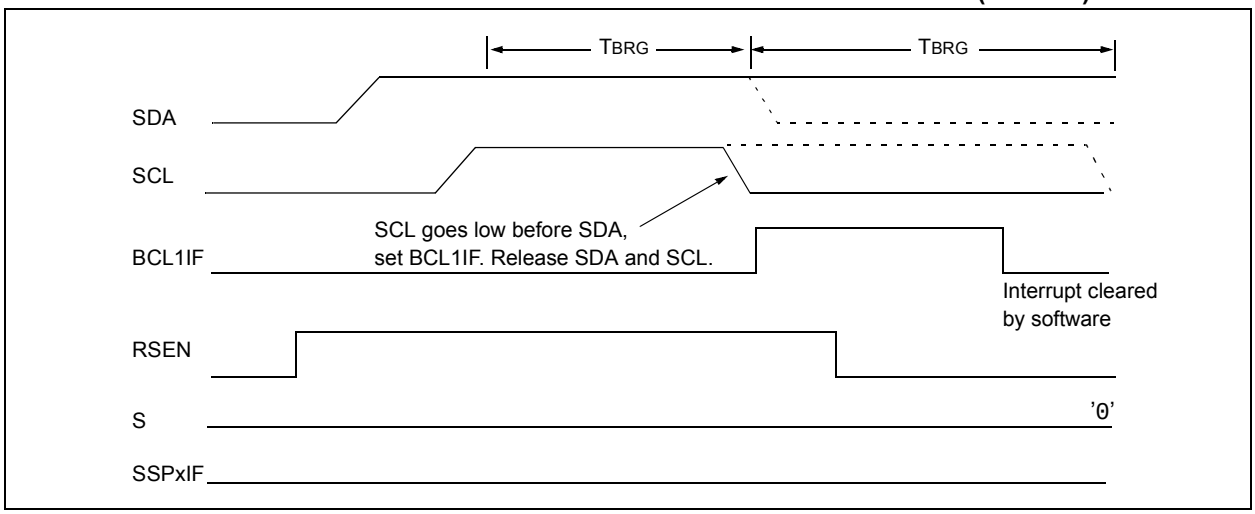


FIGURE 33-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



REGISTER 35-2: LCDPS: LCD PHASE REGISTER

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
WFT	—	LCDA	WA	LP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WFT**: Waveform Type Select bit
1 = Type-B waveform (phase changes on each frame boundary)
0 = Type-A waveform (phase changes within each common type)

bit 6 **Reserved:** Read as '0'

bit 5 **LCDA**: LCD Active Status bit
1 = LCD driver module is active
0 = LCD driver module is inactive

bit 4 **WA**: LCD Write Allow Status bit
This Status bit reflects the value of write_allow signal.
1 = Writes into the LCDDATAx registers are allowed
0 = Writes into the LCDDATAx registers are not allowed

bit 3-0 **LP<3:0>**: LCD Prescaler Select bits
Work with LMUX<3:0> bits to select frame clock prescaler value.
4-Bit Programmable Prescaler = (LP<3:0> + 1)
1111 = 1:16
1110 = 1:15
1101 = 1:14
1100 = 1:13
1011 = 1:12
1010 = 1:11
1001 = 1:10
1000 = 1:9
0111 = 1:8
0110 = 1:7
0101 = 1:6
0100 = 1:5
0011 = 1:4
0010 = 1:3
0001 = 1:2
0000 = 1:1

REGISTER 35-7: LCDRL: LCD INTERNAL REFERENCE LADDER CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
LRLAP1	LRLAP0	LRLBP1	LRLBP0	LCDIRI	LRLAT2	LRLAT1	LRLAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **LRLAP<1:0>**: LCD Reference Ladder A Time Power Control bits

During Time Interval A:

11 = Internal LCD reference is the High-Power (HP) ladder
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 5-4 **LRLBP<1:0>**: LCD Reference Ladder B Time Power Control bits

During Time Interval B:

11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 3 **LCDIRI:** LCD Internal Reference Buffer Idle Enable bit

Allows the Internal reference band gap buffer to shut down when the LCD Reference Ladder is in Power mode 'B'

1 = When the LCD Reference Ladder is in power mode 'B', the LCD Internal Reference Band Gap buffer is disabled
0 = The LCD Internal Reference Buffer ignores the LCD Reference Ladder power mode

bit 2-0 **LRLAT<2:0>**: LCD Reference Ladder A Time Interval Control bits

Sets the number of 32 clock counts when the A Time Interval Power mode is active.

For Type-A Waveforms (WFT = 0):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 9 clocks
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 10 clocks
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 11 clocks
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 12 clocks
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 13 clocks
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 14 clocks
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 15 clocks
000 = Internal LCD reference ladder is always in B Power mode

For Type-B Waveforms (WFT = 1):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 25 clocks
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 26 clocks
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 27 clocks
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 28 clocks
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 29 clocks
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 30 clocks
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 31 clocks
000 = Internal LCD reference ladder is always in B Power mode

MOVWI **Move W to INDFn**

Syntax: [*label*] MOVWI ++FSRn
[*label*] MOVWI --FSRn
[*label*] MOVWI FSRn++
[*label*] MOVWI FSRn--
[*label*] MOVWI k[FSRn]

Operands: $n \in [0,1]$
$mm \in [00, 01, 10, 11]$
$-32 \leq k \leq 31$

Operation: $W \rightarrow INDFn$
Effective address is determined by
- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:
- FSR + 1 (all increments)
- FSR - 1 (all decrements)

Unchanged

Status Affected: None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1

Cycles: 1

Example:

```
NOP
```

RESET **Software Reset**

Syntax: [*label*] RESET

Operands: None

Operation: Execute a device Reset. Resets the $\overline{RI}$ flag of the PCON register.

Status Affected: None

Description: This instruction provides a way to execute a hardware Reset by software.

RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE k

Operands: None

Operation: $TOS \rightarrow PC$,
$1 \rightarrow GIE$

Status Affected: None

Description: Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.

Words: 1

Cycles: 2

Example:

```
RETFIE
```

After Interrupt
PC = TOS
GIE = 1

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

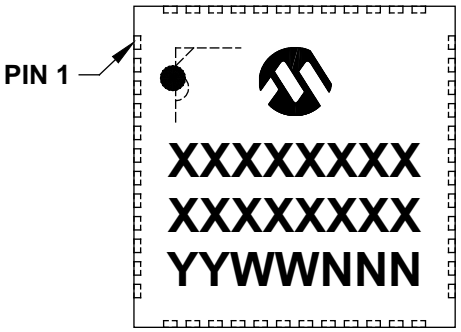
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
212h	—	Unimplemented								
213h	—	Unimplemented								
214h	—	Unimplemented								
215h	—	Unimplemented								
216h	—	Unimplemented								
217h	—	Unimplemented								
218h	—	Unimplemented								
219h	—	Unimplemented								
21Ah	—	Unimplemented								
21Bh	—	Unimplemented								
21Ch	—	Unimplemented								
21Dh	—	Unimplemented								
21Eh	CCPTMRS0	P4TSEL<1:0>		P3TSEL1:0>		C2TSEL<1:0>		C1TSEL<1:0>		461
21Fh	—	Unimplemented								
28Ch	T2TMR	TMR2								
28Dh	T2PR	PR2								
28Eh	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				404
28Fh	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					405
290h	T2CLKCON	—	—	—	—	CS<3:0>				403
291h	T2RST	—	—	—	—	RSEL<3:0>				406
292h	T4TMR	TMR4								
293h	T4PR	PR4								
294h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				404
295h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					405
296h	T4CLKCON	—	—	—	—	CS<3:0>				403
297h	T4RST	—	—	—	—	RSEL<3:0>				406
298h	—	Unimplemented								
299h	—	Unimplemented								
29Ah	—	Unimplemented								
29Bh	—	Unimplemented								
29Ch	—	Unimplemented								
29Dh	—	Unimplemented								
29Eh	—	Unimplemented								
29Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

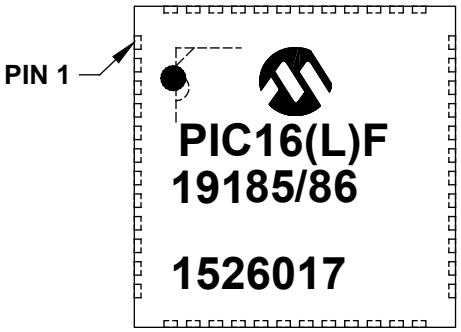
Note 1: Unimplemented data memory locations, read as '0'.

42.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.