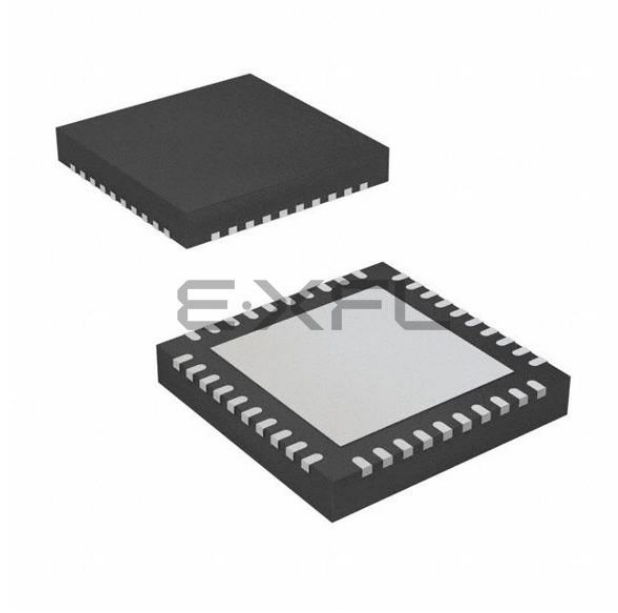

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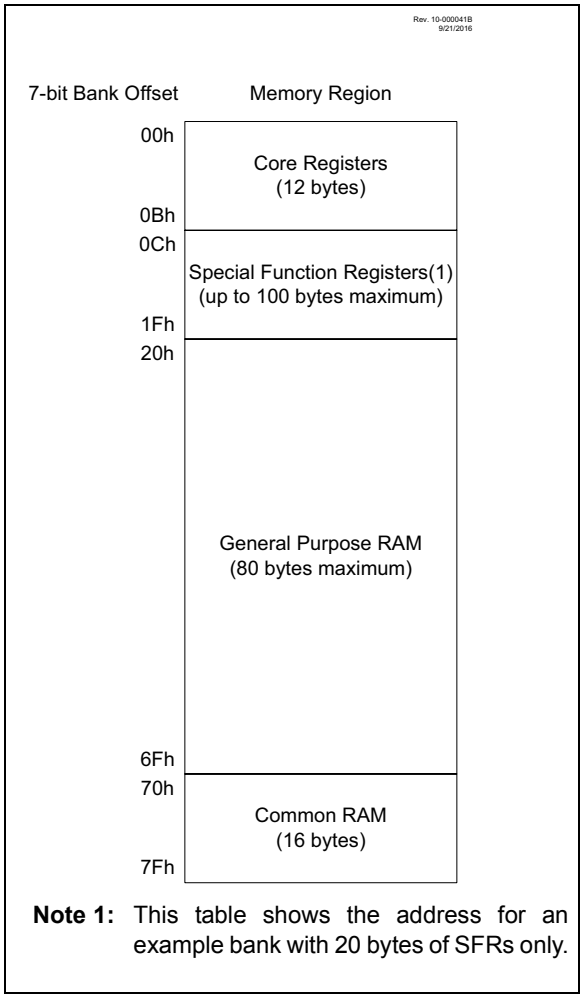
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 31x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19176-e-mv

4.3 Data Memory Organization

The data memory is partitioned into 64 memory banks with 128 bytes in each bank. Each bank consists of (**Section 4.3.6 "Device Memory Maps"**):

FIGURE 4-2: BANKED MEMORY PARTITIONING



Note 1: This table shows the address for an example bank with 20 bytes of SFRs only.

- 12 core registers
- Up to 100 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

4.3.1 BANK SELECTION

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 4.6 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

4.3.2 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 4-3. For detailed information, see Table 4-3.

TABLE 4-3: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 9											
CPU CORE REGISTERS; see Table 4-3 for specifics											
48Ch	SMT1TMRL	SMT1TMR								0000 0000	0000 0000
48Dh	SMT1TMRH	SMT1TMR								0000 0000	0000 0000
48Eh	SMT1TMRU	SMT1TMR								0000 0000	0000 0000
48Fh	SMT1CPRL	CPR								xxxx xxxx	xxxx xxxx
490h	SMT1CPRH	CPR								xxxx xxxx	xxxx xxxx
491h	SMT1CPRU	CPR								xxxx xxxx	xxxx xxxx
492h	SMT1CPWL	CPW								xxxx xxxx	xxxx xxxx
493h	SMT1CPWH	CPW								xxxx xxxx	xxxx xxxx
494h	SMT1CPWU	CPW								xxxx xxxx	xxxx xxxx
495h	SMT1PRL	SMT1PR								1111 1111	1111 1111
496h	SMT1PRH	SMT1PR								1111 1111	1111 1111
497h	SMT1PRU	SMT1PR								1111 1111	1111 1111
498h	SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		0-00 0000	0-00 0000
499h	SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				00-- 0000	00-- 0000
49Ah	SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	000- -000	000- -000
49Bh	SMT1CLK	—	—	—	—	—	CSEL<2:0>			0000 0000	0000 0000
49Ch	SMT1SIG	—	—	—	SSEL<4:0>					0000 0000	0000 0000
49Dh	SMT1WIN	—	—	—	WSEL<4:0>					0000 0000	0000 0000
49Eh	—	Unimplemented								---- ----	---- ----
49Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Banks 25-28											
CPU CORE REGISTERS; see Table 4-3 for specifics											
C8Ch — C9Fh	—	Unimplemented								---- ----	---- ----
D0Ch — D1Fh	—	Unimplemented								---- ----	---- ----
D8Ch — D9Fh	—	Unimplemented								---- ----	---- ----
E0Ch — E1Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

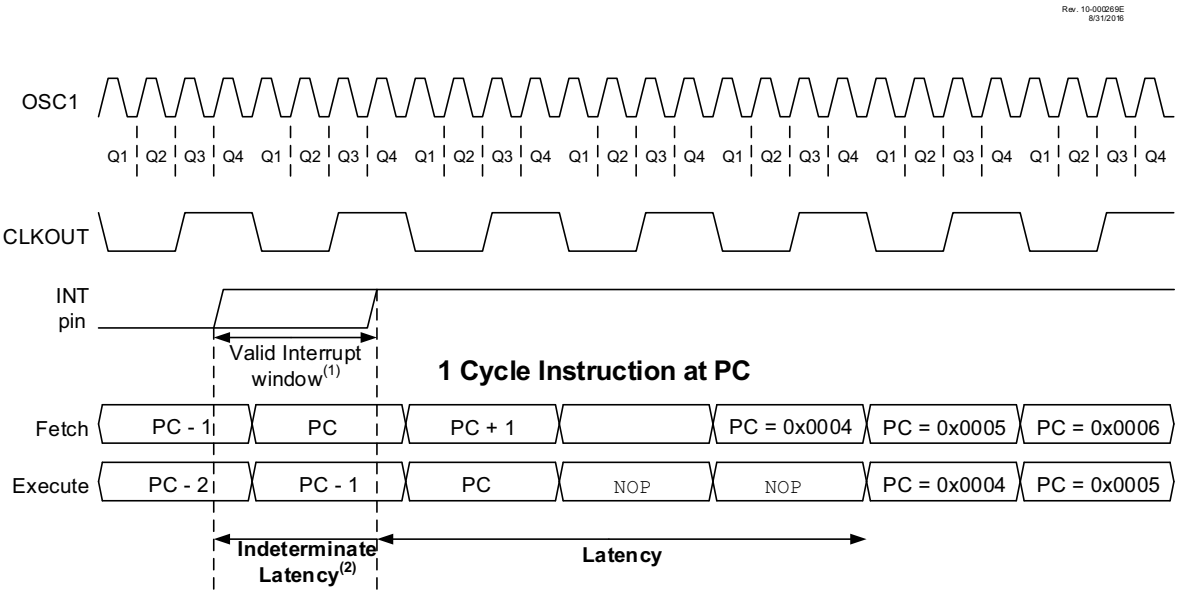
TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 29											
CPU CORE REGISTERS; see Table 4-3 for specifics											
E8Ch	VB0GPR	VB0GPR								0000 0000	uuuu uuuu
E8Dh	VB1GPR	VB1GPR								0000 0000	uuuu uuuu
E8Eh	VB2GPR	VB2GPR								0000 0000	uuuu uuuu
E8Fh	VB3GPR	VB3GPR								0000 0000	uuuu uuuu
E90h	—	Unimplemented								---- ----	---- ----
E91h	—	Unimplemented								---- ----	---- ----
E92h	—	Unimplemented								---- ----	---- ----
E93h	—	Unimplemented								---- ----	---- ----
E94h	—	Unimplemented								---- ----	---- ----
E95h	—	Unimplemented								---- ----	---- ----
E96h	—	Unimplemented								---- ----	---- ----
E97h	—	Unimplemented								---- ----	---- ----
E98h	—	Unimplemented								---- ----	---- ----
E99h	—	Unimplemented								---- ----	---- ----
E9Ah	—	Unimplemented								---- ----	---- ----
E9Bh	—	Unimplemented								---- ----	---- ----
E9Ch	—	Unimplemented								---- ----	---- ----
E9Dh	—	Unimplemented								---- ----	---- ----
E9Eh	—	Unimplemented								---- ----	---- ----
E9Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

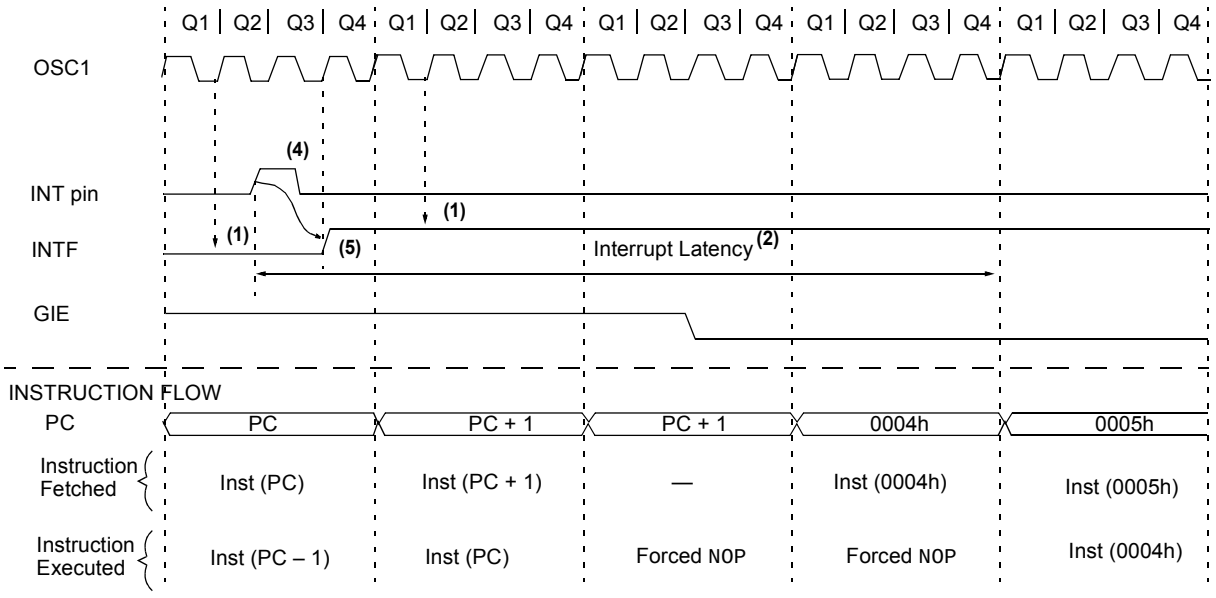
Note 1: Unimplemented data memory locations, read as '0'.

FIGURE 10-2: INTERRUPT LATENCY



Note 1: An interrupt may occur at any time during the interrupt window.
2: Since an interrupt may occur any time during the interrupt window, the actual latency can vary.

FIGURE 10-3: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: For minimum width of INT pulse, refer to AC specifications in **Section 39.0 "Electrical Specifications"**.

4: INTF is enabled to be set any time during the Q4-Q1 cycles.

REGISTER 10-5: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **RC2IE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Enables the USART receive interrupt

bit 6 **TX2IE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 5 **RC1IE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Enables the USART receive interrupt

bit 4 **TX1IE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **BCL1IE:** MSSP1 Bus Collision Interrupt Enable bit
1 = MSSP bus collision interrupt enabled
0 = MSSP bus collision interrupt disabled

bit 0 **SSP1IE:** Synchronous Serial Port (MSSP1) Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by PIE1-PIE8.

14.2 PORTA Registers

14.2.1 DATA REGISTER

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 14-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 14.2.8 shows how to initialize PORTA.

Reading the PORTA register (Register 14-1) reads the status of the pins, whereas writing to it will write to the PORT latch.

The PORT data latch LATA (Register 14-3) holds the output port data, and contains the latest value of a LATA or PORTA write.

EXAMPLE 14-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL  PORTA        ;
CLRF     PORTA        ;Init PORTA
BANKSEL  LATA         ;Data Latch
CLRF     LATA         ;
BANKSEL  ANSELA       ;
CLRF     ANSELA       ;digital I/O
BANKSEL  TRISA        ;
MOVLW    B'00111000'  ;Set RA<5:3> as inputs
MOVWF    TRISA        ;and set RA<2:0> as
                      ;outputs
```

14.2.2 DIRECTION CONTROL

The TRISA register (Register 14-2) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

14.2.3 OPEN-DRAIN CONTROL

The ODCONA register (Register 14-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note:	It is not necessary to set open-drain control when using the pin for I^2C; the I^2C module controls the pin and makes the pin open-drain.

14.2.4 SLEW RATE CONTROL

The SLRCONA register (Register 14-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

REGISTER 19-18: ADRESH: ADC RESULT REGISTER HIGH, FM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<11:4>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADRES<11:4>**: ADC Result Register bits
Upper eight bits of 12-bit conversion result.

REGISTER 19-19: ADRESL: ADC RESULT REGISTER LOW, FM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
ADRES<3:0>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **ADRES<3:0>**: ADC Result Register bits. Lower four bits of 12-bit conversion result.
bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 19-33: ADUTHH: ADC UPPER THRESHOLD HIGH BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
UTH<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **UTH<15:8>**: ADC Upper Threshold MSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

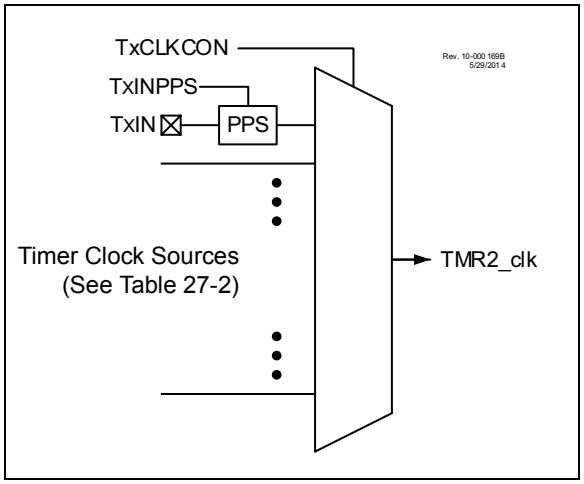
REGISTER 19-34: ADUTHL: ADC UPPER THRESHOLD LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
UTH<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **UTH<7:0>**: ADC Upper Threshold LSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

FIGURE 27-2: TIMER2/4 CLOCK SOURCE BLOCK DIAGRAM



27.1 Timer2/4 Operation

Timer2 operates in three major modes:

- Free Running Period
- One-shot
- Monostable

Within each mode there are several options for starting, stopping, and reset. Table 27-1 lists the options.

In all modes, the TMR2 count register is incremented on the rising edge of the clock signal from the programmable prescaler. When TMR2 equals T2PR, a high level is output to the postscaler counter. TMR2 is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a TMR2 count Reset. In Gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the TMR2 count is reset on either the level or edge from the external source.

The TMR2 and T2PR registers are both directly readable and writable. The TMR2 register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset
- External Reset Source event that resets the timer.

Note:	TMR2 is not cleared when T2CON is written.

27.1.1 FREE RUNNING PERIOD MODE

The value of TMR2 is compared to that of the Period register, T2PR, on each TMR2_clk cycle. When the two values match, the comparator resets the value of TMR2 to 00h on the next rising TMR2_clk edge and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS<4:0> bits of the TMRxCON1 register, a one TMR2_clk period wide pulse occurs on the TMR2_postscaled output, and the postscaler count is cleared.

27.1.2 ONE-SHOT MODE

The One-Shot mode is identical to the Free Running Period mode except that the ON bit is cleared and the timer is stopped when TMR2 matches T2PR and will not restart until the T2ON bit is cycled off and on. Postscaler OUTPS<4:0> values other than 0 are meaningless in this mode because the timer is stopped at the first period event and the postscaler is reset when the timer is restarted.

27.1.3 MONOSTABLE MODE

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

27.2 Timer2/4 Output

The Timer2 module's primary output is TMR2_postscaled, which pulses for a single TMR2_clk period when the postscaler counter matches the value in the OUTPS bits of the TMR2CON register. The T2PR postscaler is incremented each time the TMR2 value matches the T2PR value. This signal can be selected as an input to several other input modules:

- The ADC module, as an Auto-conversion Trigger
- COG, as an auto-shutdown source

In addition, the Timer2 is also used by the CCP module for pulse generation in PWM mode. Both the actual TMR2 value as well as other internal signals are sent to the CCP module to properly clock both the period and pulse width of the PWM signal. See **Section 29.0 "Capture/Compare/PWM Modules"** for more details on setting up Timer2/4 for use with the CCP, as well as the timing diagrams in **Section 27.5 "Operation Examples"** for examples of how the varying Timer2 modes affect CCP PWM output.

27.3 External Reset Sources

In addition to the clock source, the Timer2 also takes in an external Reset source. This external Reset source is selected for Timer2 with the T2RST register. This source can control starting and stopping of the timer, as well as resetting the timer, depending on which mode the timer is in. The mode of the timer is controlled by the MODE<4:0> bits of the TMRxHLT register. Edge-Triggered modes require six Timer clock periods between external triggers. Level-Triggered modes require the triggering level to be at least three Timer clock periods long. External triggers are ignored while in Debug Freeze mode.

REGISTER 28-6: SMTxSIG: SMTx SIGNAL INPUT SELECT REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	SSEL<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented**: Read as '0'

bit 4-0 **SSEL<4:0>:** SMTx Signal Selection bits
11111 = Reserved
•
•
•
10001 = Reserved
10000 = RTCC_Seconds
01111 = CLC4OUT
01110 = CLC3OUT
01101 = CLC2OUT
01100 = CLC1OUT
01011 = ZCDOUT
01010 = C2OUT
01001 = C1OUT
01000 = PWM4_out
00111 = PWM3_out
00110 = CCP2OUT
00101 = CCP1OUT
00100 = TMR4_postscaler
00011 = TMR2_postscaler
00010 = TMR1_overflow
00001 = TMR0_overflow
00000 = SMTSIG pin

28.8 Interrupts

The SMT can trigger an interrupt under three different conditions:

- PW Acquisition Complete
- PR Acquisition Complete
- Counter Period Match

The interrupts are controlled by the PIR8 and PIE8 registers of the device.

28.8.1 PW AND PR ACQUISITION INTERRUPTS

The SMT can trigger interrupts whenever it updates the SMTxCPW and SMTxCPR registers, the circumstances for which are dependent on the SMT mode, and are discussed in each mode's specific section. The SMTxCPW interrupt is controlled by SMTxPWAIF and SMTxPWAIE bits in registers PIR8 and PIE8, respectively. The SMTxCPR interrupt is controlled by the SMTxPRAIF and SMTxPRAIE bits, also located in registers PIR8 and PIE8, respectively.

In Synchronous SMT modes, the interrupt trigger is synchronized to the SMTxCLK. In Asynchronous modes, the interrupt trigger is asynchronous. In either mode, once triggered, the interrupt will be synchronized to the CPU clock.

28.8.2 COUNTER PERIOD MATCH INTERRUPT

As described in **Section 28.2.2 "Period Match interrupt"**, the SMT will also interrupt upon SMTxTMR, matching SMTxPR with its period match limit functionality described in **Section 28.4 "Halt Operation"**. The period match interrupt is controlled by SMTxIF and SMTxIE.

TABLE 28-3: SUMMARY OF REGISTERS ASSOCIATED WITH SMTx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182
SMT1CLK	—	—	—	—	—	CSEL<2:0>			413
SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		410
SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				411
SMT1CPRH	SMT1CPR<15:8>								417
SMT1CPRL	SMT1CPR<7:0>								417
SMT1CPRU	SMT1CPR<23:16>								417
SMT1CPWH	SMT1CPW<15:8>								418
SMT1CPWL	SMT1CPW<7:0>								418
SMT1CPWU	SMT1CPW<23:16>								418
SMT1PRH	SMT1PR<15:8>								419
SMT1PRL	SMT1PR<7:0>								419
SMT1PRU	SMT1PR<23:16>								419
SMT1SIG	—	—	—	SSEL<4:0>					415
SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	412
SMT1TMRH	SMT1TMR<15:8>								416
SMT1TMRL	SMT1TMR<7:0>								416
SMT1TMRU	SMT1TMR<23:16>								416
SMT1WIN	—	—	—	WSEL<4:0>					414

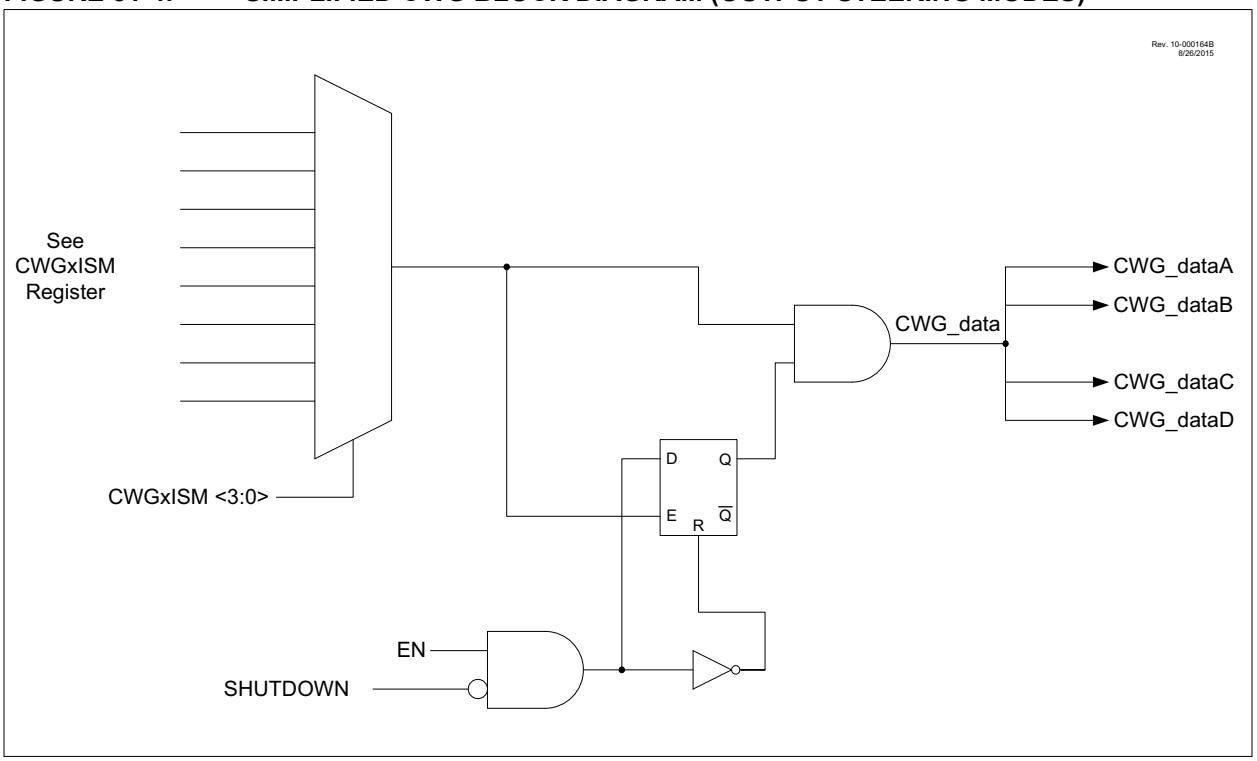
Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for SMTx module.

31.1.4 STEERING MODES

In Steering modes, the data input can be steered to any or all of the four CWG output pins. In Synchronous Steering mode, changes to steering selection registers take effect on the next rising input.

In Non-Synchronous mode, steering takes effect on the next instruction cycle. Additional details are provided in **Section 31.9 "CWG Steering Mode"**.

FIGURE 31-4: SIMPLIFIED CWG BLOCK DIAGRAM (OUTPUT STEERING MODES)



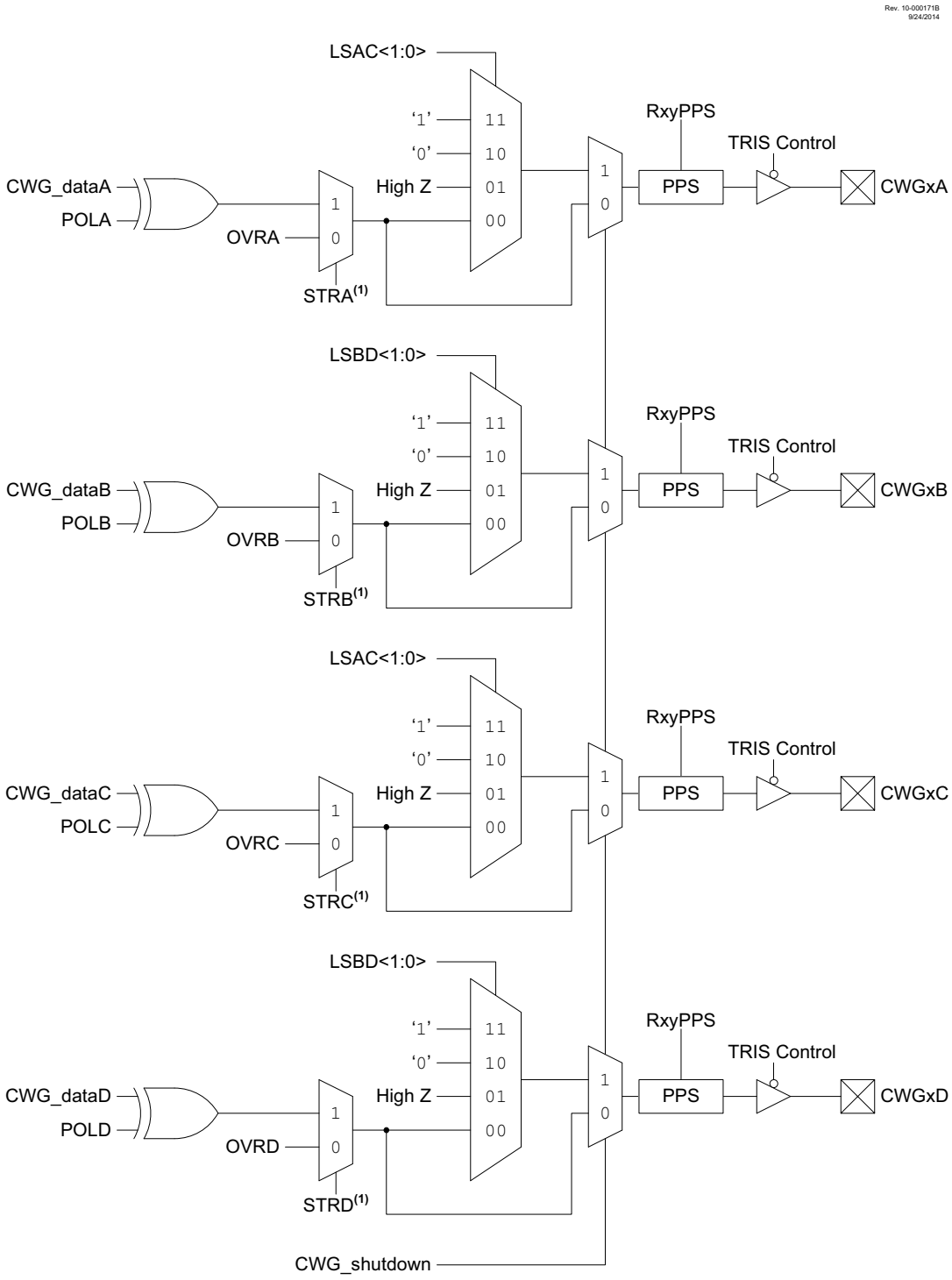
31.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the CS bit of the CWG1CLKCON register.

FIGURE 31-5: CWG OUTPUT BLOCK DIAGRAM



Note 1: STRx is held to 1 in all modes other than Output Steering Mode.

32.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

32.1.1 DATA SELECTION

There are 40 signals available as inputs to the configurable logic. Four 40-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 32-2. Data inputs in the figure are identified by a generic numbered input name.

Table 32-2 correlates the generic input name to the actual signal for each CLC module. The column labeled 'LCxDyS<5:0> Value' indicates the MUX selection code for the selected data input. LCxDyS is an abbreviation to identify specific multiplexers: LCxD1S<5:0> through LCxD4S<5:0>.

Data inputs are selected with CLCxSEL0 through CLCxSEL3 registers (Register 32-3 through Register 32-6).

TABLE 32-2: CLCx DATA INPUT SELECTION

LCxDyS<5:0> Value	CLCx Input Source
100101 to 111111	Reserved
100100	EUSART2 (TX/CK) output
100011	EUSART2 (DT) output
100010	CWG1B output
100001	CWG1A output
100000	RTCC seconds
011111	MSSP1 SCK output
011110	MSSP1 SDO output
011101	EUSART1 (TX/CK) output
011100	EUSART1 (DT) output
011011	CLC4 output
011010	CLC3 output
011001	CLC2 output
011000	CLC1 output
010111	IOCIF
010110	ZCD output
010101	C2OUT
010100	C1OUT
010011	PWM4 output
010010	PWM3 output
010001	CCP2 output
010000	CCP1 output
001111	SMT overflow
001110	Timer4 overflow
001101	Timer2 overflow
001100	Timer1 overflow
001011	Timer0 overflow
001010	ADCRC
001001	SOSC
001000	MFINTOSC (32 kHz)
000111	MFINTOSC (500 kHz)
000110	LFINTOSC
000101	HFINTOSC
000100	FOSC
000011	CLCIN3PPS
000010	CLCIN2PPS
000001	CLCIN1PPS
000000	CLCIN0PPS

FIGURE 33-7: SPI DAISY-CHAIN CONNECTION

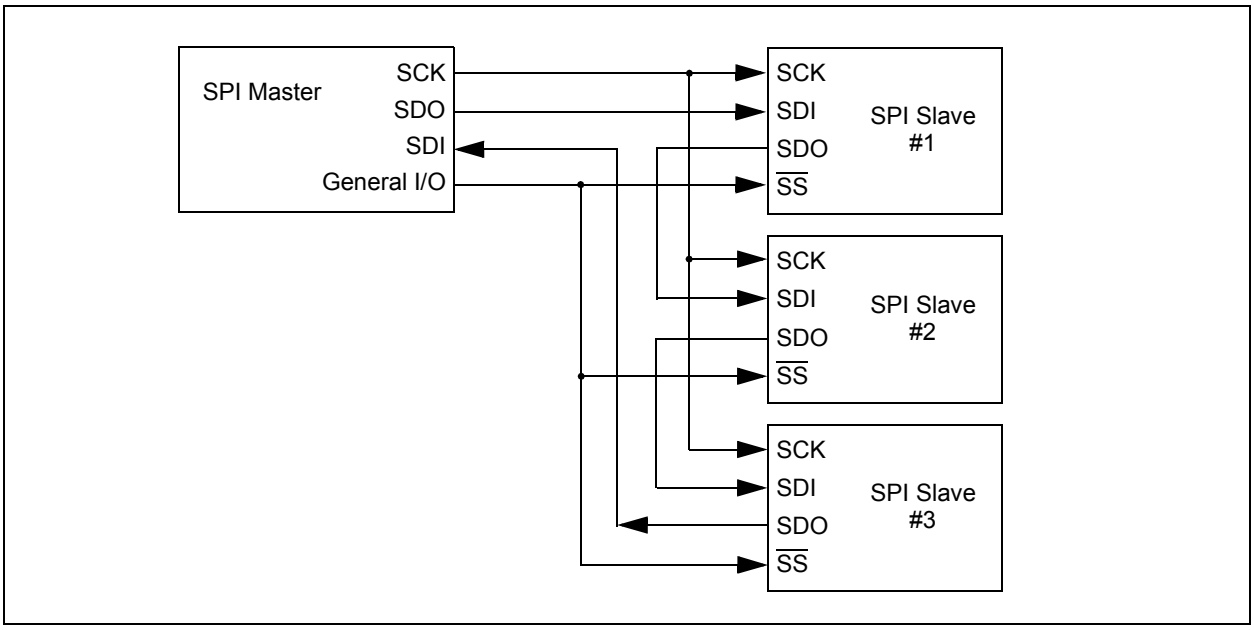


FIGURE 33-8: SLAVE SELECT SYNCHRONOUS WAVEFORM

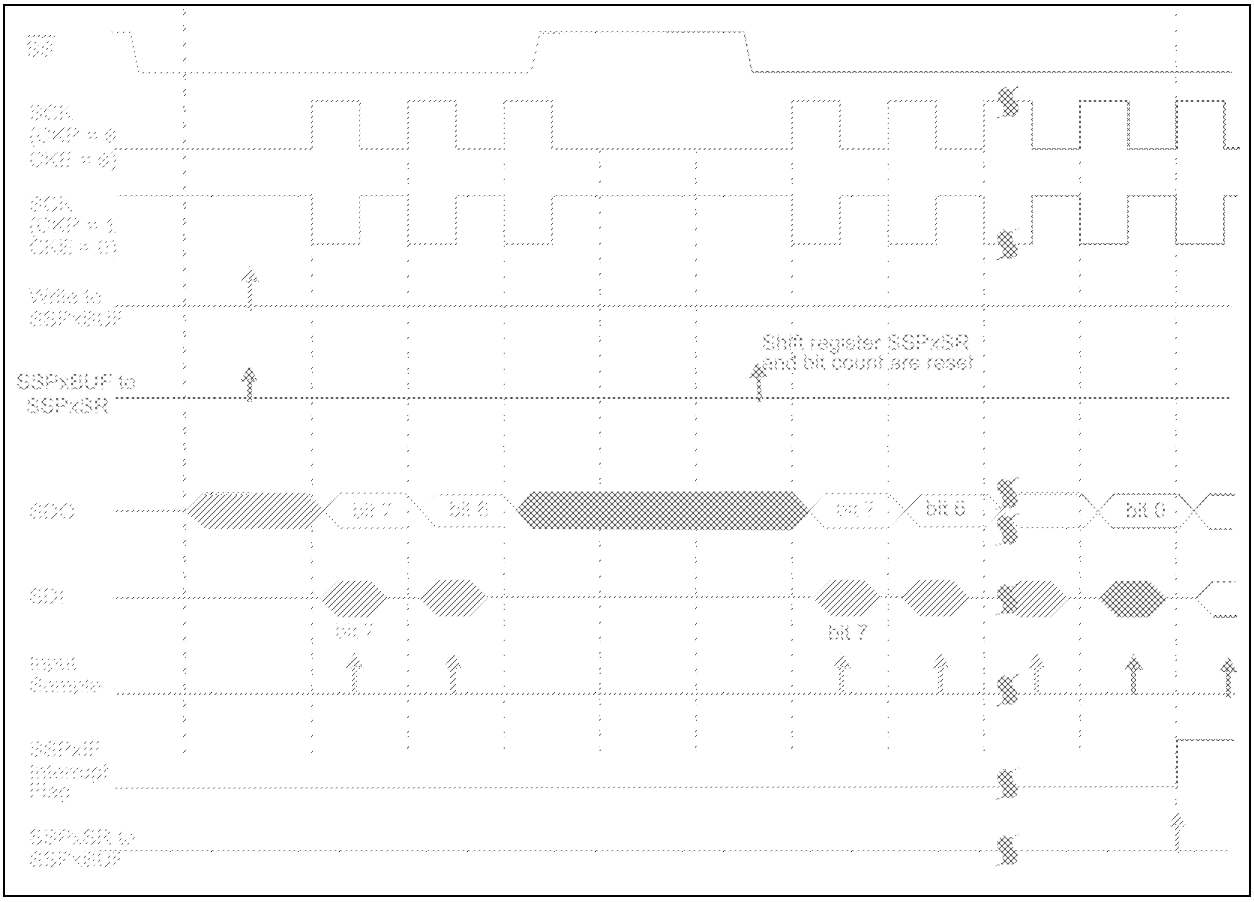


FIGURE 33-34: BUS COLLISION DURING START CONDITION (SCL = 0)

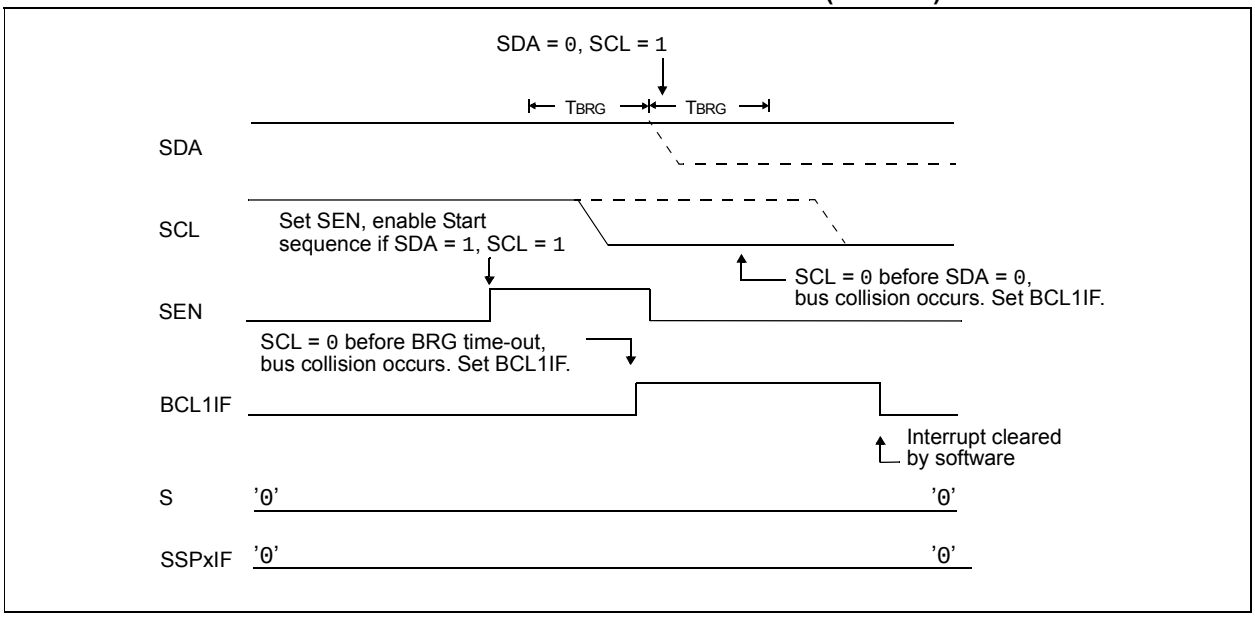


FIGURE 33-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION

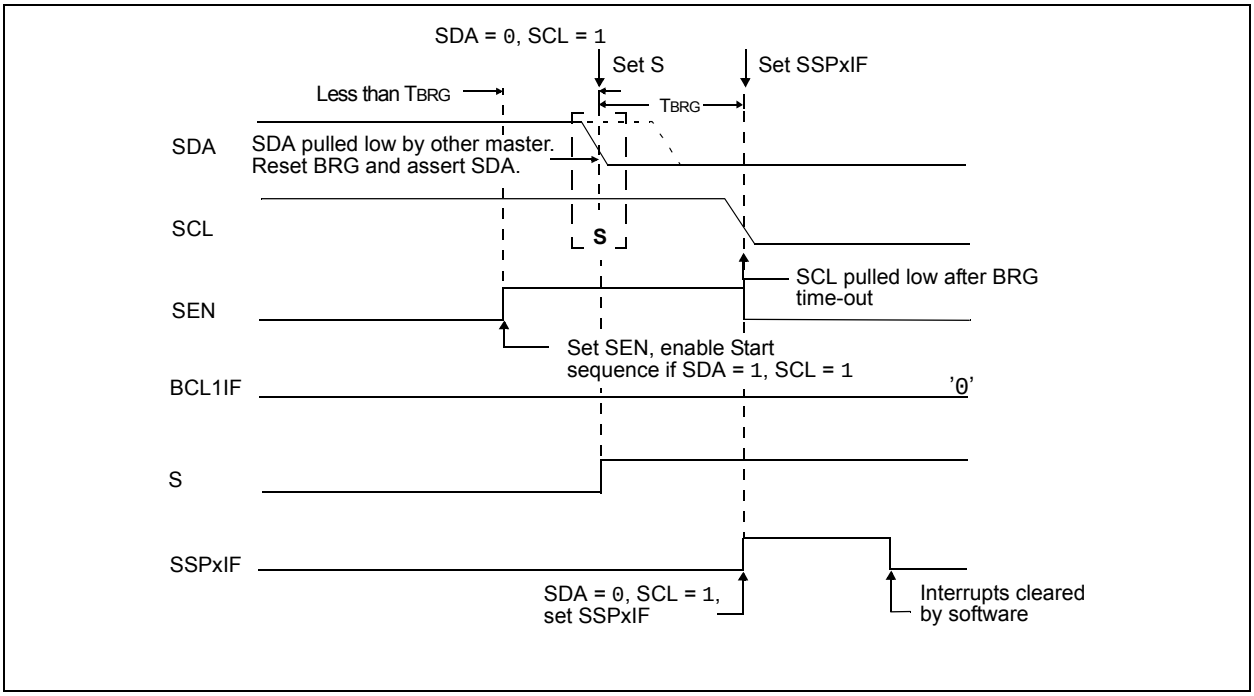


FIGURE 35-13: TYPE-A WAVEFORMS IN 1/3 MUX, 1/2 BIAS DRIVE

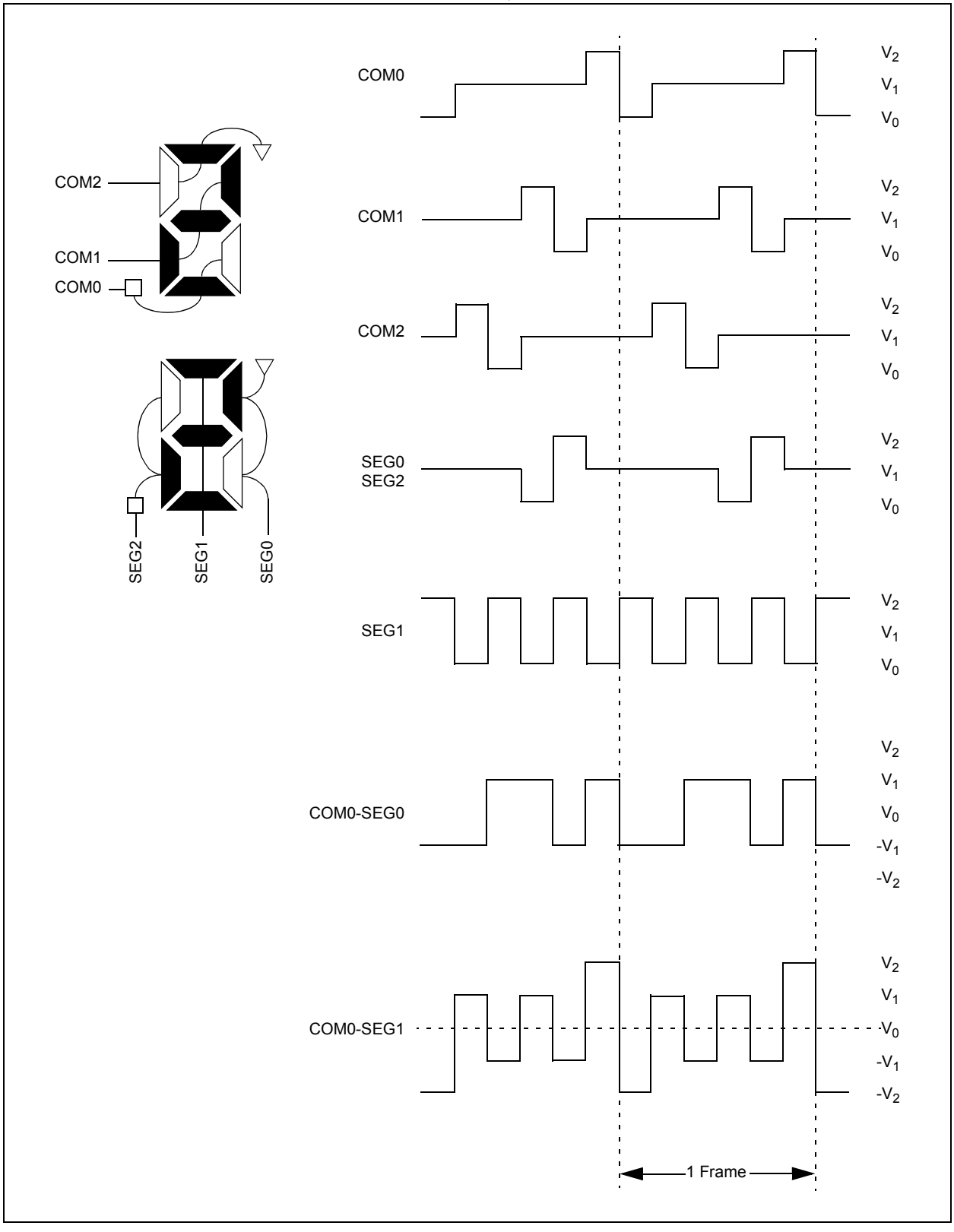
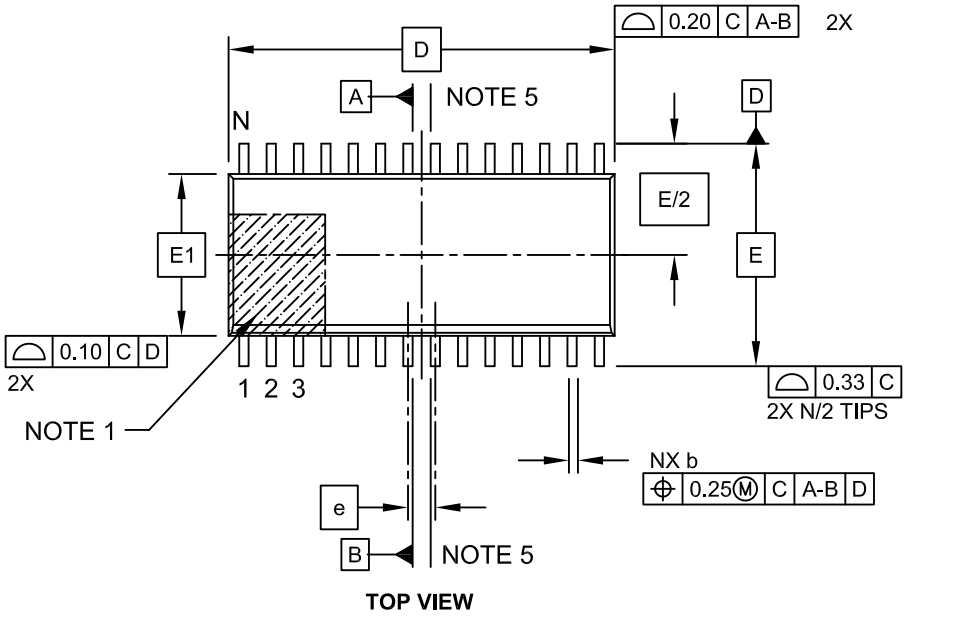


TABLE 35-10: SUMMARY OF REGISTERS ASSOCIATED WITH LCD MODULE (CONTINUED)

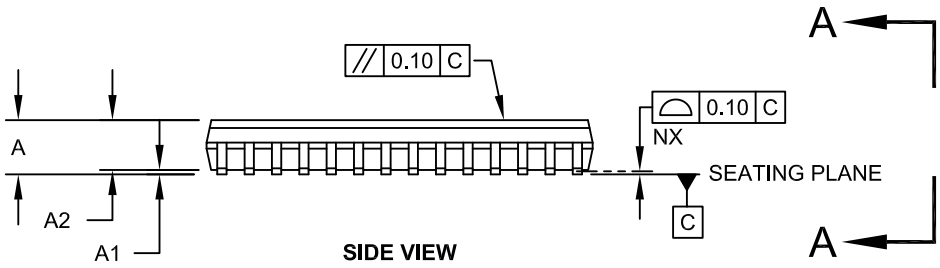
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
LCDDATA34	S47C5	S46C5	S45C5	S44C5	S43C5	S42C5	S41C5	S40C5	624
LCDDATA35	S07C6	S06C6	—	S04C6	S03C6	S02C6	S01C6	S00C6	624
LCDDATA36	S15C6	S14C6	S13C6	—	S11C6	S10C6	S09C6	S08C6	624
LCDDATA37	S23C6	S22C6	—	S20C6	S19C6	S18C6	—	—	624
LCDDATA38	S31C6	S30C6	S29C6	S28C6	S27C6	S26C6	S25C6	S24C6	624
LCDDATA39	—	—	—	—	—	S34C6	S33C6	S32C6	624
LCDDATA40	S47C6	S46C6	S45C6	S44C6	S43C6	S42C6	S41C6	S40C6	624
LCDDATA41	S07C7	S06C7	—	S04C7	S03C7	S02C7	S01C7	S00C7	624
LCDDATA42	S15C7	S14C7	S13C7	—	S11C7	S10C7	S09C7	S08C7	624
LCDDATA43	S23C7	S22C7	—	S20C7	S19C7	S18C7	—	—	624
LCDDATA44	S31C7	S30C7	S29C7	S28C7	S27C7	S26C7	S25C7	S24C7	624
LCDDATA45	—	—	—	—	—	S34C7	S33C7	S32C7	624
LCDDATA46	S47C7	S46C7	S45C7	S44C7	S43C7	S42C7	S41C7	S40C7	624
LCDDATA47	S07C0	S06C0	—	S04COM0	S03C0	S02C0	S01C0	S00C0	624

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

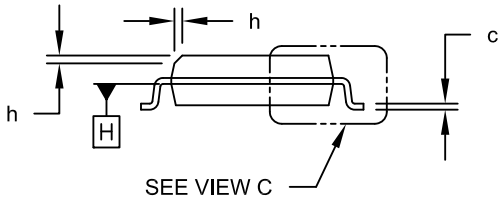
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2