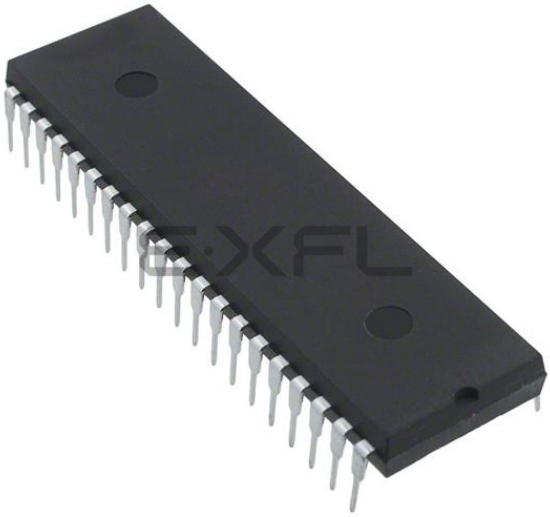

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 31x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19176-e-p

TABLE 1-3: PIC16(L)F19175/76 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/SS(1)/IOCA5/VBAT	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	SS(1)	TTL/ST	—	MSSP SPI slave select input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.
	VBAT	AN	—	RTCC Back-up Battery.
RA6/ANA6/IOCA6/SEG6/CLKOUT	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN	—	ADC Channel input.
	IOCA6	—	—	Interrupt-on-change input.
	SEG6	—	AN	LCD Analog output.
	CLKOUT	TTL/ST	—	FOSC/4 digital output.
RA7/ANA7/SEG7/CLKIN	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN	—	ADC Channel input.
	SEG7	—	AN	LCD Analog output.
	CLKIN	ST	—	External Clock driver input.
RB0/CWG1IN(1)/C2IN1+/IOCB0/ANB0/SEG8/ZCD	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	CWG1IN(1)	TTL/ST	—	Complementary Waveform Generator input
	C2IN1+	AN	—	Comparator positive input.
	IOCB0	TTL/ST	—	Interrupt-on-change input.
	ANB0	AN	—	ADC Channel input.
	SEG8	—	AN	LCD Analog output.
	ZCD	—	—	Zero-cross detect input pin (with constant current sink/source).
RB1/C1IN3-/C2IN3-/IOCB1/SCL(3,4)/SCK(1)/ANB1/HIB1/SEG9	RB1	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.
	IOCB1	TTL/ST	—	Interrupt-on-change input.
	SCL(3,4)	I^2C	OD	MSSP I^2Cclock input/output.
	SCK(1)	TTL/ST	—	MSSP SPI clock input/output.
	ANB1	AN	—	ADC Channel input.
	HIB1	TTL/ST	—	High current output.
	SEG9	—	AN	LCD Analog output.
RB2/IOCB2/SDA(3,4)/SDI(1)/ANB2/SEG10/SEGCFLY1	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB2	TTL/ST	—	Interrupt-on-change input.
	SDA(3,4)	I^2C	OD	MSSP I^2C data input/output.
	SDI(1)	TTL/ST	—	MSSP SPI serial data in.
	ANB2	AN	—	ADC Channel input.
	SEG10	—	AN	LCD Analog output.
	SEGCFLY1	AN	—	LCD Drive Charge Pump Capacitor Inputs

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 5											
CPU CORE REGISTERS; see Table 4-3 for specifics											
28Ch	T2TMR	TMR2								0000 0000	0000 0000
28Dh	T2PR	PR2								1111 1111	1111 1111
28Eh	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
28Fh	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
290h	T2CLKCON	—	—	—	—	CS<3:0>				0000 0000	0000 0000
291h	T2RST	—	—	—	—	RSEL<3:0>				0000 0000	0000 0000
292h	T4TMR	TMR4								0000 0000	0000 0000
293h	T4PR	PR4								1111 1111	1111 1111
294h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
295h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
296h	T4CLKCON	—	—	—	—	CS<3:0>				0000 0000	0000 0000
297h	T4RST	—	—	—	—	RSEL<3:0>				0000 0000	0000 0000
298h	—	Unimplemented								---- ----	---- ----
299h	—	Unimplemented								---- ----	---- ----
29Ah	—	Unimplemented								---- ----	---- ----
29Bh	—	Unimplemented								---- ----	---- ----
29Ch	—	Unimplemented								---- ----	---- ----
29Dh	—	Unimplemented								---- ----	---- ----
29Eh	—	Unimplemented								---- ----	---- ----
29Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 63 (Continued)											
1FE4h	STATUS_SHAD	—	—	—	—	—	Z_SHAD	DC_SHAD	C_SHAD	---- -xxx	---- -uuu
1FE5h	WREG_SHAD	WREG_SHAD<7:0>								xxxx xxxx	uuuu uuuu
1FE6h	BSR_SHAD	—	—	—	BSR_SHAD<4:0>					---x xxxx	---u uuuu
1FE7h	PCLATH_SHAD	—	PCLATH_SHAD<6:0>							-xxx xxxx	-uuu uuuu
1FE8h	FSR0L_SHAD	FSR0L_SHAD<7:0>								xxxx xxxx	uuuu uuuu
1FE9h	FSR0H_SHAD	FSR0H_SHAD<7:0>								xxxx xxxx	uuuu uuuu
1FEAh	FSR1L_SHAD	FSR1L_SHAD<7:0>								xxxx xxxx	uuuu uuuu
1FEBh	FSR1H_SHAD	FSR1H_SHAD<7:0>								xxxx xxxx	uuuu uuuu
1FECh	—	Unimplemented								---- ----	---- ----
1FEDh	STKPTR	—	—	—	STKPTR<4:0>					-111 1100	---u uuuu
1FEEh	TOSL	TOSL<7:0>								xxxx xxxx	uuuu uuuu
1FEFh	TOSH	—	TOSH<6:0>							-xxx xxxx	-uuu uuuu

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 5-1: BOOT BLOCK SIZE BITS

$\overline{\text{BBEN}}$	BBSIZE[2:0]	Actual Boot Block Size User Program Memory Size (words)			Last Boot Block Memory Access
		8k	16k	32k	
1	xxx	0	0	0	—
0	111	512	512	512	01FFh
0	110	1024	1024	1024	03FFh
0	101	2048	2048	2048	07FFh
0	100	4096	4096	4096	0FFFh
0	011	Note 1	8192	8192	1FFFh
0	010			16384	3FFFh
0	001				3FFFh
0	000				3FFFh

Note 1: The maximum boot block size is half the user program memory size. All selections higher than the maximum are set to half size. For example, all BBSIZE = 000 - 100 produce a boot block size of 4 kW on a 8 kW device.

REGISTER 5-5: CONFIGURATION WORD 5: CODE PROTECTION

U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—
bit 13					bit 8

U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1
—	—	—	—	—	—	—	$\overline{\text{CP}}$
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	x = Bit is unknown	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	W = Writable bit	n = Value when blank or after Bulk Erase

bit 13-1 **Unimplemented:** Read as ‘1’

bit 0 **$\overline{\text{CP}}$:** Program Flash Memory Code Protection bit
1 = Program Flash Memory code protection disabled
0 = Program Flash Memory code protection enabled

REGISTER 9-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-q/q	R/W-q/q	R/W-q/q
—	—	—	—	—	HFFRQ<2:0>(1)		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **HFFRQ<2:0>:** HFINTOSC Frequency Selection bits
Nominal Freq (MHz):
111 = Reserved
110 = 32
101 = 16
100 = 12
011 = 8
010 = 4
001 = 2
000 = 1

Note 1: When RSTOSC=110 (HFINTOSC 1 MHz), the HFFRQ bits will default to '010' upon Reset; when RSTOSC = 000 (HFINTOSC 32 MHz), the HFFRQ bits will default to '110' upon Reset.

REGISTER 9-7: OSCTUNE: HFINTOSC TUNING REGISTER

U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	HFTUN<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **HFTUN<5:0>:** HFINTOSC Frequency Tuning bits(1)
01 1111 = Maximum frequency
01 1110 =
•
•
•
00 0001 =
00 0000 = Center frequency. Oscillator module is running at the calibrated frequency (default value).
11 1111 =
•
•
•
10 0001 =
10 0000 = Minimum frequency.

Note 1: Read-only when ACTEN = 1.

13.4.7 NVMREG ACCESS TO DEVICE INFORMATION AREA, DEVICE CONFIGURATION AREA, USER ID, DEVICE ID AND CONFIGURATION WORDS

Instead of accessing Program Flash Memory (PFM), the Device Information Area (DIA), Device Configuration Information (DCI), the User ID's, Device ID/Revision ID, EEPROM and Configuration Words can be accessed when NVMREGS = 1 in the NVMCON1 register. This is the region that would be pointed to by PC<15> = 1, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 13-3.

When read access is initiated on an address outside the parameters listed in Table 13-3, the NVMDATH: NVMDATL register pair is cleared, reading back '0's.

TABLE 13-3: NVRM ACCESS TO DEVICE INFORMATION AREA, DEVICE CONFIGURATION AREA, USER ID, DEVICE ID AND CONFIGURATION WORDS (NVMREGS = 1)

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8005h-8006h	Device ID/Revision ID	Yes	No
8007h-800Bh	Configuration Words 1-5	Yes	No
8100h-82FFh	DIA and DCI	Yes	No
F000h-F0FFh	EEPROM	Yes	Yes

14.5 Register Definitions: PORTB

REGISTER 14-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **RB<7:0>**: PORTB I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

REGISTER 14-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TRISB<7:0>:** PORTB Tri-State Control bit
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

14.11 Register Definitions: PORTE

REGISTER 14-33: PORTE: PORTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u
RE7	RE6	RE5	RE4	RE3	—	RE1	RE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **RE<7:3>**: PORTE I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **RE<1:0>**: PORTE I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTE are actually written to corresponding LATE register. Reads from PORTE register is return of actual I/O pin values.

REGISTER 14-34: TRISE: PORTE TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1
TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	—	TRISE1	TRISE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **TRISE<7:3>:** PORTE Tri-State Control bit
1 = PORTE pin configured as an input (tri-stated)
0 = PORTE pin configured as an output

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **TRISE<1:0>:** PORTE Tri-State Control bit
1 = PORTE pin configured as an input (tri-stated)
0 = PORTE pin configured as an output

REGISTER 17-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **IOCBP<7:0>:** Interrupt-on-Change PORTB Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

REGISTER 17-5: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **IOCBN<7:0>:** Interrupt-on-Change PORTB Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

REGISTER 17-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-0 **IOCBF<7:0>:** Interrupt-on-Change PORTB Flag bits
1 = An enabled change was detected on the associated pin
Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.
0 = No change was detected, or the user cleared the detected change

REGISTER 17-7: IOCCP: INTERRUPT-ON-CHANGE PORTC POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCCP7	IOCCP6	—	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IOCCP<7:6>:** Interrupt-on-Change PORTC Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **IOCCP<4:0>:** Interrupt-on-Change PORTC Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

REGISTER 17-8: IOCCN: INTERRUPT-ON-CHANGE PORTC NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCCN7	IOCCN6	—	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
bit 7							bit 0

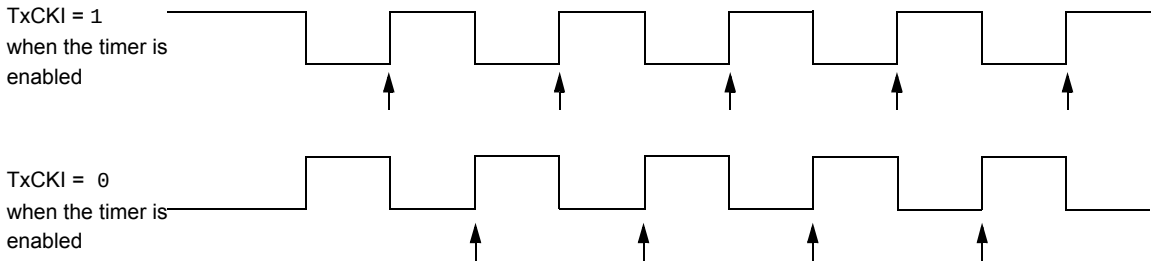
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **IOCCN<7:6>:** Interrupt-on-Change PORTC Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **IOCCN<4:0>:** Interrupt-on-Change PORTC Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

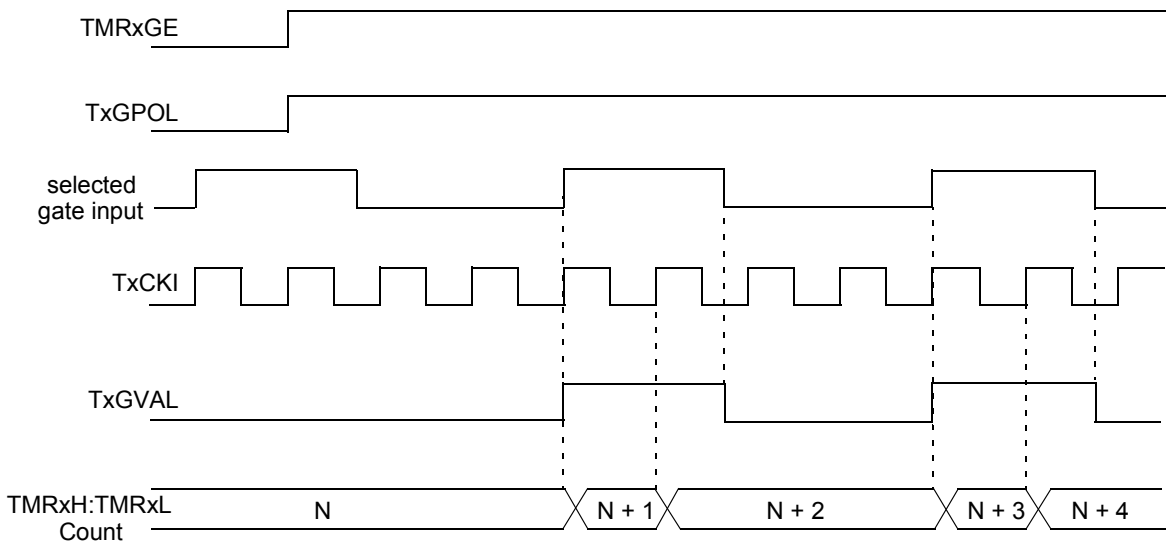
FIGURE 26-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

FIGURE 26-3: TIMER1 GATE ENABLE MODE



27.5.6 EDGE-TRIGGERED ONE-SHOT MODE

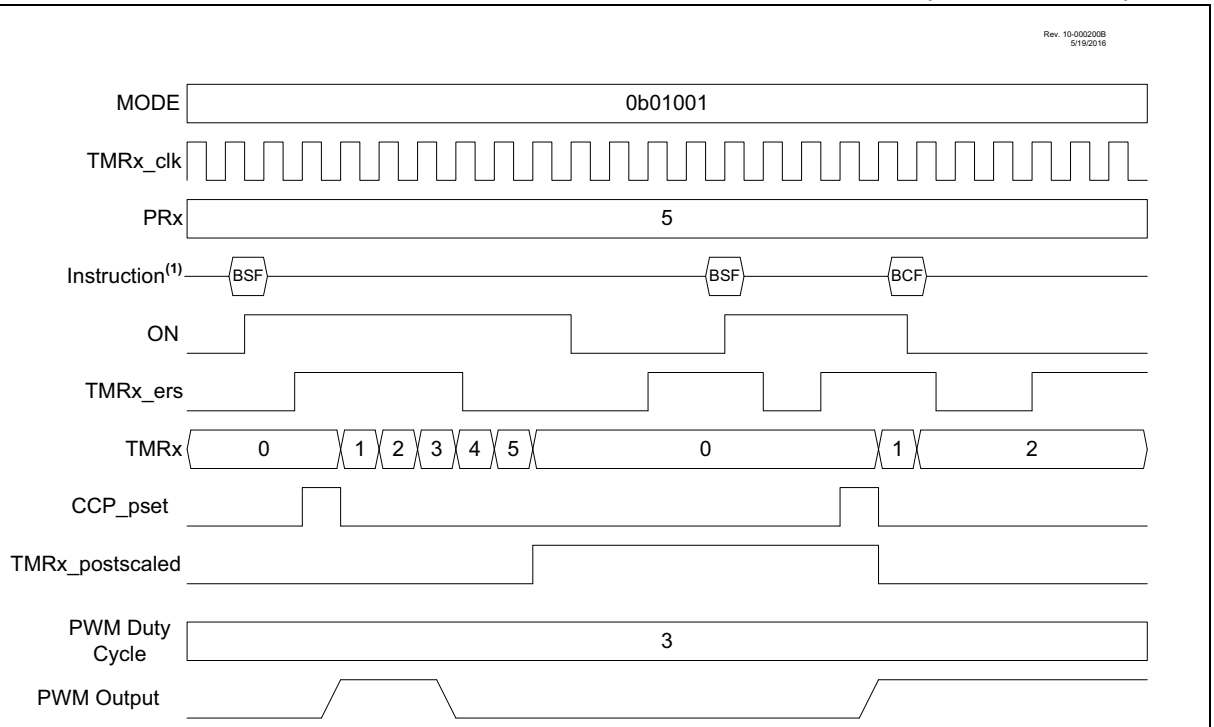
The Edge-Triggered One-Shot modes start the timer on an edge from the external signal input, after the ON bit is set, and clear the ON bit when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 01001)
- Falling edge (MODE<4:0> = 01010)
- Rising or Falling edge (MODE<4:0> = 01011)

If the timer is halted by clearing the ON bit then another TMRx_ers edge is required after the ON bit is set to resume counting. Figure 27-9 illustrates operation in the rising edge One-Shot mode.

When Edge-Triggered One-Shot mode is used in conjunction with the CCP then the edge-trigger will activate the PWM drive and the PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated when the timer halts at the PRx period count match.

FIGURE 27-9: EDGE-TRIGGERED ONE-SHOT MODE TIMING DIAGRAM (MODE = 01001)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

27.5.7 EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE

In Edge-Triggered Hardware Limit One-Shot modes the timer starts on the first external signal edge after the ON bit is set and resets on all subsequent edges. Only the first edge after the ON bit is set is needed to start the timer. The counter will resume counting automatically two clocks after all subsequent external Reset edges. Edge triggers are as follows:

- Rising edge start and Reset (MODE<4:0> = 01100)
- Falling edge start and Reset (MODE<4:0> = 01101)

The timer resets and clears the ON bit when the timer value matches the PRx period value. External signal edges will have no effect until after software sets the ON bit. Figure 27-10 illustrates the rising edge hardware limit one-shot operation.

When this mode is used in conjunction with the CCP then the first starting edge trigger, and all subsequent Reset edges, will activate the PWM drive. The PWM drive will deactivate when the timer matches the CCPRx pulse-width value and stay deactivated until the timer halts at the PRx period match unless an external signal edge resets the timer before the match occurs.

TABLE 27-2: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2/4

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	EN	—	OUT	FMT	MODE<3:0>				458
CCP2CON	EN	—	OUT	FMT	MODE<3:0>				458
CCPTMRS0	P4TSEL<1:0>		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		461
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	166
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
T2TMR	TMR2<7:0>								384*
T2PR	PR2 <7:0>								384*
T2CON	ON	CKPS <2:0>			OUTPS <3:0>				404
T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					405
T2CLKCON	—	—	—	—	CS <3:0>				403
T2RST	—	—	—	—	RSEL <3:0>				406
T4TMR	TMR4<7:0>								384*
T4PR	PR4 <7:0>								384*
T4CON	ON	CKPS <2:0>			OUTPS <3:0>				404
T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					405
T4CLKCON	—	—	—	—	CS <3:0>				403
T4RST	—	—	—	—	RSEL <3:0>				406

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2/4 module.

* Page provides register information.

30.1 Standard PWM Mode

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the PWMx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- TMR2 register
- PR2 register
- PWMxCON registers
- PWMxDCH registers
- PWMxDCL registers

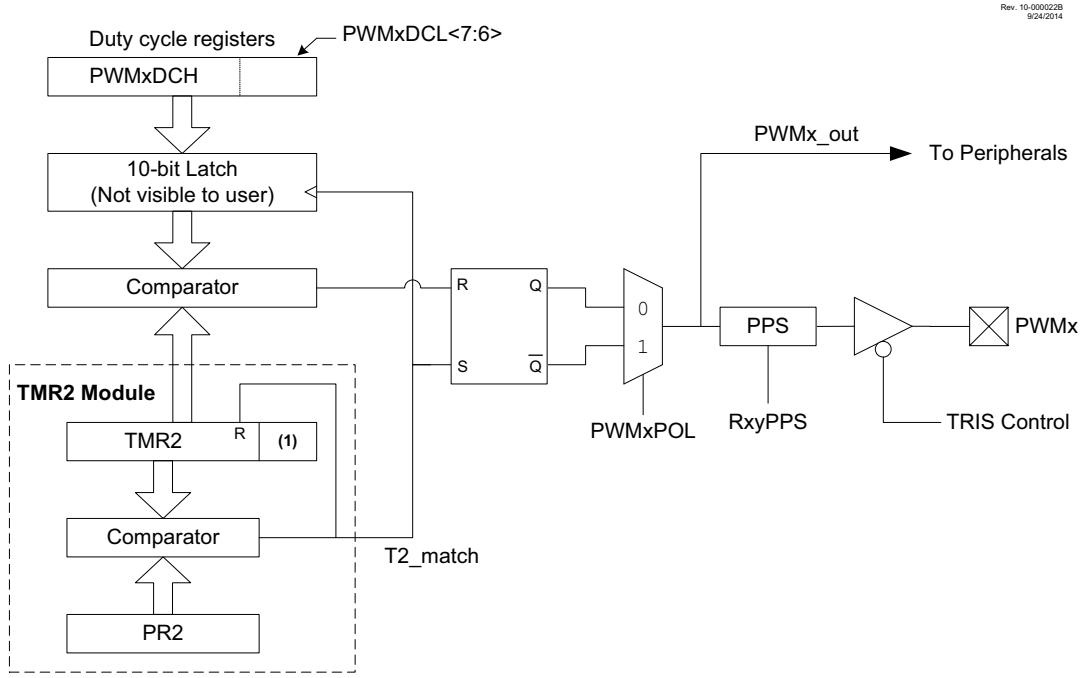
Figure 30-2 shows a simplified block diagram of PWM operation.

If PWMPOL = 0, the default state of the output is '0'. If PWMPOL = 1, the default state is '1'. If PWMEN = 0, the output will be the default state.

Note 1: The corresponding TRIS bit must be cleared to enable the PWM output on the PWMx pin.

2: Two identical Timer2 modules are implemented on this device. The timers are named Timer2 and Timer4. All references to Timer2 apply as well to Timer4. All references to T2PR apply as well to T4PR.

FIGURE 30-2: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time-base.

TABLE 31-2: SUMMARY OF REGISTERS ASSOCIATED WITH CWG

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CWG1CLKCON	—	—	—	—	—	—	—	CS	492
CWG1ISM	—	—	—	—	IS<3:0>				492
CWG1DBR	—	—	DBR<5:0>						488
CWG1DBF	—	—	DBF<5:0>						488
CWG1CON0	EN	LD	—	—	—	MODE<2:0>			486
CWG1CON1	—	—	IN	—	POLD	POLC	POLB	POLA	487
CWG1AS0	SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	489
CWG1AS1	—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	490
CWG1STR	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	491
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	172
PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	181

Legend: – = unimplemented locations read as '0'. Shaded cells are not used by CWG.

33.6 I²C Master Mode

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSPxCON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDA and SCL lines.

The following events will cause the SSP Interrupt Flag bit, SSPxIF, to be set (SSP interrupt, if enabled):

- Start condition generated
- Stop condition generated
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated

Note 1: The MSSP module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur

2: When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

33.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/$\overline{W}$) bit. In this case, the R/$\overline{W}$ bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{W}$ bit. In this case, the R/$\overline{W}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received eight bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. See **Section 33.7 "Baud Rate Generator"** for more detail.

TABLE 34-2: SUMMARY OF REGISTERS ASSOCIATED WITH EUSART

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	177
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	168
RCxSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	583
TXxSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	582
BAUDxCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	584
RCxREG	RCxREG<7:0>								585*
TXxREG	TXxREG<7:0>								585*
SPxBRGL	SPxBRG<7:0>								585*
SPxBRGH	SPxBRG<15:8>								586*
RXPPS	—	—	—	RXPPS<4:0>					264
CKPPS	—	—	—	CXPPS<4:0>					264
RxyPPS	—	—	—	RxyPPS<4:0>					265
CLCxSELy	—	—	—	LCxDyS<4:0>					503

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for the EUSART module.

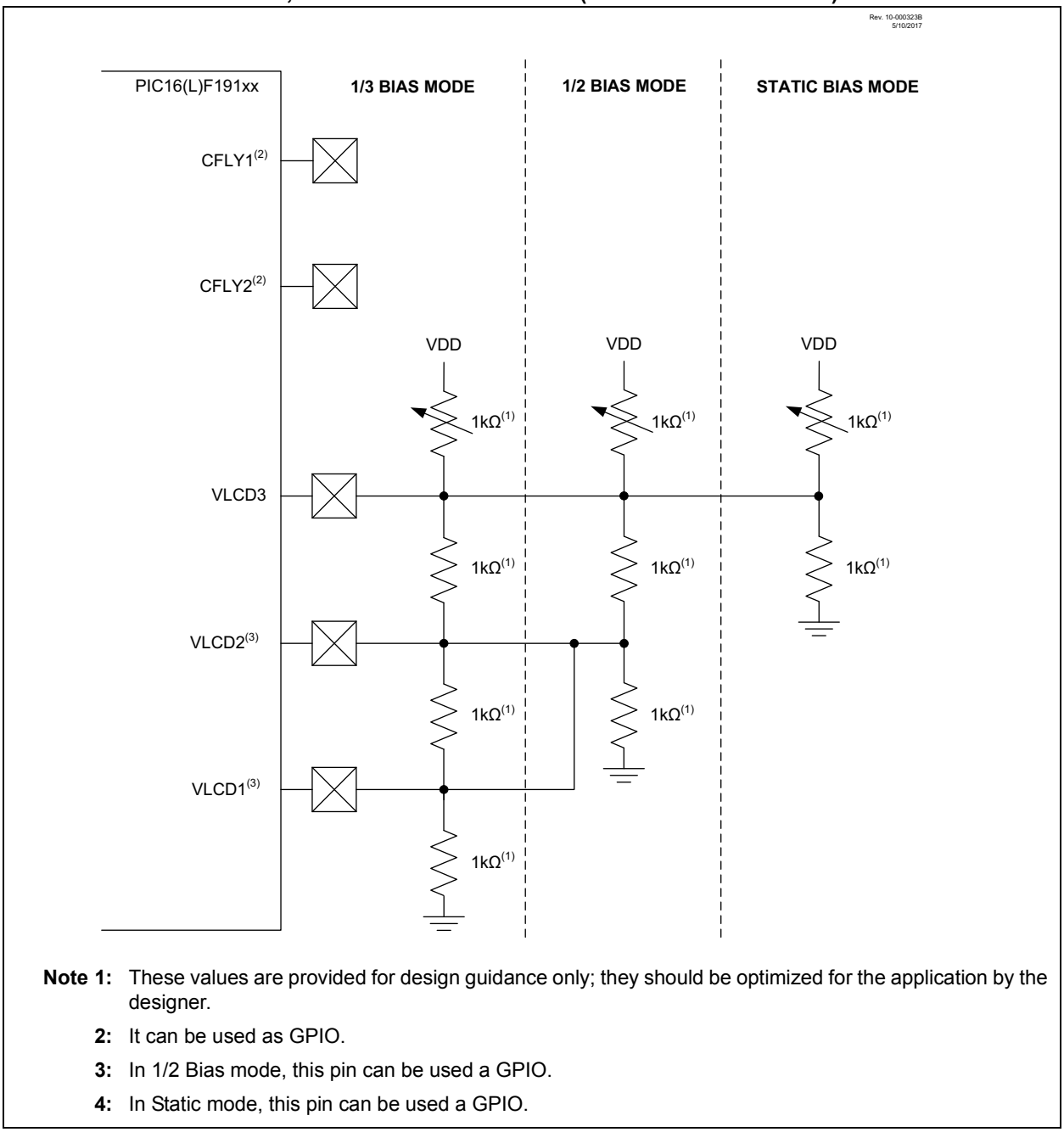
* Page with register information.

35.7.3 LCD VOLTAGE SUPPLIED FROM EXTERNAL RESISTOR LADDER

In this mode, the LCD charge pump is completely disabled. The LCD bias levels are tied to VDD and are generated using an external divider. The difference is that the internal voltage reference is also disabled and the bottom of the ladder is tied to ground (VSS); see Figure 35-6. The value of the resistors, and the difference between VSS and VDD, determine the contrast range; no software adjustment is possible. This configuration is also used where the LCD's current requirements exceed the capacity of the charge pump and the high power (HP) internal resistor ladder and the software contrast control is not needed.

Depending on the bias type required, resistors are connected between some or all of the pins. A potentiometer can also be connected between VLCD3 and VDD to allow for hardware controlled contrast adjustment.

FIGURE 35-6: CONNECTIONS FOR LCD VOLTAGE SUPPLIED FROM EXTERNAL LADDER, STATIC, 1/2 AND 1/3 BIAS MODES (LCDVSRC<3:0> = 1000)



Note 1: These values are provided for design guidance only; they should be optimized for the application by the designer.

2: It can be used as GPIO.

3: In 1/2 Bias mode, this pin can be used a GPIO.

4: In Static mode, this pin can be used a GPIO.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

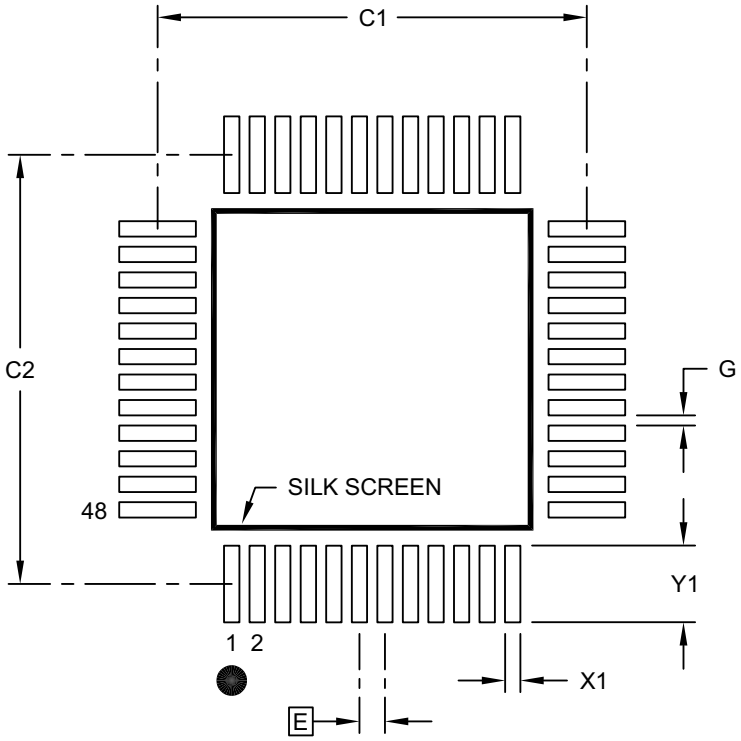
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1EBEh	CLCIN3PPS	—	—	—	CLCIN3PPS<4:0>					264
1EBFh	—	Unimplemented								
1EC0h	—	Unimplemented								
1EC1h	—	Unimplemented								
1EC2h	—	Unimplemented								
1EC3h	ADCACTPPS	—	—	ADCACTPPS<5:0>						264
1EC4h	—	Unimplemented								
1EC5h	SSP1CLKPPS	—	—	—	SSP1CLKPPS<4:0>					264
1EC6h	SSP1DATPPS	—	—	—	SSP1DATPPS<4:0>					264
1EC7h	SSP1SSPPS	—	—	—	SSP1SSPPS<4:0>					264
1EC8h	—	Unimplemented								
1EC9h	—	Unimplemented								
1ECAh	—	Unimplemented								
1ECBh	RX1PPS	—	—	—	RX1PPS<4:0>					264
1ECCh	TX1PPS	—	—	—	TX1PPS<4:0>					264
1ECDh	RX2PPS	—	—	—	RX2PPS<4:0>					264
1ECEh	TX2PPS	—	—	—	TX2PPS<4:0>					264
1ECFh	—	Unimplemented								
1ED0h	—	Unimplemented								
1ED1h	—	Unimplemented								
1ED2h	—	Unimplemented								
1ED3h	—	Unimplemented								
1ED4h	—	Unimplemented								
1ED5h	—	Unimplemented								
1ED6h	—	Unimplemented								
1ED7h	—	Unimplemented								
1ED8h	—	Unimplemented								
1ED9h	—	Unimplemented								
1EDAh	—	Unimplemented								
1EDBh	—	Unimplemented								
1EDCh	—	Unimplemented								
1EDDh	—	Unimplemented								
1EDEh	—	Unimplemented								
1EDFh	—	Unimplemented								
1EE0h	—	Unimplemented								
1EE1h	—	Unimplemented								
1EE2h	—	Unimplemented								
1EE3h	—	Unimplemented								
1EE4h	—	Unimplemented								
1EE5h	—	Unimplemented								
1EE6h	—	Unimplemented								
1EE7h	—	Unimplemented								
1EE8h	—	Unimplemented								
1EE9h	—	Unimplemented								
1EEAh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-PT Rev A