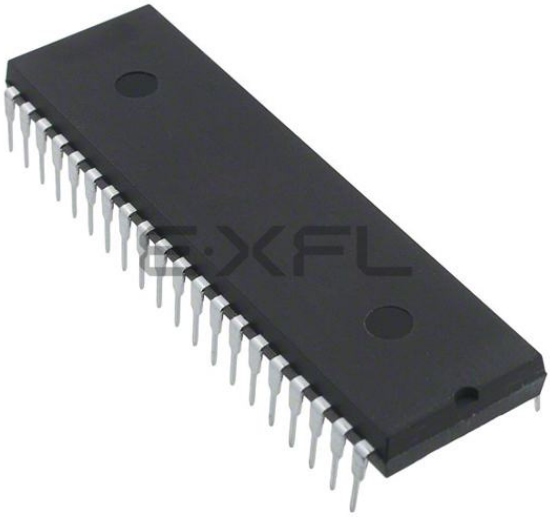

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Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
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Supplier Device Package	40-PDIP
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1D3Bh	LCDDATA35	1DBBh	—	1E3Bh	RF3PPS(3)	1EBBh	CLCIN0PPS	1F3Bh	SLRCONA	1FBBh	—
1D3Ch	LCDDATA36	1DBCh	—	1E3Ch	RF4PPS(3)	1EBCh	CLCIN1PPS	1F3Ch	INLVLA	1FBCh	—
1D3Dh	LCDDATA37	1DBDh	—	1E3Dh	RF5PPS(3)	1EBDh	CLCIN2PPS	1F3Dh	IOCAP	1FBDh	—
1D3Eh	LCDDATA38	1DBEh	—	1E3Eh	RF6PPS(3)	1EBEh	CLCIN3PPS	1F3Eh	IOCAN	1FBEh	—
1D3Fh	LCDDATA39	1DBFh	—	1E3Fh	RF7PPS(3)	1EBFh	—	1F3Fh	IOCAF	1FBFh	—
1D40h	LCDDATA40	1DC0h	—	1E40h	—	1EC0h	—	1F40h	—	1FC0h	—
1D41h	LCDDATA41	1DC1h	—	1E41h	—	1EC1h	—	1F41h	—	1FC1h	—
1D42h	LCDDATA42	1DC2h	—	1E42h	—	1EC2h	—	1F42h	—	1FC2h	—
1D43h	LCDDATA43	1DC3h	—	1E43h	—	1EC3h	ADCACTPPS	1F43h	ANSELB	1FC3h	—
1D44h	LCDDATA44	1DC4h	—	1E44h	—	1EC4h	—	1F44h	WPUB	1FC4h	—
1D45h	LCDDATA45	1DC5h	—	1E45h	—	1EC5h	SSP1CLKPPS	1F45h	ODCONB	1FC5h	—
1D46h	LCDDATA46	1DC6h	—	1E46h	—	1EC6h	SSP1DATPPS	1F46h	SLRCONB	1FC6h	—
1D47h	LCDDATA47	1DC7h	—	1E47h	—	1EC7h	SSP1SSPPS	1F47h	INLVLB	1FC7h	—
1D48h	—	1DC8h	—	1E48h	—	1EC8h	—	1F48h	IOCBP	1FC8h	—
1D49h	—	1DC9h	—	1E49h	—	1EC9h	—	1F49h	IOCBN	1FC9h	—
1D4Ah	—	1DCAh	—	1E4Ah	—	1ECAh	—	1F4Ah	IOCBF	1FCAh	—
1D4Bh	—	1DCBh	—	1E4Bh	—	1ECBh	RX1PPS	1F4Bh	—	1FCBh	—
1D4Ch	—	1DCCh	—	1E4Ch	—	1ECCh	TX1PPS	1F4Ch	—	1FCCh	—
1D4Dh	—	1DCDh	—	1E4Dh	—	1ECDh	RX2PPS	1F4Dh	—	1FCDh	—
1D4Eh	—	1DCEh	—	1E4Eh	—	1ECEh	TX2PPS	1F4Eh	ANSELC	1FCEh	—
1D4Fh	—	1DCFh	—	1E4Fh	—	1ECFh	—	1F4Fh	WPUC	1FCFh	—
1D50h	—	1DD0h	—	1E50h	ANSELF(3)	1ED0h	—	1F50h	ODCONC	1FD0h	—
1D51h	—	1DD1h	—	1E51h	WPUF(3)	1ED1h	—	1F51h	SLRCONC	1FD1h	—
1D52h	—	1DD2h	—	1E52h	ODCONF(3)	1ED2h	—	1F52h	INLVLC	1FD2h	—
1D53h	—	1DD3h	—	1E53h	SLRCONF(3)	1ED3h	—	1F53h	IOCCP	1FD3h	—
1D54h	—	1DD4h	—	1E54h	INLVLF(3)	1ED4h	—	1F54h	IOCCN	1FD4h	—
1D55h	—	1DD5h	—	1E55h	—	1ED5h	—	1F55h	IOCCF	1FD5h	—
1D56h	—	1DD6h	—	1E56h	—	1ED6h	—	1F56h	—	1FD6h	—
1D57h	—	1DD7h	—	1E57h	—	1ED7h	—	1F57h	—	1FD7h	—
1D58h	—	1DD8h	—	1E58h	—	1ED8h	—	1F58h	—	1FD8h	—
1D59h	—	1DD9h	—	1E59h	—	1ED9h	—	1F59h	ANSELD	1FD9h	—
1D5Ah	—	1DDAh	—	1E5Ah	—	1EDAh	—	1F5Ah	WPUD	1FDAh	—
1D5Bh	—	1DDBh	—	1E5Bh	—	1EDBh	—	1F5Bh	ODCOND	1FDBh	—
1D5Ch	—	1DDCh	—	1E5Ch	—	1EDCh	—	1F5Ch	SLRCOND	1FDCh	—
1D5Dh	—	1DDDh	—	1E5Dh	—	1EDDh	—	1F5Dh	INLVLD	1FDDh	—
1D5Eh	—	1DDEh	—	1E5Eh	—	1EDEh	—	1F5Eh	—	1FDEh	—
1D5Fh	—	1DDFh	—	1E5Fh	—	1EDFh	—	1F5Fh	—	1FDFh	—
1D60h	—	1DE0h	—	1E60h	—	1EE0h	—	1F60h	—	1FE0h	—
1D61h	—	1DE1h	—	1E61h	—	1EE1h	—	1F61h	—	1FE1h	—
1D62h	—	1DE2h	—	1E62h	—	1EE2h	—	1F62h	—	1FE2h	—
1D63h	—	1DE3h	—	1E63h	—	1EE3h	—	1F63h	—	1FE3h	—
1D64h	—	1DE4h	—	1E64h	—	1EE4h	—	1F64h	ANSELE	1FE4h	STATUS_SHAD
1D65h	—	1DE5h	—	1E65h	—	1EE5h	—	1F65h	WPUE	1FE5h	WREG_SHAD
1D66h	—	1DE6h	—	1E66h	—	1EE6h	—	1F66h	ODCONE	1FE6h	BSR_SHAD
1D67h	—	1DE7h	—	1E67h	—	1EE7h	—	1F67h	SLRCONE	1FE7h	PCLATH_SHAD
1D68h	—	1DE8h	—	1E68h	—	1EE8h	—	1F68h	INLVLE	1FE8h	FSR0L_SHAD
1D69h	—	1DE9h	—	1E69h	—	1EE9h	—	1F69h	IOCEP	1FE9h	FSR0H_SHAD
1D6Ah	—	1DEAh	—	1E6Ah	—	1EEAh	—	1F6Ah	IOCEN	1FEAh	FSR1L_SHAD
1D6Bh	—	1DEBh	—	1E6Bh	—	1EEBh	—	1F6Bh	IOCEF	1FEBh	FSR1H_SHAD
1D6Ch	—	1DECh	—	1E6Ch	—	1EECh	—	1F6Ch	—	1FECh	—
1D6Dh	—	1DEDh	—	1E6Dh	—	1EEDh	—	1F6Dh	—	1FEDh	STKPTR

Note 1: Unimplemented locations read as '0'.
2: Present only on PIC16(L)F19156/76/86.
3: Present only on PIC16(L)F19185/86.

TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (ALL BANKS)

Bank Offset Bank 0-Bank 63	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
All Banks											
x00h or x80h	INDF0	INDF0								xxxx xxxx	xxxx xxxx
x01h or x81h	INDF1	INDF1								xxxx xxxx	xxxx xxxx
x02h or x82h	PCL	PCL								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	FSR0L								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	FSR0H								0000 0000	0000 0000
x06h or x86h	FSR1L	FSR1L								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	FSR1H								0000 0000	0000 0000
x08h or x88h	BSR	—	—	BSR						--00 0000	--00 0000
x09h or x89h	WREG	WREG0								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	PCLATH							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	00-- ---1	00-- ---1

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: These Registers can be accessed from any bank

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TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 58 (continued)											
1D2Ah	LCDDATA18	S15C3	S14C3	S13C3	—	SE11C3	S10C3	S09C3	S08C3	0000 0000	0000 0000
1D2Bh	LCDDATA19	S23C3	S22C3	—	S20C3	S19C3	S18C3	—	—	0000 0000	0000 0000
1D2Ch	LCDDATA20	S31C3	S30C3	S29C3	S28C3	S27C3	S26C3	S25C3	S24C3	0000 0000	0000 0000
1D2Dh	LCDDATA21	—	—	—	—	—	S34C3	S33C3	S32C3	0000 0000	0000 0000
1D2Eh	LCDDATA22	S47C3	S46C3	S45C3	S44C3	S43C3	S42C3	S41C3	S40C3	0000 0000	0000 0000
1D2Fh	LCDDATA23	S07C4	S06C4	—	S04C4	S03C4	S02C4	S01C4	S00C4	0000 0000	0000 0000
1D30h	LCDDATA24	S15C4	S14C4	S13C4	—	S11C4	S10C4	S09C4	S08C4	0000 0000	0000 0000
1D31h	LCDDATA25	S23C4	S22C4	—	S20C4	S19C4	S18C4	—	—	0000 0000	0000 0000
1D32h	LCDDATA26	S31C4	S30C4	S29C4	S28C4	S27C4	S26C4	S25C4	S24C4	0000 0000	0000 0000
1D33h	LCDDATA27	—	—	—	—	—	S34C4	S33C4	S32C4	0000 0000	0000 0000
1D34h	LCDDATA28	S47C4	S46C4	S45C4	S44C4	S43C4	S42C4	S41C4	S40C4	0000 0000	0000 0000
1D35h	LCDDATA29	S07C5	S06C5	—	S04C5	S03C5	S02C5	S01C5	S00C5	0000 0000	0000 0000
1D36h	LCDDATA30	S15C5	S14C5	S13C5	—	S11C5	S10C5	S09C5	S08C5	0000 0000	0000 0000
1D37h	LCDDATA31	S23C5	S22C5	—	S20C5	S19C5	S18C5	—	—	0000 0000	0000 0000
1D38h	LCDDATA32	S31C5	S30C5	S29C5	S28C5	S27C5	S26C5	S25C5	S24C5	0000 0000	0000 0000
1D39h	LCDDATA33	—	—	—	—	—	S34C5	S33C5	S32C5	0000 0000	0000 0000
1D3Ah	LCDDATA34	S47C5	S46C5	S45C5	S44C5	S43C5	S42C5	S41C5	S40C5	0000 0000	0000 0000
1D3Bh	LCDDATA35	S07C6	S06C6	—	S04C6	S03C6	S02C6	S01C6	S00C6	0000 0000	0000 0000
1D3Ch	LCDDATA36	S15C6	S14C6	S13C6	—	S11C6	S10C6	S09C6	S08C6	0000 0000	0000 0000
1D3Dh	LCDDATA37	S23C6	S22C6	—	S20C6	S19C6	S18C6	—	—	0000 0000	0000 0000
1D3Eh	LCDDATA38	S31C6	S30C6	S29C6	S28C6	S27C6	S26C6	S25C6	S24C6	0000 0000	0000 0000
1D3Fh	LCDDATA39	—	—	—	—	—	S34C6	S33C6	S32C6	0000 0000	0000 0000
1D40h	LCDDATA40	S47C6	S46C6	S45C6	S44C6	S43C6	S42C6	S41C6	S40C6	0000 0000	0000 0000
1D41h	LCDDATA41	S07C7	S06C7	—	S04C7	S03C7	S02C7	S01C7	S00C7	0000 0000	0000 0000
1D42h	LCDDATA42	S15C7	S14C7	S13C7	—	S11C7	S10C7	S09C7	S08C7	0000 0000	0000 0000
1D43h	LCDDATA43	S23C7	S22C7	—	S20C7	S19C7	S18C7	—	—	0000 0000	0000 0000
1D44h	LCDDATA44	S31C7	S30C7	S29C7	S28C7	S27C7	S26C7	S25C7	S24C7	0000 0000	0000 0000
1D45h	LCDDATA45	—	—	—	—	—	S34C7	S33C7	S32C7	0000 0000	0000 0000
1D46h	LCDDATA46	S47C7	S46C7	S45C7	S44C7	S43C7	S42C7	S41C7	S40C7	0000 0000	0000 0000
1D47h	LCDDATA47	S07C0	S06C0	—	S04C0	S03C0	S02C0	S01C0	S00C0	0000 0000	0000 0000

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9.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits of the OSCCON1 register.

9.3.1 NEW OSCILLATOR SOURCE (NOSC) AND NEW DIVIDER SELECTION REQUEST (NDIV) BITS

The New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits of the OSCCON1 register select the system clock source and the frequency that are used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, and will be immediately ready. The device may enter Sleep while waiting for the switch as described in **Section 9.3.3 "Clock Switch and Sleep"**.

When the new oscillator is ready, the New Oscillator is Ready (NOSCR) bit of OSCCON3 and the Clock Switch Interrupt Flag (CSWIF) bit of PIR1 become set (CSWIF = 1). If Clock Switch Interrupts are enabled (CSWIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

If the Clock Switch Hold (CSWHOLD) bit of OSCCON3 is clear, the oscillator switch will occur when the new Oscillator's READY bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

- set CSWHOLD = 0 so the switch can complete, or
- copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (e.g., changing FOSC from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock source will already be active, so the switch is relatively quick. CSWHOLD must be clear (CSWHOLD = 0) for the switch to complete.

The current COSC and CDIV are indicated in the OSCCON2 register up to the moment when the switch actually occurs, at which time OSCCON2 is updated and ORDY is set. NOSCR is cleared by hardware to indicate that the switch is complete.

9.3.2 PLL INPUT SWITCH

Switching between the PLL and any non-PLL source is managed as described above. The input to the PLL is established when NOSC selects the PLL, and maintained by the COSC setting.

When NOSC and COSC select the PLL with different input sources, the system continues to run using the COSC setting, and the new source is enabled per NOSC. When the new oscillator is ready (and CSWHOLD = 0), system operation is suspended while the PLL input is switched and the PLL acquires lock.

Note:	If the PLL fails to lock, the FSCM will trigger.

9.3.3 CLOCK SWITCH AND SLEEP

If OSCCON1 is written with a new value and the device is put to Sleep before the switch completes, the switch will not take place and the device will enter Sleep mode.

When the device wakes from Sleep and the CSWHOLD bit is clear, the device will wake with the 'new' clock active, and the clock switch interrupt flag bit (CSWIF) will be set.

When the device wakes from Sleep and the CSWHOLD bit is set, the device will wake with the 'old' clock active and the new clock will be requested again.

REGISTER 10-16: PIR5: PERIPHERAL INTERRUPT REQUEST REGISTER 5

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	R/W/HS-0/0
CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **CLC4IF:** CLC4 Interrupt Flag bit
1 = A CLC4OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC4 interrupt event has occurred

bit 6 **CLC3IF:** CLC3 Interrupt Flag bit
1 = A CLC3OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC3 interrupt event has occurred

bit 5 **CLC2IF:** CLC2 Interrupt Flag bit
1 = A CLC2OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC2 interrupt event has occurred

bit 4 **CLC1IF:** CLC1 Interrupt Flag bit
1 = A CLC1OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC1 interrupt event has occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = The Timer1 Gate has gone inactive (the acquisition is complete)
0 = The Timer1 Gate has not gone inactive

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

12.0 WINDOWED WATCHDOG TIMER (WWDT)

The Windowed Watchdog Timer (WWDT) is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that CLRWDT instructions are only accepted when they are performed within a specific window during the time-out period.

The WWDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WWDT is always on
  - WWDT is off when in Sleep
  - WWDT is controlled by software
  - WWDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Configurable window size from 12.5 to 100 percent of the time-out period
- Multiple Reset conditions
- Operation during Sleep

14.4.7 ANALOG CONTROL

The ANSELB register (Register 14-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.4.8 WEAK PULL-UP CONTROL

The WPUB register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.4.9 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

TABLE 14-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	229
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	229
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	230
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	230
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	231
ODCONB	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	231
SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	232
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	232
HIDRVB	—	—	—	—	—	—	HIDB1	—	232

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

14.8 PORTD Registers

Note:	PORTD functionality is not available on the PIC16(L)F19155/56 family of devices.

14.8.1 DATA REGISTER

PORTD is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISD (Register 14-2). Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., disable the output driver). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 14.2.8 shows how to initialize PORTD.

Reading the PORTD register (Register 14-1) reads the status of the pins, whereas writing to it will write to the PORT latch.

The PORT data latch LATD (Register 14-3) holds the output port data, and contains the latest value of a LATD or PORTD write.

EXAMPLE 14-3: INITIALIZING PORTD

```
; This code example illustrates
; initializing the PORTD register. The
; other ports are initialized in the same
; manner.

BANKSEL  PORTD        ;
CLRF     PORTD        ;Init PORTD
BANKSEL  LATD         ;Data Latch
CLRF     LATD         ;
BANKSEL  ANSELD       ;
CLRF     ANSELD       ;digital I/O
BANKSEL  TRISD        ;
MOVLW    B'00111000'  ;Set RD<5:3> as inputs
MOVWF    TRISD        ;and set RD<2:0> as
                      ;outputs
```

14.8.2 DIRECTION CONTROL

The TRISD register (Register 14-2) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

14.8.3 OPEN-DRAIN CONTROL

The ODCOND register (Register 14-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCOND bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCOND bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note:	It is not necessary to set open-drain control when using the pin for I^2C; the I^2C module controls the pin and makes the pin open-drain.

14.8.4 SLEW RATE CONTROL

The SLRCOND register (Register 14-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCOND bit is set, the corresponding port pin drive is slew rate limited. When an SLRCOND bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

14.8.5 INPUT THRESHOLD CONTROL

The INLVLD register (Register 14-8) controls the input voltage threshold for each of the available PORTD input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTD register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 39-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

REGISTER 26-3: T1CLK TIMER1 CLOCK SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	—	CS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **CS<3:0>:** Timer1 Clock Select bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = LC4_out
1011 = LC3_out
1010 = LC2_out
1001 = LC1_out
1000 = Timer0 Overflow Output
0111 = SOSC
0110 = MFINTOSC (32 kHz)
0101 = MFINTOSC (500 kHz)
0100 = LFINTOSC
0011 = HFINTOSC
0010 = FOSC
0001 = FOSC/4
0000 = TxCKIPPS

28.1 Register Definitions: SMT Control

Long bit name prefixes for the SMT peripherals are shown in Table 28-1. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information.

TABLE 28-1:

Peripheral	Bit Name Prefix
SMT1	SMT1

REGISTER 28-1: SMTxCON0: SMT CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN(1)	—	STP	WPOL	SPOL	CPOL	SMTxPS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** SMT Enable bit(1)
1 = SMT is enabled
0 = SMT is disabled; internal states are reset, clock requests are disabled

bit 6 **Unimplemented**: Read as '0'

bit 5 **STP:** SMT Counter Halt Enable bit
When SMTxTMR = SMTxPR:
1 = Counter remains SMTxPR; period match interrupt occurs when clocked
0 = Counter resets to 24'h000000; period match interrupt occurs when clocked

bit 4 **WPOL:** SMTxWIN Input Polarity Control bit
1 = SMTxWIN signal is active-low/falling edge enabled
0 = SMTxWIN signal is active-high/rising edge enabled

bit 3 **SPOL:** SMTxSIG Input Polarity Control bit
1 = SMTx_signal is active-low/falling edge enabled
0 = SMTx_signal is active-high/rising edge enabled

bit 2 **CPOL:** SMT Clock Input Polarity Control bit
1 = SMTxTMR increments on the falling edge of the selected clock signal
0 = SMTxTMR increments on the rising edge of the selected clock signal

bit 1-0 **SMTxPS<1:0>:** SMT Prescale Select bits
11 = Prescaler = 1:8
10 = Prescaler = 1:4
01 = Prescaler = 1:2
00 = Prescaler = 1:1

Note 1: Setting EN to '0' does not affect the register contents.

REGISTER 29-1: CCPxCON: CCPx CONTROL REGISTER (CONTINUED)

bit 3-0 **MODE<3:0>:** CCPx Mode Select bits(1)

1111 = PWM mode
1110 = Reserved
1101 = Reserved
1100 = Reserved

1011 = Compare mode: output will pulse 0-1-0; Clears TMR1
1010 = Compare mode: output will pulse 0-1-0
1001 = Compare mode: clear output on compare match
1000 = Compare mode: set output on compare match

0111 = Capture mode: every 16th rising edge of CCPx input
0110 = Capture mode: every 4th rising edge of CCPx input
0101 = Capture mode: every rising edge of CCPx input
0100 = Capture mode: every falling edge of CCPx input

0011 = Capture mode: every edge of CCPx input
0010 = Compare mode: toggle output on match
0001 = Compare mode: toggle output on match; clear TMR1
0000 = Capture/Compare/PWM off (resets CCPx module)

Note 1: All modes will set the CCPxIF bit, and will trigger an ADC conversion if CCPx is selected as the ADC trigger source.

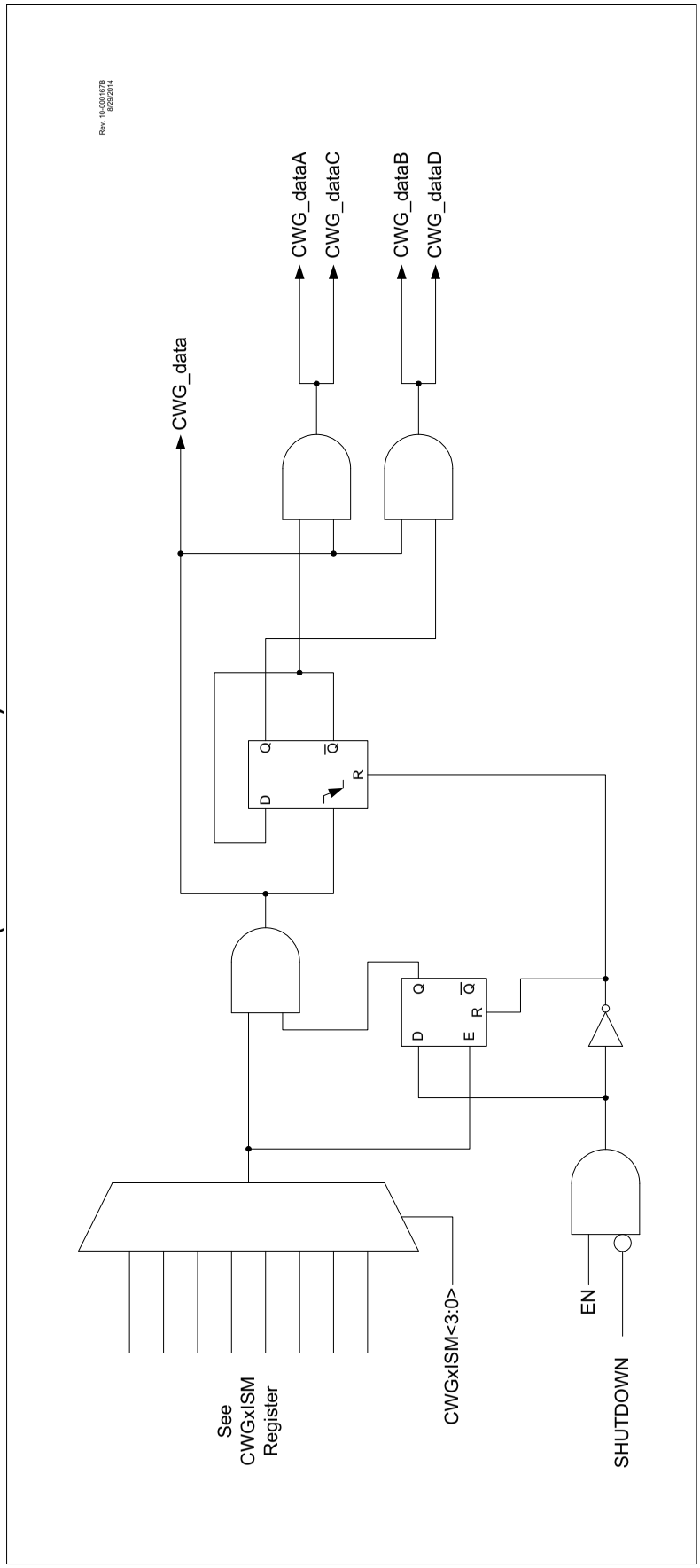


FIGURE 31-2: SIMPLIFIED CWG BLOCK DIAGRAM (PUSH-PULL MODE)

FIGURE 31-6: DEAD-BAND OPERATION CWG1DBR = 0X01, CWG1DBF = 0X02

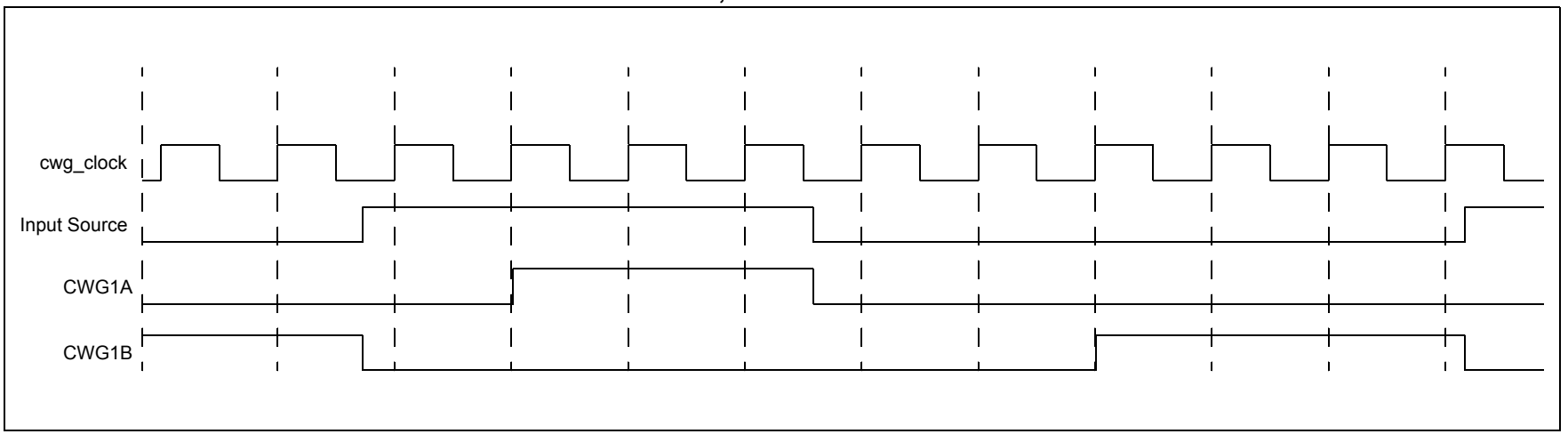
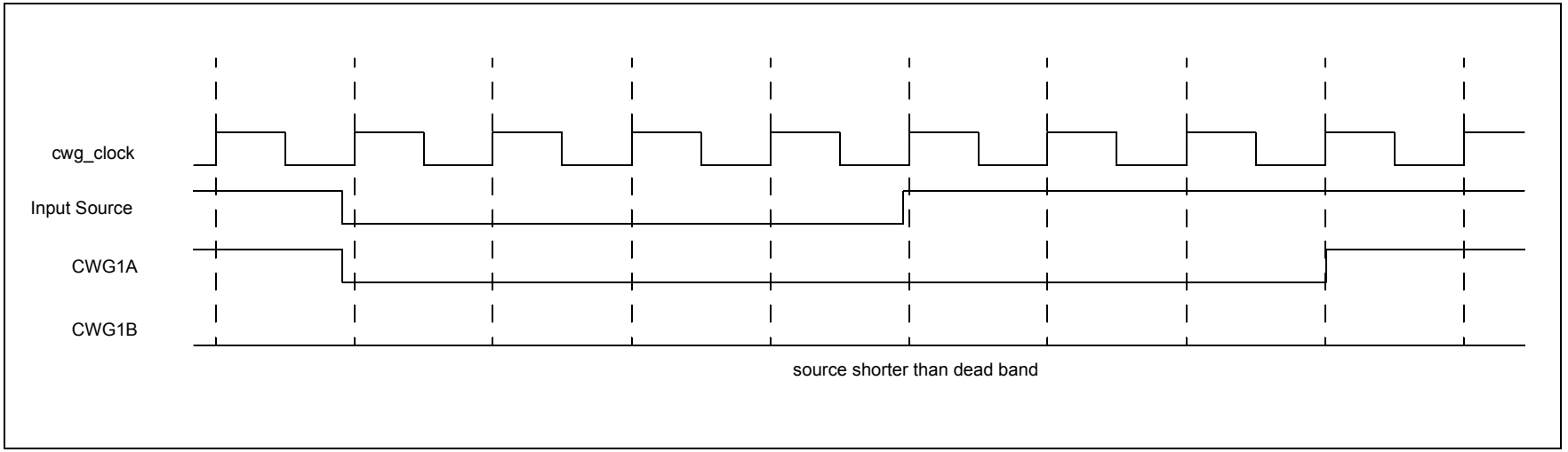


FIGURE 31-7: DEAD-BAND OPERATION, CWG1DBR = 0X03, CWG1DBF = 0X04, SOURCE SHORTER THAN DEAD BAND



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33.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

33.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

33.4 I²C MODE OPERATION

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC® microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

33.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

33.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I²C specification.

33.4.3 SDA AND SCL PINS

When selecting any I²C mode, the SCL and SDA pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note 1:	Any device pin can be selected for SDA and SCL functions with the PPS peripheral. These functions are bidirectional. The SDA input is selected with the SSPDATPPS registers. The SCL input is selected with the SSPCLKPPS registers. Outputs are selected with the RxyPPS registers. It is the user's responsibility to make the selections so that both the input and the output for each function is on the same pin.

33.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPxCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

TABLE 33-1: I²C BUS TERMS

TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by the master.
Multi-master	A bus with more than one device that can initiate data transfers.
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.
Idle	No master is controlling the bus, and both SDA and SCL lines are high.
Active	Any time one or more master devices are controlling the bus.
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPxADD.
Write Request	Slave receives a matching address with R/$\overline{W}$ bit clear, and is ready to clock in data.
Read Request	Master sends an address byte with the R/$\overline{W}$ bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.
Clock Stretching	When a device on the bus hold SCL low to stall communication.
Bus Collision	Any time the SDA line is sampled low by the module while it is outputting and expected high state.

33.4.5 START CONDITION

The I²C specification defines a Start condition as a transition of SDA from a high to a low state while SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 33-12 shows wave forms for Start and Stop conditions.

33.4.6 STOP CONDITION

A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

Note: At least one SCL low time must appear before a Stop is valid, therefore, if the SDA line goes low then high again while the SCL line stays high, only the Start condition is detected.

33.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 33-13 shows the wave form for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/$\overline{W}$ bit set. The slave logic will then hold the clock and prepare to clock out data.

33.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

33.5.8 GENERAL CALL ADDRESS SUPPORT

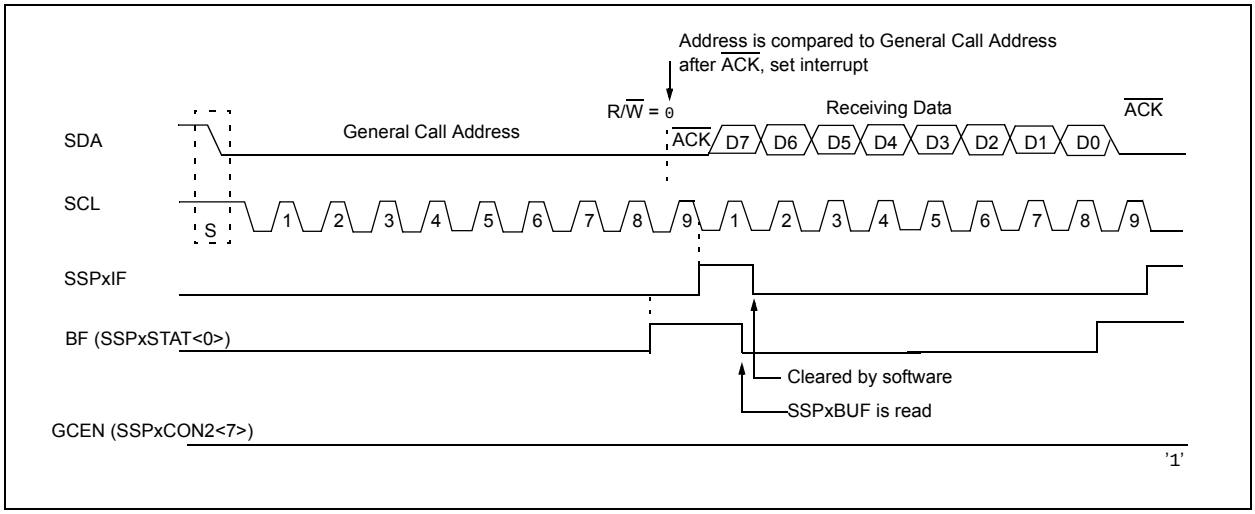
The addressing procedure for the I²C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I²C protocol, defined as address 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically $\overline{\text{ACK}}$ the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/$\overline{\text{W}}$ bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 33-24 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the eighth falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

FIGURE 33-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE



33.5.9 SSP MASK REGISTER

An SSP Mask (SSPxMSK) register (Register 33-5) is available in I²C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

33.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out (Case 1).

b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high (Case 2).

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to zero. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 33-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 33-39).

FIGURE 33-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

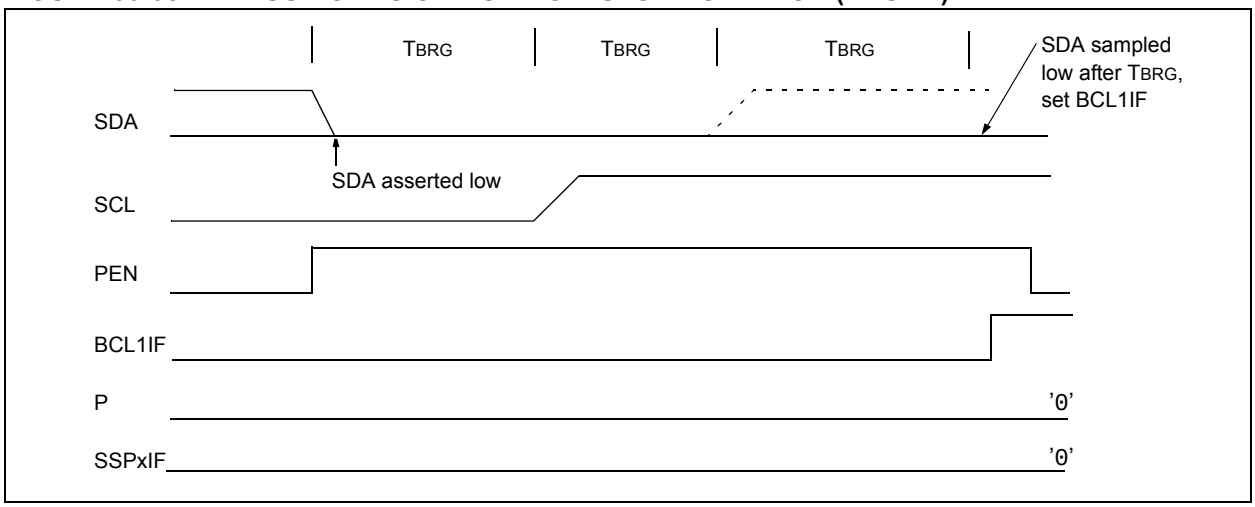


FIGURE 33-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)

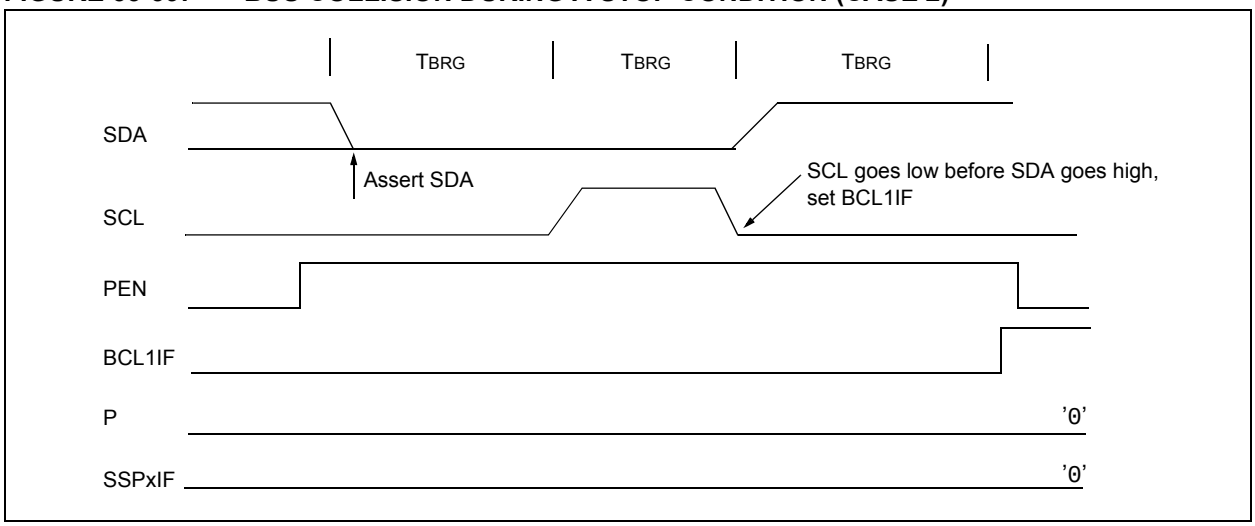


TABLE 39-9: PLL SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) $V_{DD} \geq 2.5V$							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
PLL01	F_{PLLIN}	PLL Input Frequency Range	4	—	8	MHz	
PLL02	F_{PLLOUT}	PLL Output Frequency Range	16	—	32	MHz	**Note 1**
PLL03	T_{PLLST}	PLL Lock Time from Start-up	—	200	—	µs	
PLL04	F_{PLLJIT}	PLL Output Frequency Stability (Jitter)	-0.25	—	0.25	%	

* These parameters are characterized but not tested.

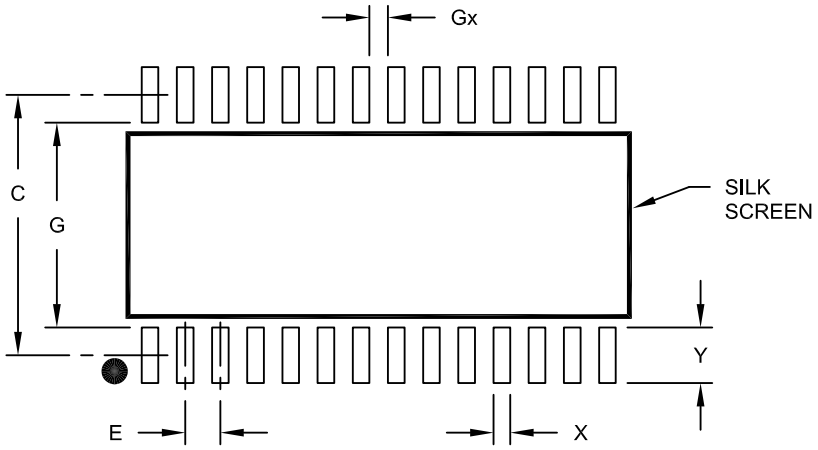
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The output frequency of the PLL must meet the F_{OSC} requirements listed in Parameter D002.

PRELIMINARY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A