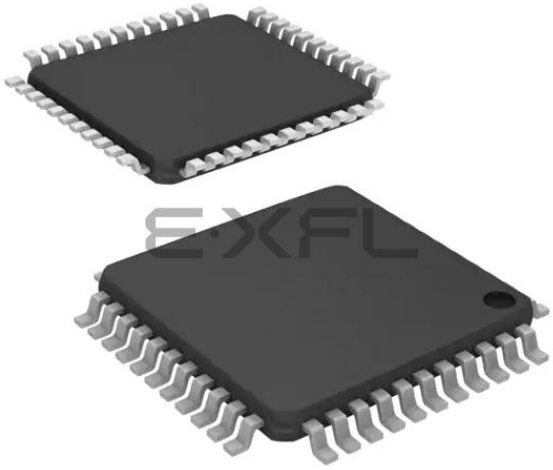

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 31x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19176-i-pt

5.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory are controlled independently. Internal access to the program memory is unaffected by any code protection setting.

5.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Words. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Self-writing the program memory is dependent upon the write protection setting. See **Section 5.4 "Write Protection"** for more information.

5.3.2 DATA MEMORY PROTECTION

The entire data EEPROM is protected from external reads and writes by the $\overline{WRTD}$ bit in the Configuration Words. When $\overline{WRTD}$ = 0, external reads and writes of EEPROM memory are inhibited and a read will return all '0's. The CPU can continue to read and write EEPROM memory, regardless of the protection bit settings.

5.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The $\overline{WRTAPP}$, $\overline{WRTSAF}$, $\overline{WRTB}$, $\overline{WRTC}$ bits in Configuration Words (Register 5-4) define whether the corresponding region of the program memory block is protected or not.

5.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 13.4.7 "NVMREG Access to Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Words"** for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F191XX Memory Programming Specification"* (DS40001880).

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON1	—	NOSC<2:0>			NDIV<3:0>				152
OSCCON2	—	COSC<2:0>			CDIV<3:0>				152
OSCCON3	CWSHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	154
OSCFRQ	—	—	—	—	—	HFFRQ<2:0>			157
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	155
OSCTUNE	—	—	HFTUN<5:0>						157
OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	156
ACTCON	ACTEN	ACTUD	—	—	ACTLOCK	—	ACTORS		158

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	—	CSWEN	LCDPEN	$\overline{\text{VBATEN}}$	$\overline{\text{CLKOUTEN}}$	120
	7:0	—	RSTOSC<2:0>			—	FEXTOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

10.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) of the PIEx[y] registers for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIEx registers)

The PIR1, PIR2, PIR3, PIR4, PIR5, PIR6, PIR7 and PIR8 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while interrupts are enabled:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See **"Section 10.5 "Automatic Context Saving"**)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupts operation, refer to its peripheral chapter.

Note 1:	Individual interrupt flag bits are set, regardless of the state of any other enable bits.
2:	All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

10.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The interrupt is sampled during Q1 of the instruction cycle. The actual interrupt latency then depends on the instruction that is executing at the time the interrupt is detected. See Figure 10-2 and Figure 10-3 for more details.

10.6 Register Definitions: Interrupt Control

REGISTER 10-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R/W-1/1
GIE	PEIE	—	—	—	—	—	INTEDG
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH WINDOWED WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON1	—	NOSC<2:0>			NDIV<3:0>				152
OSCCON2	—	COSC<2:0>			CDIV<3:0>				152
OSCCON3	CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	154
PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	140
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	50
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	196
WDTCON1	—	WDTCS<2:0>			—	WINDOW<2:0>			197
WDTPSL	PSCNT<7:0>								198
WDTPSH	PSCNT<15:8>								198
WDTTMR	—	WDTTMR<3:0>				STATE	PSCNT<17:16>		198

Legend: – = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 12-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	—	CSWEN	LCDPEN	$\overline{\text{VBATEN}}$	$\overline{\text{CLKOUTEN}}$	120
	7:0	—	RSTOSC<2:0>			—	FEXTOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

14.2.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 14-8) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 39-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

14.2.6 ANALOG CONTROL

The ANSELA register (Register 14-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.2.7 WEAK PULL-UP CONTROL

The WPUA register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.2.8 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 16-5: PMD4: PMD CONTROL REGISTER 4

R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
UART2MD	UART1MD	—	MSSP1MD	—	—	—	CWG1MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **UART2MD:** Disable EUSART2 bit
1 = EUSART2 module disabled
0 = EUSART2 module enabled

bit 6 **UART1MD:** Disable EUSART1 bit
1 = EUSART1 module disabled
0 = EUSART1 module enabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **MSSP1MD:** Disable MSSP1 bit
1 = MSSP1 module disabled
0 = MSSP1 module enabled

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **CWG1MD:** Disable CWG1 bit
1 = CWG1 module disabled
0 = CWG1 module enabled

REGISTER 19-8: ADPCH: ADC POSITIVE CHANNEL SELECTION REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ADPCH<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented**: Read as '0'

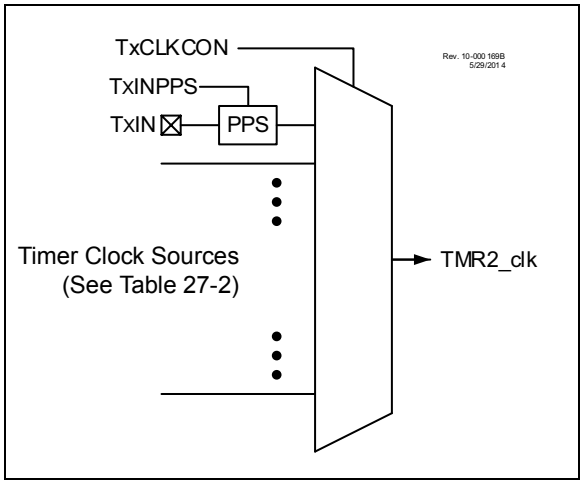
bit 5-0 **ADPCH<5:0>**: ADC Positive Input Channel Selection bits

ADPCH <5:0>	Device Pin Count			ADC Input Connection
	28	40	48	
0x00	•	•	•	RA0
0x01	•	•	•	RA1
0x02	•	•	•	RA2
0x03	•	•	•	RA3
0x04	•	•	•	RA4
0x05	—	—	—	RA5
0x06	•	•	•	RA6
0x07	•	•	•	RA7
0x08	•	•	•	RB0
0x09	•	•	•	RB1
0x0A	•	•	•	RB2
0x0B	•	•	•	RB3
0x0C	•	•	•	RB4
0x0D	•	•	•	RB5
0x0E	•	•	•	RB6
0x0F	•	•	•	RB7
0x10	—	—	—	RC0
0x11	—	—	—	RC1
0x12	•	•	•	RC2
0x13	•	•	•	RC3
0x14	•	•	•	RC4
0x15	—	—	—	RC5
0x16	•	•	•	RC6
0x17	•	•	•	RC7
0x18	—	•	•	RD0
0x19	—	•	•	RD1
0x1A	—	•	•	RD2
0x1B	—	•	•	RD3
0x1C	—	•	•	RD4
0x1D	—	•	•	RD5
0x1E	—	•	•	RD6
0x1F	—	•	•	RD7

ADPCH <5:0>	Device Pin Count			ADC Input Connection
	28	40	48	
0x20	—	•	•	RE0
0x21	—	•	•	RE1
0x22	—	•	•	RE2
0x23	—	—	—	RE3
0x24	—	—	—	RE4
0x25	—	—	—	RE5
0x26	—	—	—	RE6
0x27	—	—	—	RE7
0x28	—	—	•	RF0
0x29	—	—	•	RF1
0x2A	—	—	•	RF2
0x2B	—	—	•	RF3
0x2C	—	—	•	RF4
0x2D	—	—	•	RF5
0x2E	—	—	•	RF6
0x2F	—	—	•	RF7
0x30	—	—	—	RG0
0x31	—	—	—	RG1
0x32	—	—	—	RG2
0x33	—	—	—	RG3
0x34	—	—	—	RG4
0x35	—	—	—	RG5
0x36	—	—	—	RG6
0x37	—	—	—	RG7
0x38	—	—	—	—
0x39	VLCD3 divided by 4(4)			
0x3A	VBAT divided by 3(5)			
0x3B	AVSS (Analog Ground)			
0x3C	Temperature Indicator(3)			
0x3D	DAC1 Output(1)			
0x3E	FVR Buffer 1(2)			
0x3F	FVR Buffer 2(2)			

Note 1: See **Section 19.0 "Analog-to-Digital Converter with Computation (ADC2) Module"** for more information.
2: See **Section 18.0 "Fixed Voltage Reference (FVR)"** for more information.
3: See **Section 20.0 "Temperature Indicator Module (TIM)"** for more information.
4: See **Section 35.0 "Liquid Crystal Display (LCD) Controller"** for more information.
5: See **Section 8.0 "Resets and Vbat"** for more information.

FIGURE 27-2: TIMER2/4 CLOCK SOURCE BLOCK DIAGRAM



27.1 Timer2/4 Operation

Timer2 operates in three major modes:

- Free Running Period
- One-shot
- Monostable

Within each mode there are several options for starting, stopping, and reset. Table 27-1 lists the options.

In all modes, the TMR2 count register is incremented on the rising edge of the clock signal from the programmable prescaler. When TMR2 equals T2PR, a high level is output to the postscaler counter. TMR2 is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a TMR2 count Reset. In Gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the TMR2 count is reset on either the level or edge from the external source.

The TMR2 and T2PR registers are both directly readable and writable. The TMR2 register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset
- External Reset Source event that resets the timer.

Note:	TMR2 is not cleared when T2CON is written.

27.1.1 FREE RUNNING PERIOD MODE

The value of TMR2 is compared to that of the Period register, T2PR, on each TMR2_clk cycle. When the two values match, the comparator resets the value of TMR2 to 00h on the next rising TMR2_clk edge and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS<4:0> bits of the TMRxCON1 register, a one TMR2_clk period wide pulse occurs on the TMR2_postscaled output, and the postscaler count is cleared.

27.1.2 ONE-SHOT MODE

The One-Shot mode is identical to the Free Running Period mode except that the ON bit is cleared and the timer is stopped when TMR2 matches T2PR and will not restart until the T2ON bit is cycled off and on. Postscaler OUTPS<4:0> values other than 0 are meaningless in this mode because the timer is stopped at the first period event and the postscaler is reset when the timer is restarted.

27.1.3 MONOSTABLE MODE

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

27.2 Timer2/4 Output

The Timer2 module's primary output is TMR2_postscaled, which pulses for a single TMR2_clk period when the postscaler counter matches the value in the OUTPS bits of the TMR2CON register. The T2PR postscaler is incremented each time the TMR2 value matches the T2PR value. This signal can be selected as an input to several other input modules:

- The ADC module, as an Auto-conversion Trigger
- COG, as an auto-shutdown source

In addition, the Timer2 is also used by the CCP module for pulse generation in PWM mode. Both the actual TMR2 value as well as other internal signals are sent to the CCP module to properly clock both the period and pulse width of the PWM signal. See **Section 29.0 "Capture/Compare/PWM Modules"** for more details on setting up Timer2/4 for use with the CCP, as well as the timing diagrams in **Section 27.5 "Operation Examples"** for examples of how the varying Timer2 modes affect CCP PWM output.

27.3 External Reset Sources

In addition to the clock source, the Timer2 also takes in an external Reset source. This external Reset source is selected for Timer2 with the T2RST register. This source can control starting and stopping of the timer, as well as resetting the timer, depending on which mode the timer is in. The mode of the timer is controlled by the MODE<4:0> bits of the TMRxHLT register. Edge-Triggered modes require six Timer clock periods between external triggers. Level-Triggered modes require the triggering level to be at least three Timer clock periods long. External triggers are ignored while in Debug Freeze mode.

29.2.1 CCPX PIN CONFIGURATION

The software must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxyPPS registers. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more details.

The CCP output can also be used as an input for other peripherals.

Note:	Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

29.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 26.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

29.2.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxIF). When this flag is set and a match occurs, an Auto-conversion Trigger can take place if the CCP module is selected as the conversion trigger source.

Refer to **Section 19.2.6 "ADC Conversion Procedure (Basic Mode)"** for more information.

Note:	Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring

29.2.4 COMPARE DURING SLEEP

Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

29.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 29-3 shows a typical waveform of the PWM signal.

29.3.1 STANDARD PWM OPERATION

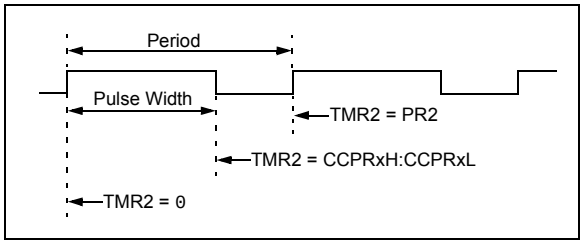
The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 29-4 shows a simplified block diagram of PWM operation.

Note:	The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

FIGURE 29-3: CCP PWM OUTPUT SIGNAL



31.10 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in Figure 31-12.

31.10.1 SHUTDOWN

The shutdown state can be entered by either of the following two methods:

- Software generated
- External input

31.10.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit of the CWG1AS0 register will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event.

31.10.2 EXTERNAL INPUT SOURCE

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the selected override levels without software delay. Several input sources can be selected to cause a shutdown condition. All input sources are active-low. The sources are:

- Comparator C1OUT_sync
- Comparator C2OUT_sync
- Timer2 – TMR2_postscaled
- CWG1IN input pin

Shutdown inputs are selected using the CWG1AS1 register (Register 31-6).

Note:	Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

31.11 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep when all the following conditions are met:

- CWG module is enabled
- Input source is active
- HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, then the CPU will go idle during Sleep, but the HFINTOSC will remain active and the CWG will continue to operate. This will have a direct effect on the Sleep mode current.

31.13 Register Definitions: CWG Control

Long bit name prefixes for the CWG peripherals are shown in **Section 1.1 "Register and Bit Naming Conventions"**.

REGISTER 31-1: CWG1CON0: CWG1 CONTROL REGISTER 0

R/W-0/0	R/W/HC-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
EN	LD(1)	—	—	—	MODE<2:0>		
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **EN:** CWG1 Enable bit
- 1 = Module is enabled
- 0 = Module is disabled

bit 6 **LD:** CWG1 Load Buffer bits(1)
- 1 = Buffers to be loaded on the next rising/falling event
- 0 = Buffers not loaded

bit 5-3 **Unimplemented**: Read as '0'

bit 2-0 **MODE<2:0>:** CWG1 Mode bits
- 111 = Reserved
- 110 = Reserved
- 101 = CWG outputs operate in Push-Pull mode
- 100 = CWG outputs operate in Half-Bridge mode
- 011 = CWG outputs operate in Reverse Full-Bridge mode
- 010 = CWG outputs operate in Forward Full-Bridge mode
- 001 = CWG outputs operate in Synchronous Steering mode
- 000 = CWG outputs operate in Steering mode

Note 1: This bit can only be set after EN = 1 and cannot be set in the same instruction that EN is set.

33.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPxCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

TABLE 33-1: I²C BUS TERMS

TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by the master.
Multi-master	A bus with more than one device that can initiate data transfers.
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.
Idle	No master is controlling the bus, and both SDA and SCL lines are high.
Active	Any time one or more master devices are controlling the bus.
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPxADD.
Write Request	Slave receives a matching address with R/$\overline{W}$ bit clear, and is ready to clock in data.
Read Request	Master sends an address byte with the R/$\overline{W}$ bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.
Clock Stretching	When a device on the bus hold SCL low to stall communication.
Bus Collision	Any time the SDA line is sampled low by the module while it is outputting and expected high state.

33.4.5 START CONDITION

The I²C specification defines a Start condition as a transition of SDA from a high to a low state while SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 33-12 shows wave forms for Start and Stop conditions.

33.4.6 STOP CONDITION

A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

Note: At least one SCL low time must appear before a Stop is valid, therefore, if the SDA line goes low then high again while the SCL line stays high, only the Start condition is detected.

33.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 33-13 shows the wave form for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/$\overline{W}$ bit set. The slave logic will then hold the clock and prepare to clock out data.

33.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

34.6 Register Definitions: EUSART Control

REGISTER 34-1: TXxSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Unused in this mode – value ignored
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send SYNCH BREAK on next transmission – Start bit, followed by 12 '0' bits, followed by Stop bit; cleared by hardware upon completion
0 = SYNCH BREAK transmission disabled or completed
Synchronous mode:
Unused in this mode – value ignored

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode – value ignored

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

35.7.4 35.6.4 INTERNAL RESISTOR WITH EXTERNAL CAPACITORS

In this configuration, the user can use the internal resistor ladders to generate the LCD bias levels, and use external capacitors to guard again burst currents. It is recommend the user utilize the external capacitors when driving large glass panels with a large pixels and a high pixel count. The external capacitors will help dampen current spikes during segment switching. Contrast is adjusted using the LCDCST<2:0> bits. The CFLYx pins are available as a GPIO. See Figure 35-7 for supported connections.

External capacitors can be used when voltage to the internal resistor ladder is supplied by VDD (LCDVSRC<3:0> = 0101) or an external source (LCDVSRC<3:0> = 0100). When supplying an external voltage to internal resistor ladder the external capacitors should be limited to VLCD2, and VLCD3.

35.9 Segment Enables

The LCDSENx registers are used to select the pin function for each segment pin. The selection allows the designated SEG pins to be configured as LCD segment driver pins. To configure the pin as a segment pin, the corresponding bits in the LCDSENx registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSENx registers overrides any bit settings in the corresponding TRIS register.

Note:	On a Power-on Reset, these pins are configured as digital I/O.

35.10 Pixel Control

The LCDDATAx registers contain bits that define the state of each pixel. Each bit defines one unique pixel. Table 35-2 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

35.11 LCD Frame Frequency

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

TABLE 35-9: FRAME FREQUENCY FORMULAS

Multiplex	Frame Frequency =
Static ('0001')	Clock Source/(4 x 1 x (LP<3:0> + 1))
1/2 ('0010')	Clock Source/(2 x 2 x (LP<3:0> + 1))
1/3 ('0011')	Clock Source/(1 x 3 x (LP<3:0> + 1))
1/4 ('0100')	Clock Source/(1 x 4 x (LP<3:0> + 1))
1/5 ('0101')	Clock Source/(1 x 5 x (LP<3:0> + 1))
1/6 ('0110')	Clock Source/(1 x 6 x (LP<3:0> + 1))
1/7 ('0111')	Clock Source/(1 x 7 x (LP<3:0> + 1))
1/8 ('1000')	Clock Source/(1 x 8 x (LP<3:0> + 1))

Note: The clock source is SOSC/32 or LFINTOSC/32.

35.12 LCD Waveform Generation

LCD waveform generation is based on the theory that the net AC voltage across the dark pixel should be maximized and the net AC voltage across the clear pixel should be minimized. The net DC voltage across any pixel should be zero.

The COM signal represents the time slice for each common, while the SEG contains the pixel data.

The pixel signal (COM-SEG) will have no DC component and can take only one of the two rms values. The higher rms value will create a dark pixel and a lower rms value will create a clear pixel.

As the number of commons increases, the delta between the two rms values decreases. The delta represents the maximum contrast that the display can have.

The LCDs can be driven by two types of waveforms: Type-A and Type-B. In a Type-A waveform, the phase changes within each common type, whereas a Type-B waveform's phase changes on each frame boundary. Thus, Type-A waveforms maintain 0 VDC over a single frame, whereas Type-B waveforms take two frames.

Figure 35-8 through Figure 35-19 provide waveforms for static, half-multiplex, one-third multiplex and quarter multiplex drives for Type-A and Type-B waveforms.

TABLE 35-10: SUMMARY OF REGISTERS ASSOCIATED WITH LCD MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182
PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
PMD5	—	SMT1MD	LCDMD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	274
LCDCON	LCDEN	SLPEN	WERR	CS	LMUX<3:0>				622
LCDPS	WFT	—	LCDA	WA	LP<3:0>				623
LCDSE0	SE07	SE06	SE05	SE04	SE03	SE02	SE01	SE00	624
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	624
LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	624
LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	624
LCDSE4	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	624
LCDSE5	SE47	SE46	SE45	SE44	SE43	SE42	SE41	SE40	624
LCDVCON1	LPEN	EN5V	—	—	—	BIAS<2:0>			625
LCDVCON2	—	—	—	—	LCDVSRC<3:0>				626
LCDREF	—	—	—	—	—	LCDCST<2:0>			628
LCDRL	LRLAP<1:0>		LRLBP<1:0>		LCDIRI	LRLAT<2:0>			627
LCDDATA0	S07C0	S06C0	—	S04C0	S03C0	S02C0	S01C0	S00C0	624
LCDDATA1	S15C0	S14C0	S13C0	—	S11C0	S10C0	S09C0	S08C0	624
LCDDATA2	S23C0	S22C0	—	S20C0	S19C0	S18C0	—	—	624
LCDDATA3	S31C0	S30C0	S29C0	S28C0	S27C0	S26C0	S25C0	S24C0	624
LCDDATA4	—	—	—	—	—	S34C0	S33C0	S32C0	624
LCDDATA5	S47C0	S46C0	S45C0	S44C0	S43C0	S42C0	S41C0	S40C0	624
LCDDATA6	S07C1	S06C1	—	S04C1	S03C1	S02C1	S01C1	S00C1	624
LCDDATA7	S15C1	S14C1	S13C1	—	S11C1	S10C1	S09C1	S08C1	624
LCDDATA8	S23C1	S22C1	—	S20C1	S19C1	S18C1	—	—	624
LCDDATA9	S31C1	S30C1	S29C1	S28C1	S27C1	S26C1	S25C1	S24C1	624
LCDDATA10	—	—	—	—	—	S34C1	S33C1	S32C1	624
LCDDATA11	S47C1	S46C1	S45C1	S44C1	S43C1	S42C1	S41C1	S40C1	624
LCDDATA12	S07C2	S06C2	—	S04C2	S3C2	S2C2	S01C2	S00C2	624
LCDDATA13	S15C2	S14C2	S13C2	—	S11C2	S10C2	S09C2	S08C2	624
LCDDATA14	S23C2	S22C2	—	S20C2	S19C2	S18C2	—	—	624
LCDDATA15	S31C2	S30C2	S29C2	S28C2	S27C2	S26C2	S25C2	S24C2	624
LCDDATA16	—	—	—	—	—	S34C2	S33C2	S32C2	624
LCDDATA17	S47C2	S46C2	S45C2	S44C2	S43C2	S42C2	S41C2	S40C2	624
LCDDATA18	S15C3	S14C3	S13C3	—	SE11C3	S10C3	S09C3	S08C3	624
LCDDATA19	S23C3	S22C3	—	S20C3	S19C3	S18C3	—	—	624
LCDDATA20	S31C3	S30C3	S29C3	S28C3	S27C3	S26C3	S25C3	S24C3	624
LCDDATA21	—	—	—	—	—	S34C3	S33C3	S32C3	624
LCDDATA22	S47C3	S46C3	S45C3	S44C3	S43C3	S42C3	S41C3	S40C3	624
LCDDATA23	S07C4	S06C4	—	S04C4	S03C4	S02C4	S01C4	S00C4	624
LCDDATA24	S15C4	S14C4	S13C4	—	S11C4	S10C4	S09C4	S08C4	624
LCDDATA25	S23C4	S22C4	—	S20C4	S19C4	S18C4	—	—	624
LCDDATA26	S31C4	S30C4	S29C4	S28C4	S27C4	S26C4	S25C4	S24C4	624
LCDDATA27	—	—	—	—	—	S34C4	S33C4	S32C4	624
LCDDATA28	S47C4	S46C4	S45C4	S44C4	S43C4	S42C4	S41C4	S40C4	624
LCDDATA29	S07C5	S06C5	—	S04C5	S03C5	S02C5	S01C5	S00C5	624
LCDDATA30	S15C5	S14C5	S13C5	—	S11C5	S10C5	S09C5	S08C5	624
LCDDATA31	S23C5	S22C5	—	S20C5	S19C5	S18C5	—	—	624
LCDDATA32	S31C5	S30C5	S29C5	S28C5	S27C5	S26C5	S25C5	S24C5	624
LCDDATA33	—	—	—	—	—	S34C5	S33C5	S32C5	624

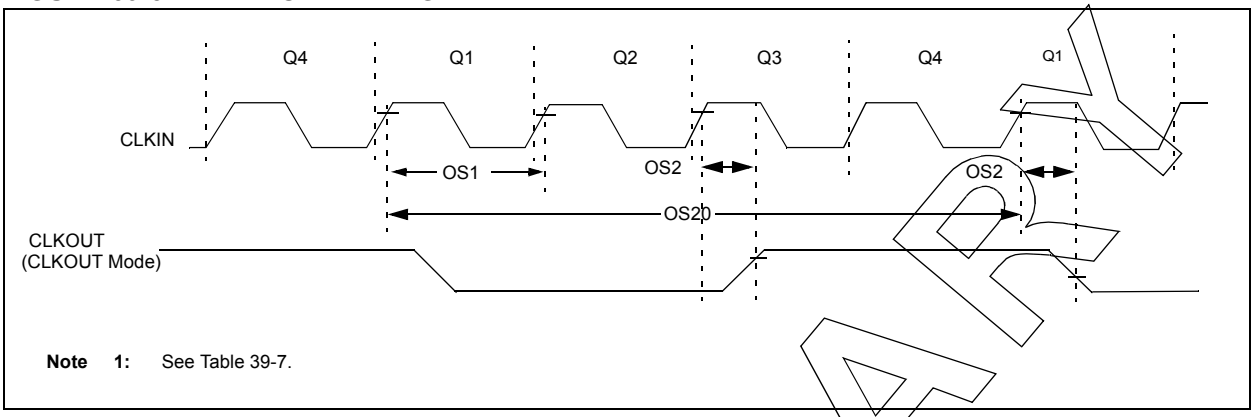
TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
212h	—	Unimplemented								
213h	—	Unimplemented								
214h	—	Unimplemented								
215h	—	Unimplemented								
216h	—	Unimplemented								
217h	—	Unimplemented								
218h	—	Unimplemented								
219h	—	Unimplemented								
21Ah	—	Unimplemented								
21Bh	—	Unimplemented								
21Ch	—	Unimplemented								
21Dh	—	Unimplemented								
21Eh	CCPTMRS0	P4TSEL<1:0>		P3TSEL1:0>		C2TSEL<1:0>		C1TSEL<1:0>		461
21Fh	—	Unimplemented								
28Ch	T2TMR	TMR2								
28Dh	T2PR	PR2								
28Eh	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				404
28Fh	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					405
290h	T2CLKCON	—	—	—	—	CS<3:0>				403
291h	T2RST	—	—	—	—	RSEL<3:0>				406
292h	T4TMR	TMR4								
293h	T4PR	PR4								
294h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				404
295h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					405
296h	T4CLKCON	—	—	—	—	CS<3:0>				403
297h	T4RST	—	—	—	—	RSEL<3:0>				406
298h	—	Unimplemented								
299h	—	Unimplemented								
29Ah	—	Unimplemented								
29Bh	—	Unimplemented								
29Ch	—	Unimplemented								
29Dh	—	Unimplemented								
29Eh	—	Unimplemented								
29Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

FIGURE 39-5: CLOCK TIMING



Note 1: See Table 39-7.

TABLE 39-7: EXTERNAL CLOCK/OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
ECL Oscillator							
OS1	F_{ECL}	Clock Frequency	—	—	500	kHz	
OS2	T_{ECL_DC}	Clock Duty Cycle	40	—	60	%	
ECM Oscillator							
OS3	F_{ECM}	Clock Frequency	—	—	4	MHz	
OS4	T_{ECM_DC}	Clock Duty Cycle	40	—	60	%	
ECH Oscillator							
OS5	F_{ECH}	Clock Frequency	—	—	32	MHz	
OS6	T_{ECH_DC}	Clock Duty Cycle	40	—	60	%	
System Oscillator							
OS20	F_{OSC}	System Clock Frequency	—	—	32	MHz	**(Note 2, Note 3)**
OS21	F_{CY}	Instruction Frequency	—	FOSC/4	—	MHz	
OS22	T_{CY}	Instruction Period	125	$1/F_{CY}$	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

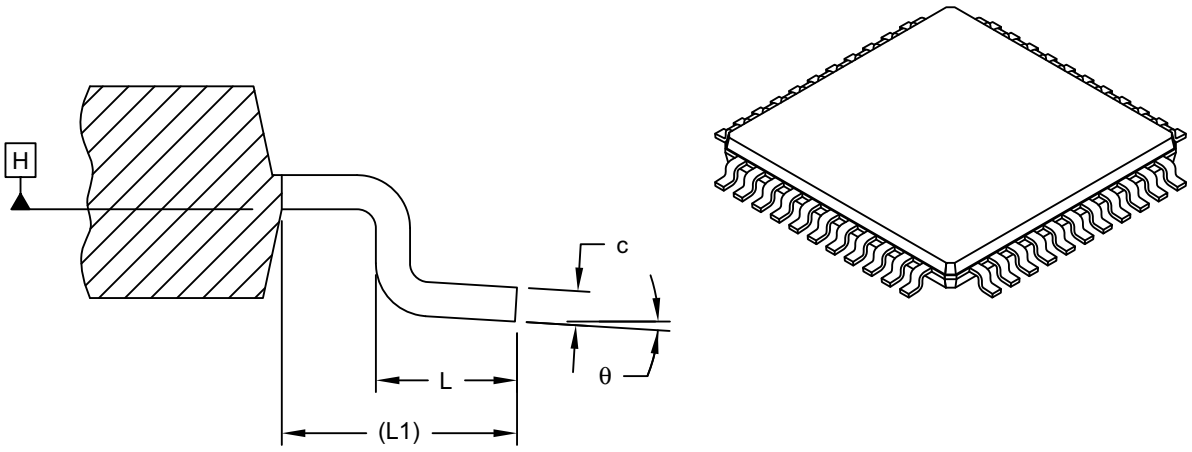
Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: The system clock frequency (FOSC) is selected by the "main clock switch controls" as described in **Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)"**.

3: The system clock frequency (FOSC) must meet the voltage requirements defined in the **Section 39.2 "Standard Operating Conditions"**.

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2