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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19185-i-pt

TABLE 5: 48-PIN ALLOCATION TABLE (PIC16(L)F19185/86)

I/O(2)	48-Pin TQFP/QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RA0	21	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG0	IOCA0	—	Y	—
RA1	22	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	SEG1	IOCA1	—	Y	—
RA2	23	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG2	IOCA2	—	Y	—
RA3	24	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	SEG3	IOCA3	—	Y	—
RA4	25	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG4 COM3	IOCA4	—	Y	—
RA5	26	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	—	IOCA5	—	Y	VBAT
RA6	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG6	IOCA6	—	Y	CLKOUT OSC2
RA7	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	SEG7	IOCA7	—	Y	OSC1 CLKIN
RB0	8	ANB0	—	C2IN1+	ZCD	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG8	IOCB0	—	Y	INTPPS
RB1	9	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG9	IOCB1	HIB1	Y	—
RB2	10	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG10 CFLY1	IOCB2	—	Y	—
RB3	11	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG11 CFLY2	IOCB3	—	Y	—
RB4	16	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM0	IOCB4	—	Y	—
RB5	17	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG13 COM1	IOCB5	—	Y	—
RB6	18	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	SEG14	IOCB6	—	Y	ICDCLK/ ICSPCLK
RB7	19	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	SEG15	IOCB7	—	Y	ICDDAT/ ICSPDAT

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 5											
CPU CORE REGISTERS; see Table 4-3 for specifics											
28Ch	T2TMR	TMR2								0000 0000	0000 0000
28Dh	T2PR	PR2								1111 1111	1111 1111
28Eh	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
28Fh	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
290h	T2CLKCON	—	—	—	—	CS<3:0>				0000 0000	0000 0000
291h	T2RST	—	—	—	—	RSEL<3:0>				0000 0000	0000 0000
292h	T4TMR	TMR4								0000 0000	0000 0000
293h	T4PR	PR4								1111 1111	1111 1111
294h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
295h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
296h	T4CLKCON	—	—	—	—	CS<3:0>				0000 0000	0000 0000
297h	T4RST	—	—	—	—	RSEL<3:0>				0000 0000	0000 0000
298h	—	Unimplemented								---- ----	---- ----
299h	—	Unimplemented								---- ----	---- ----
29Ah	—	Unimplemented								---- ----	---- ----
29Bh	—	Unimplemented								---- ----	---- ----
29Ch	—	Unimplemented								---- ----	---- ----
29Dh	—	Unimplemented								---- ----	---- ----
29Eh	—	Unimplemented								---- ----	---- ----
29Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 13											
CPU CORE REGISTERS; see Table 4-3 for specifics											
68Ch	—	Unimplemented								---- ----	---- ----
68Dh	—	Unimplemented								---- ----	---- ----
68Eh	—	Unimplemented								---- ----	---- ----
68Fh	—	Unimplemented								---- ----	---- ----
690h	—	Unimplemented								---- ----	---- ----
691h	—	Unimplemented								---- ----	---- ----
692h	—	Unimplemented								---- ----	---- ----
693h	—	Unimplemented								---- ----	---- ----
694h	—	Unimplemented								---- ----	---- ----
695h	—	Unimplemented								---- ----	---- ----
696h	—	Unimplemented								---- ----	---- ----
697h	—	Unimplemented								---- ----	---- ----
698h	—	Unimplemented								---- ----	---- ----
699h	—	Unimplemented								---- ----	---- ----
69Ah	—	Unimplemented								---- ----	---- ----
69Bh	—	Unimplemented								---- ----	---- ----
69Ch	—	Unimplemented								---- ----	---- ----
69Dh	—	Unimplemented								---- ----	---- ----
69Eh	—	Unimplemented								---- ----	---- ----
69Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 15											
CPU CORE REGISTERS; see Table 4-3 for specifics											
78Ch	—	Unimplemented								---- ----	---- ----
78Dh	—	Unimplemented								---- ----	---- ----
78Eh	—	Unimplemented								---- ----	---- ----
78Fh	—	Unimplemented								---- ----	---- ----
790h	—	Unimplemented								---- ----	---- ----
791h	—	Unimplemented								---- ----	---- ----
792h	—	Unimplemented								---- ----	---- ----
793h	—	Unimplemented								---- ----	---- ----
794h	—	Unimplemented								---- ----	---- ----
795h	—	Unimplemented								---- ----	---- ----
796h	PMD0	SYSCMD	FVRMD	ACTMD	—	—	NVMMD	—	IOCMD	000- -0-0	000- -0-0
797h	PMD1	—	—	—	TMR4MD	—	TMR2MD	TMR1MD	TMR0MD	---0 -000	0000 0000
798h	PMD2	RTCCMD	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	000- -000	000- -000
799h	PMD3	—	—	—	—	PWM4MD	PWM3MD	CCP2MD	CCP1MD	0000 0000	0000 0000
79Ah	PMD4	UART2MD	UART1MD	—	MSSP1MD	—	—	—	CWG1MD	00-0 ---0	00-0 ---0
79Bh	PMD5	—	SMT1MD	LCDMD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	-000 000-	-000 000-
79Ch	—	Unimplemented								---- ----	---- ----
79Dh	—	Unimplemented								---- ----	---- ----
79Eh	—	Unimplemented								---- ----	---- ----
79Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 29											
CPU CORE REGISTERS; see Table 4-3 for specifics											
E8Ch	VB0GPR	VB0GPR								0000 0000	uuuu uuuu
E8Dh	VB1GPR	VB1GPR								0000 0000	uuuu uuuu
E8Eh	VB2GPR	VB2GPR								0000 0000	uuuu uuuu
E8Fh	VB3GPR	VB3GPR								0000 0000	uuuu uuuu
E90h	—	Unimplemented								---- ----	---- ----
E91h	—	Unimplemented								---- ----	---- ----
E92h	—	Unimplemented								---- ----	---- ----
E93h	—	Unimplemented								---- ----	---- ----
E94h	—	Unimplemented								---- ----	---- ----
E95h	—	Unimplemented								---- ----	---- ----
E96h	—	Unimplemented								---- ----	---- ----
E97h	—	Unimplemented								---- ----	---- ----
E98h	—	Unimplemented								---- ----	---- ----
E99h	—	Unimplemented								---- ----	---- ----
E9Ah	—	Unimplemented								---- ----	---- ----
E9Bh	—	Unimplemented								---- ----	---- ----
E9Ch	—	Unimplemented								---- ----	---- ----
E9Dh	—	Unimplemented								---- ----	---- ----
E9Eh	—	Unimplemented								---- ----	---- ----
E9Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

10.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) of the PIEx[y] registers for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIEx registers)

The PIR1, PIR2, PIR3, PIR4, PIR5, PIR6, PIR7 and PIR8 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while interrupts are enabled:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See **"Section 10.5 "Automatic Context Saving"**)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupts operation, refer to its peripheral chapter.

Note 1:	Individual interrupt flag bits are set, regardless of the state of any other enable bits.
2:	All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

10.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The interrupt is sampled during Q1 of the instruction cycle. The actual interrupt latency then depends on the instruction that is executing at the time the interrupt is detected. See Figure 10-2 and Figure 10-3 for more details.

12.6 Operation During Sleep

When the device enters Sleep, the WWDT is cleared. If the WWDT is enabled during Sleep, the WWDT resumes counting. When the device exits Sleep, the WWDT is cleared again.

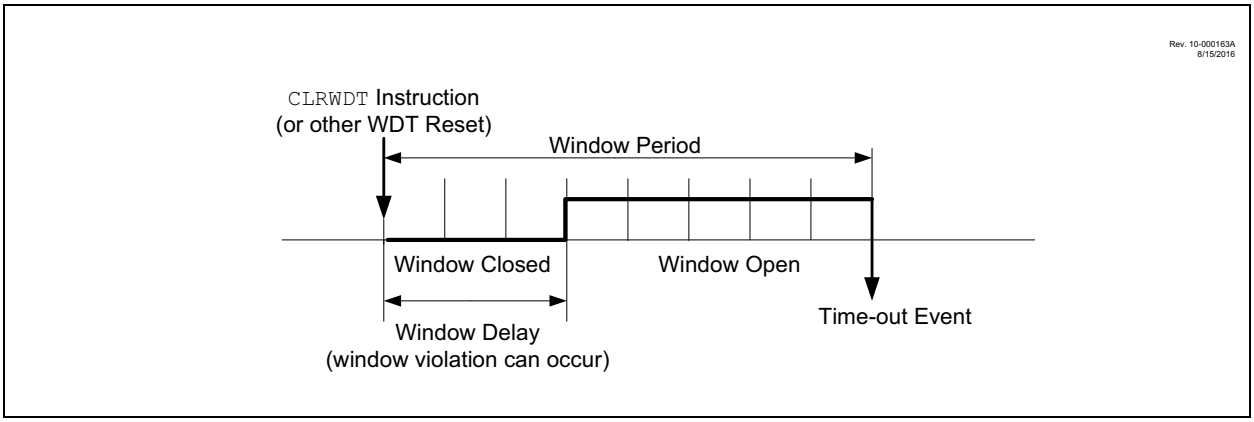
The WWDT remains clear until the OST, if enabled, completes. See **Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information on the OST.

When a WWDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the event. The $\overline{RWDT}$ bit in the PCON register can also be used. See **Section 4.3.2.1 "STATUS Register"** for more information.

TABLE 12-2: WWDT CLEARING CONDITIONS

Conditions	WWDT
WDTE<1:0> = 00	Cleared
WDTE<1:0> = 01 and SWDTEN = 0	
WDTE<1:0> = 10 and enter Sleep	
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = SOSC, EXTOSC, INTOSC	
Change INTOSC divider (IRCF bits)	Unaffected

FIGURE 12-2: WINDOW PERIOD AND DELAY



14.5 Register Definitions: PORTB

REGISTER 14-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **RB<7:0>**: PORTB I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

REGISTER 14-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TRISB<7:0>:** PORTB Tri-State Control bit
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

26.3 Timer Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

26.4 Secondary Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins SOSCI (input) and SOSCO (amplifier output). This internal circuit is designed to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the SOSCEN bit of the OSCEN register. The oscillator will continue to run during Sleep.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, SOSCEN should be set and a suitable delay observed prior to using Timer1 with the SOSC source. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

26.5 Timer Operation in Asynchronous Counter Mode

If the control bit $\overline{\text{SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 26.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

26.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

26.6 Timer Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using the time gate circuitry. This is also referred to as Timer Gate Enable.

The timer gate can also be driven by multiple selectable sources.

26.6.1 TIMER GATE ENABLE

The Timer Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer Gate Enable signal is enabled, the timer will increment on the rising edge of the Timer1 clock source. When Timer Gate Enable signal is disabled, the timer always increments, regardless of the GE bit. See Figure 26-3 for timing details.

TABLE 26-2: TIMER GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer Operation
↑	1	1	Counts
↑	1	0	Holds Count
↑	0	1	Holds Count
↑	0	0	Counts

REGISTER 28-5: SMTxWIN: SMTx WINDOW INPUT SELECT REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	WSEL<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented**: Read as '0'

bit 4-0 **WSEL<4:0>:** SMTx Window Selection bits

11111 = Reserved
•
•
•
10011 = Reserved
10010 = RTCC_Seconds
10001 = CLC4OUT
10000 = CLC3OUT
01111 = CLC2OUT
01110 = CLC1OUT
01101 = ZCDOUT
01100 = C2OUT
01011 = C1OUT
01010 = PWM4_out
01001 = PWM3_out
01000 = CCP1OUT
00111 = CCP1OUT
00110 = TMR4_postscaler
00101 = TMR2_postscaler
00100 = TMR0_overflow
00011 = SOSC
00010 = MFINTOSC (31 kHz)
00001 = LFINTOSC (31 kHz)
00000 = SMTWINx pin

FIGURE 28-10: WINDOWED MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM

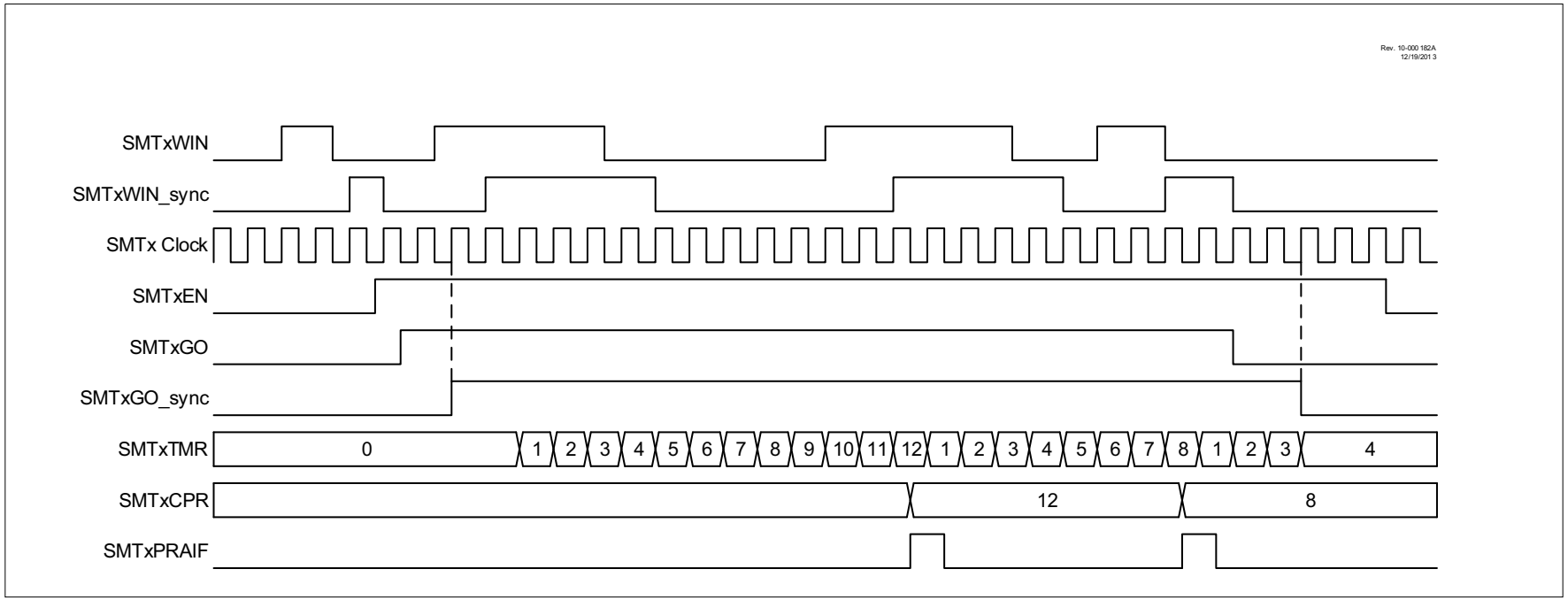
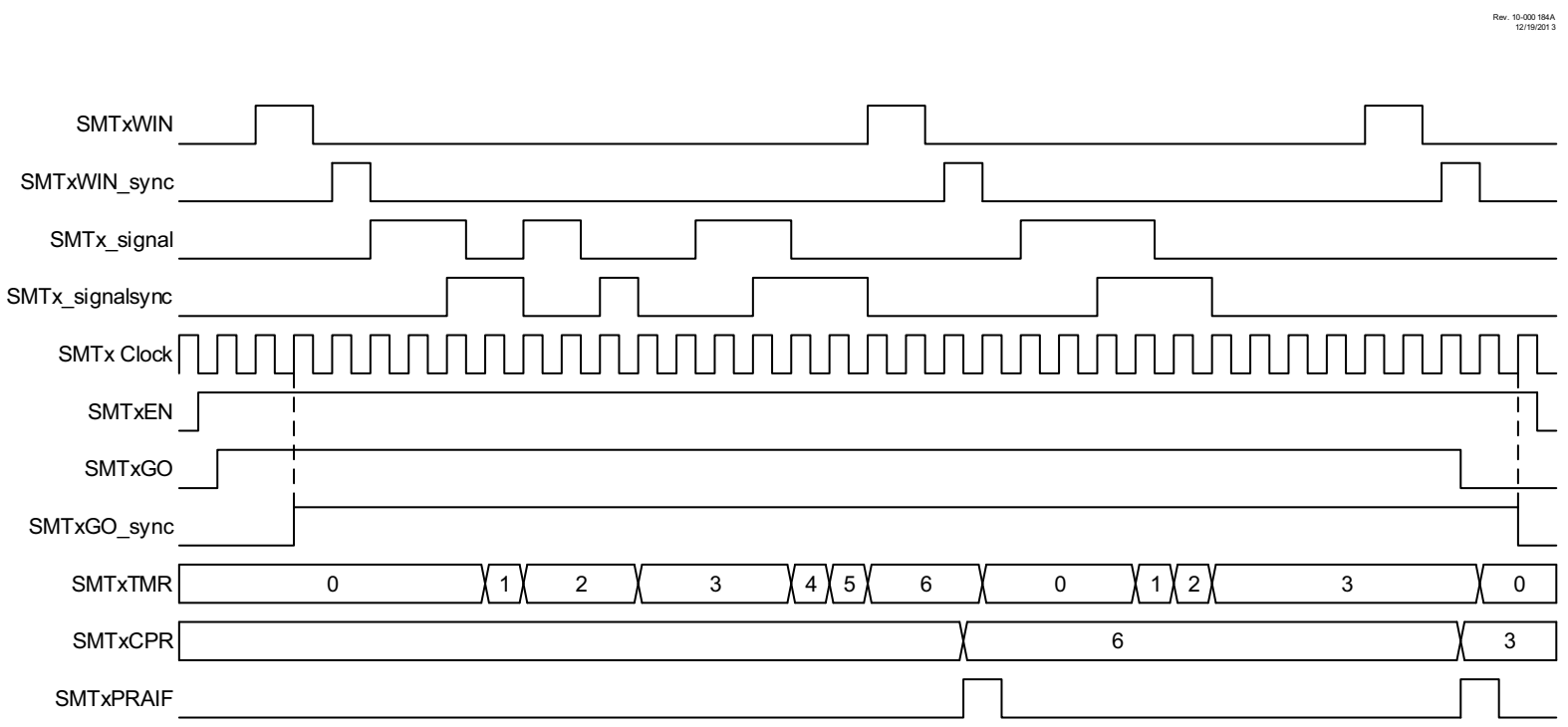


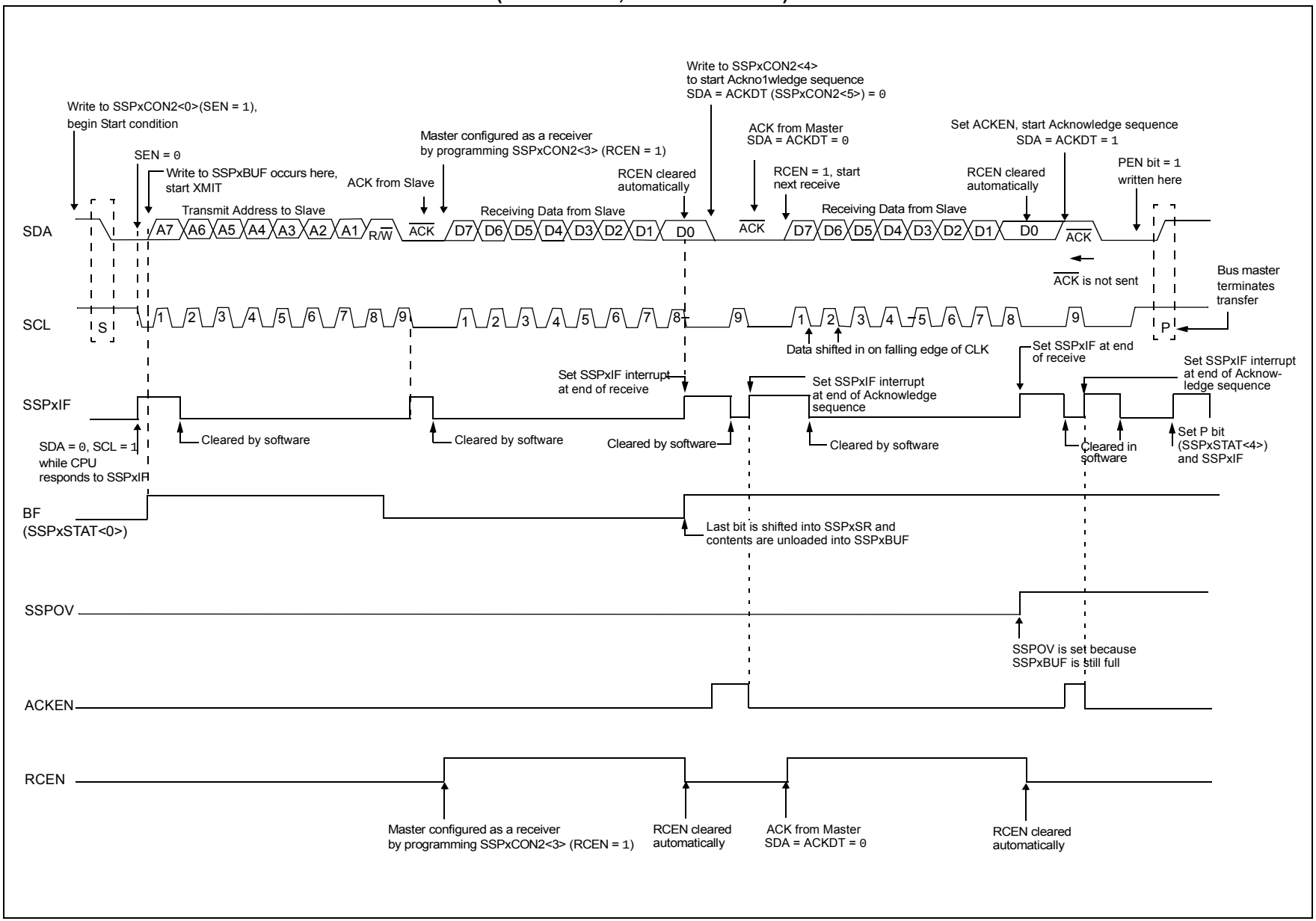
FIGURE 28-12: GATED WINDOWED MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM



28.7.8 CAPTURE MODE

Capture mode captures the Timer value based on a rising or falling edge on the SMTWINx input and triggers an interrupt. This mimics the capture feature of a CCP module. The timer begins incrementing upon the SMTxGO bit being set, and updates the value of the SMTxCPR register on each rising edge of SMTWINx, and updates the value of the CPW register on each falling edge of the SMTWINx. The timer is not reset by any hardware conditions in this mode and must be reset by software, if desired. See Figure 28-16 and Figure 28-17.

FIGURE 33-29: I^2C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



33.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPxCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into IDLE mode (Figure 33-30).

33.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

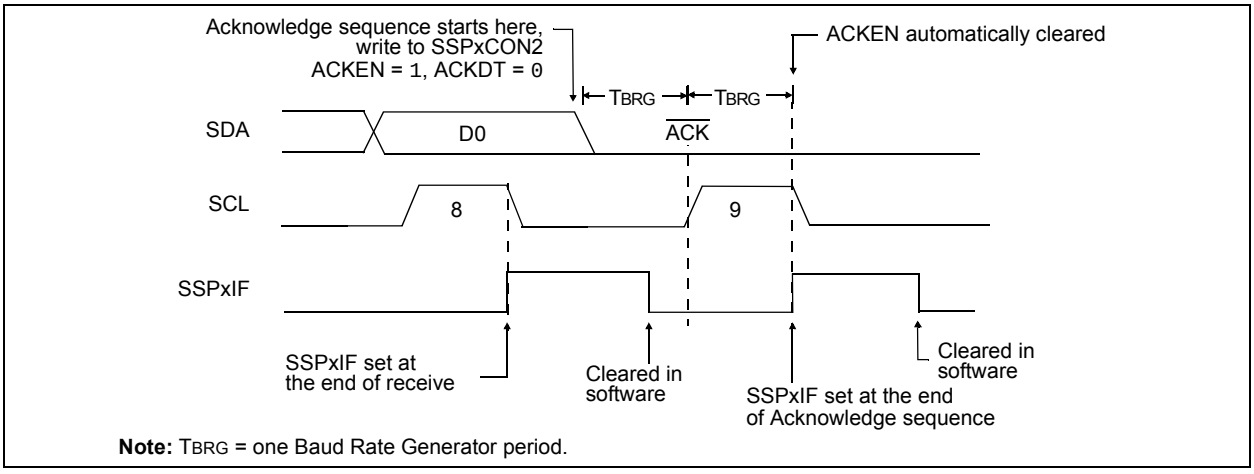
33.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPxCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 33-31).

33.6.9.1 WCOL Status Flag

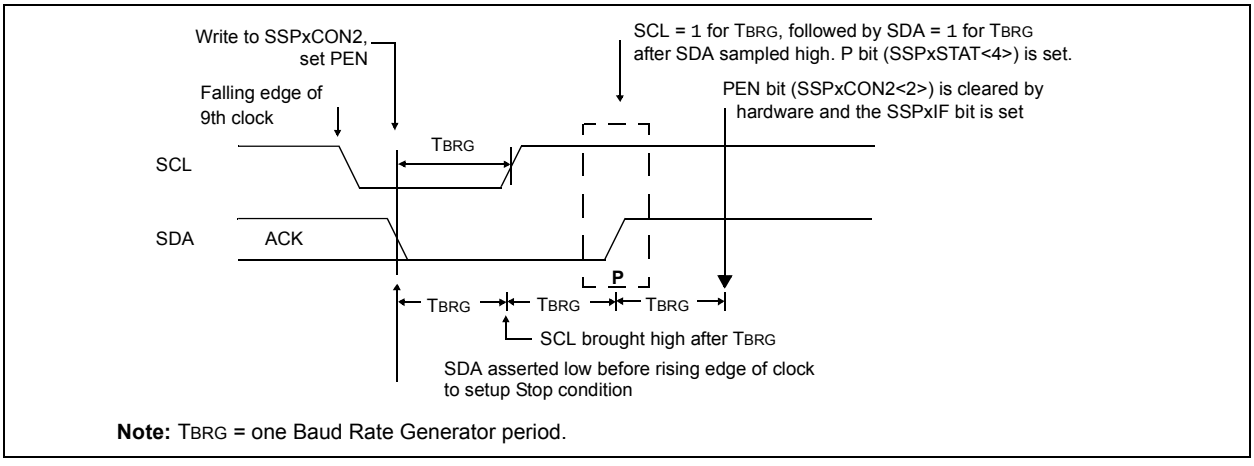
If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 33-30: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

FIGURE 33-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



Note: TBRG = one Baud Rate Generator period.

TABLE 35-5: LCDDATAX REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS (48-PIN)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDDATA0	SEG7 COM0	SEG6 COM0	—	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	—	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0
LCDDATA2	SEG23 COM0	SEG22 COM0	—	SEG20 COM0	SEG19 COM0	SEG18 COM0	—	—
LCDDATA3	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
LCDDATA4	—	—	—	—	—	SEG34 COM0	SEG33 COM0	SEG32 COM0
LCDDATA5	SEG47 COM0	SEG46 COM0	SEG45 COM0	SEG44 COM0	SEG43 COM0	SEG42 COM0	SEG41 COM0	SEG40 COM0
LCDDATA6	SEG7 COM1	SEG6 COM1	—	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1
LCDDATA7	SEG15 COM1	SEG14 COM1	SEG13 COM1	—	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1
LCDDATA8	SEG23 COM1	SEG22 COM1	—	SEG20 COM1	SEG19 COM1	SEG18 COM1	—	—
LCDDATA9	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
LCDDATA10	—	—	—	—	—	SEG34 COM1	SEG33 COM1	SEG32 COM1
LCDDATA11	SEG47 COM1	SEG46 COM1	SEG45 COM1	SEG44 COM1	SEG43 COM1	SEG42 COM1	SEG41 COM1	SEG40 COM1
LCDDATA12	SEG7 COM2	SEG6 COM2	—	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2
LCDDATA13	SEG15 COM2	SEG14 COM2	SEG13 COM2	—	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2
LCDDATA14	SEG23 COM2	SEG22 COM2	—	SEG20 COM2	SEG19 COM2	SEG18 COM2	—	—
LCDDATA15	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
LCDDATA16	—	—	—	—	—	SEG34 COM2	SEG33 COM2	SEG32 COM2
LCDDATA17	SEG47 COM2	SEG46 COM2	SEG45 COM2	SEG44 COM2	SEG43 COM2	SEG42 COM2	SEG41 COM2	SEG40 COM2
LCDDATA18	SEG7 COM3	SEG6 COM3	—	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3
LCDDATA19	SEG15 COM3	SEG14 COM3	SEG13 COM3	—	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3
LCDDATA20	SEG23 COM3	SEG22 COM3	—	SEG20 COM3	SEG19 COM3	SEG18 COM3	—	—
LCDDATA21	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3
LCDDATA22	—	—	—	—	—	SEG34 COM3	SEG33 COM3	SEG32 COM3
LCDDATA23	SEG47 COM3	SEG46 COM3	SEG45 COM3	SEG44 COM3	SEG43 COM3	SEG42 COM3	SEG41 COM3	SEG40 COM3
LCDDATA24	SEG7 COM4	SEG6 COM4	—	SEG4 COM4	SEG3 COM4	SEG2 COM4	SEG1 COM4	SEG0 COM4
LCDDATA25	SEG15 COM4	SEG14 COM4	SEG13 COM4	—	SEG11 COM4	SEG10 COM4	SEG9 COM4	SEG8 COM4
LCDDATA26	SEG23 COM4	SEG22 COM4	—	SEG20 COM4	SEG19 COM4	SEG18 COM4	—	—
LCDDATA27	SEG31 COM4	SEG30 COM4	SEG29 COM4	SEG28 COM4	SEG27 COM4	SEG26 COM4	SEG25 COM4	SEG24 COM4
LCDDATA28	—	—	—	—	—	SEG34 COM4	SEG33 COM4	SEG32 COM4
LCDDATA29	SEG47 COM4	SEG46 COM4	SEG45 COM4	SEG44 COM4	SEG43 COM4	SEG42 COM4	SEG41 COM4	SEG40 COM4
LCDDATA30	SEG7 COM5	SEG6 COM5	—	SEG4 COM5	SEG3 COM5	SEG2 COM5	SEG1 COM5	SEG0 COM5
LCDDATA31	SEG15 COM5	SEG14 COM5	SEG13 COM5	—	SEG11 COM5	SEG10 COM5	SEG9 COM5	SEG8 COM5
LCDDATA32	SEG23 COM5	SEG22 COM5	—	SEG20 COM5	SEG19 COM5	SEG18 COM5	—	—
LCDDATA33	SEG31 COM5	SEG30 COM5	SEG29 COM5	SEG28 COM5	SEG27 COM5	SEG26 COM5	SEG25 COM5	SEG24 COM5
LCDDATA34	—	—	—	—	—	SEG34 COM5	SEG33 COM5	SEG32 COM5
LCDDATA35	SEG47 COM5	SEG46 COM5	SEG45 COM5	SEG44 COM5	SEG43 COM5	SEG42 COM5	SEG41 COM5	SEG40 COM5
LCDDATA36	SEG7 COM6	SEG6 COM6	—	SEG4 COM6	SEG3 COM6	SEG2 COM6	SEG1 COM6	SEG0 COM6
LCDDATA37	SEG15 COM6	SEG14 COM6	SEG13 COM6	—	SEG11 COM6	SEG10 COM6	SEG9 COM6	SEG8 COM6
LCDDATA38	SEG23 COM6	SEG22 COM6	—	SEG20 COM6	SEG19 COM6	SEG18 COM6	—	—
LCDDATA39	SEG31 COM6	SEG30 COM6	SEG29 COM6	SEG28 COM6	SEG27 COM6	SEG26 COM6	SEG25 COM6	SEG24 COM6
LCDDATA40	—	—	—	—	—	SEG34 COM6	SEG33 COM6	SEG32 COM6
LCDDATA41	SEG47 COM6	SEG46 COM6	SEG45 COM6	SEG44 COM6	SEG43 COM6	SEG42 COM6	SEG41 COM6	SEG40 COM6
LCDDATA42	SEG7 COM7	SEG6 COM7	—	SEG4 COM7	SEG3 COM7	SEG2 COM7	SEG1 COM7	SEG0 COM7
LCDDATA43	SEG15 COM7	SEG14 COM7	SEG13 COM7	—	SEG11 COM7	SEG10 COM7	SEG9 COM7	SEG8 COM7
LCDDATA44	SEG23 COM7	SEG22 COM7	—	SEG20 COM7	SEG19 COM7	SEG18 COM7	—	—
LCDDATA45	SEG31 COM7	SEG30 COM7	SEG29 COM7	SEG28 COM7	SEG27 COM7	SEG26 COM7	SEG25 COM7	SEG24 COM7
LCDDATA46	—	—	—	—	—	SEG34 COM7	SEG33 COM7	SEG32 COM7
LCDDATA47	SEG47 COM7	SEG46 COM7	SEG45 COM7	SEG44 COM7	SEG43 COM7	SEG42 COM7	SEG41 COM7	SEG40 COM7

REGISTER 35-6: LCDVCON2: LCD VOLTAGE CONTROL 2 BITS

R-0	R-0	R-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	LCDVSRC<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Reserved**: Read as '0'

bit 2-0 **LCDVSRC<3:0>:** LCD Voltage Source Control bits

1111-1001 = Reserved
1000 = LCD voltage supplied from External Resistor Ladder(1)(4)
0111 = LCD voltage supplied from Charge Pump + Internal Resistor Ladder(2)(3)
0110 = LCD voltage supplied from Charge Pump Only (no Resistor ladder)(2)(3)
0101 = LCDvoltage supplied from Internal Resistor Ladder + External Capacitors + V_{DD} for VLCD3(1)(4)
0100 = LCDvoltage supplied from Internal Resistor Ladder + External Capacitors + External VLCD3(1)(4)
0011 = LCD voltage supplied from Internal Resistor Ladder + FVR for VLCD3(4)
0010 = LCD voltage supplied from Internal Resistor Ladder + V_{DD} for VLCD3(4)
0001 = LCD voltage supplied from Internal Resistor Ladder + External VLCD3(4)
0000 = All voltage sources are disabled

Note 1: VLCD1/2/3 used for 1/3 BIAS, VLCD3/2 for 1/2 BIAS, VLCD3 for Static BIAS.

2: VLCD1 is only used when (EN5V = 1 and LPEN = 0).

3: Only valid when LCDPEN = 1. If selected when LCDPEN = 0, module will behave as if all sources are disabled.

4: Only valid when LCDPEN = 0. If selected when LCDPEN = 1, module will behave as if all sources are disabled.

REGISTER 35-8: LCDREF: LCD REFERENCE VOLTAGE/CONTRAST CONTROL REGISTER

R-0	R-0	R-0	R-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	LCDCST2	LCDCST1	LCDCST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'.

bit 2-0 **LCDCST<2:0>**: LCD Contrast Control bits(1)

Selects the resistance of the LCD contrast control resistor ladder

Bit Value	Resistor ladder
000 =	Contrast Control Bypassed (Maximum contrast).
001 =	Contrast Control Resistor ladder is at 1/7th of maximum resistance
010 =	Contrast Control Resistor ladder is at 2/7th of maximum resistance
011 =	Contrast Control Resistor ladder is at 3/7th of maximum resistance
100 =	Contrast Control Resistor ladder is at 4/7th of maximum resistance
101 =	Contrast Control Resistor ladder is at 5/7th of maximum resistance
110 =	Contrast Control Resistor ladder is at 6/7th of maximum resistance
111 =	Contrast Control Resistor ladder is at maximum resistance (Minimum contrast)

Note 1: This setting is only valid in Internal Resistance Ladder Only modes.

TABLE 39-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param. No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	60	°C/W	28-pin SPDIP package
			80	°C/W	28-pin SOIC package
			90	°C/W	28-pin SSOP package
			48	°C/W	28-pin UQFN 4x4 mm package
			47.2	°C/W	40-pin PDIP package
			41.0	°C/W	40-pin UQFN 5x5 package
			46.0	°C/W	44-pin TQFP package
			24.4	°C/W	44-pin QFN 8x8 mm package
			27.6	°C/W	48-pin UQFN 6x6 package
			—	°C/W	48-pin TQFP 7x7 package
TH02	θJC	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package
			24	°C/W	28-pin SOIC package
			24	°C/W	28-pin SSOP package
			12	°C/W	28-pin UQFN 4x4 mm package
			24.70	°C/W	40-pin PDIP package
			5.5	°C/W	40-pin UQFN 5x5 package
			14.5	°C/W	44-pin TQFP package
			20.0	°C/W	44-pin QFN 8x8 mm package
			6.7	°C/W	48-pin UQFN 6x6 package
			—	°C/W	48-pin TQFP 7x7 package
TH03	TJMAX	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD(1)
TH06	PI/O	I/O Power Dissipation	—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power	—	W	PDER = PDMAX (TJ - TA)/θJA(2)

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature, TJ = Junction Temperature

FIGURE 39-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

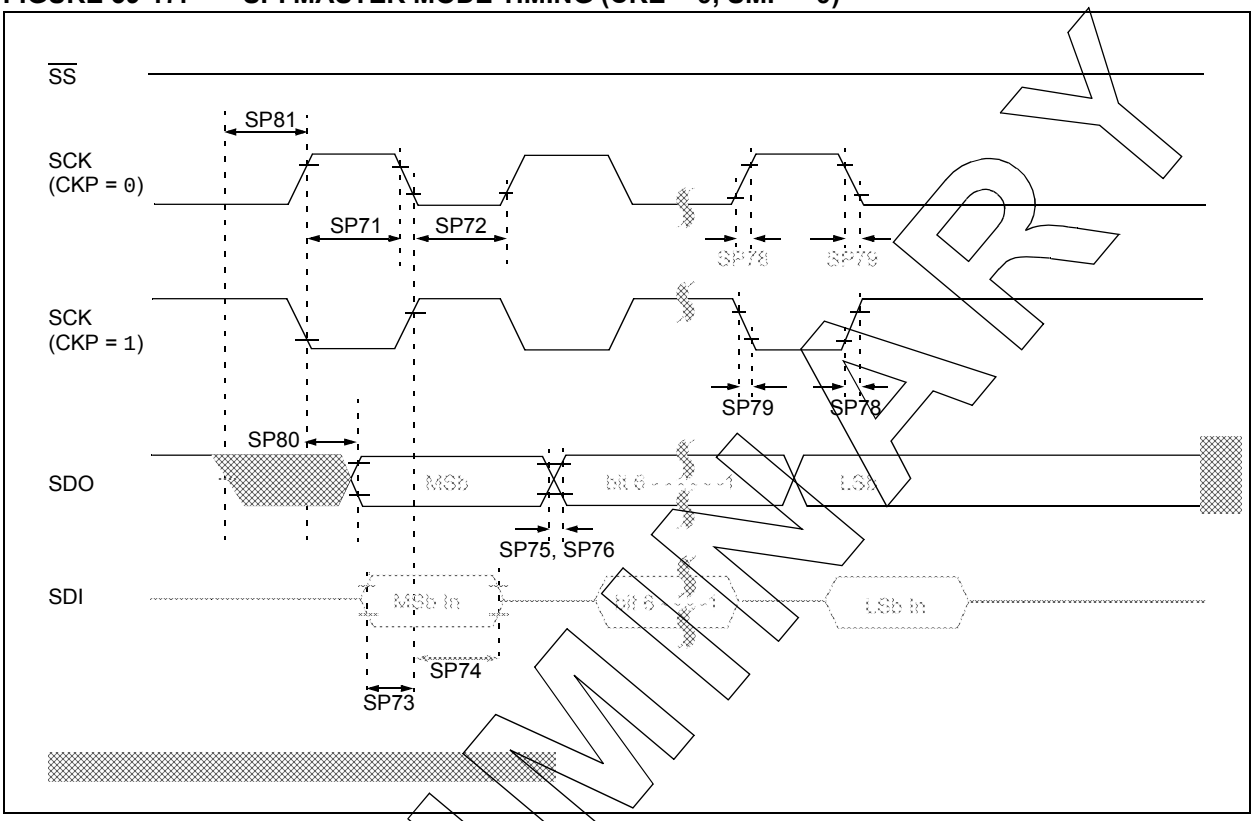
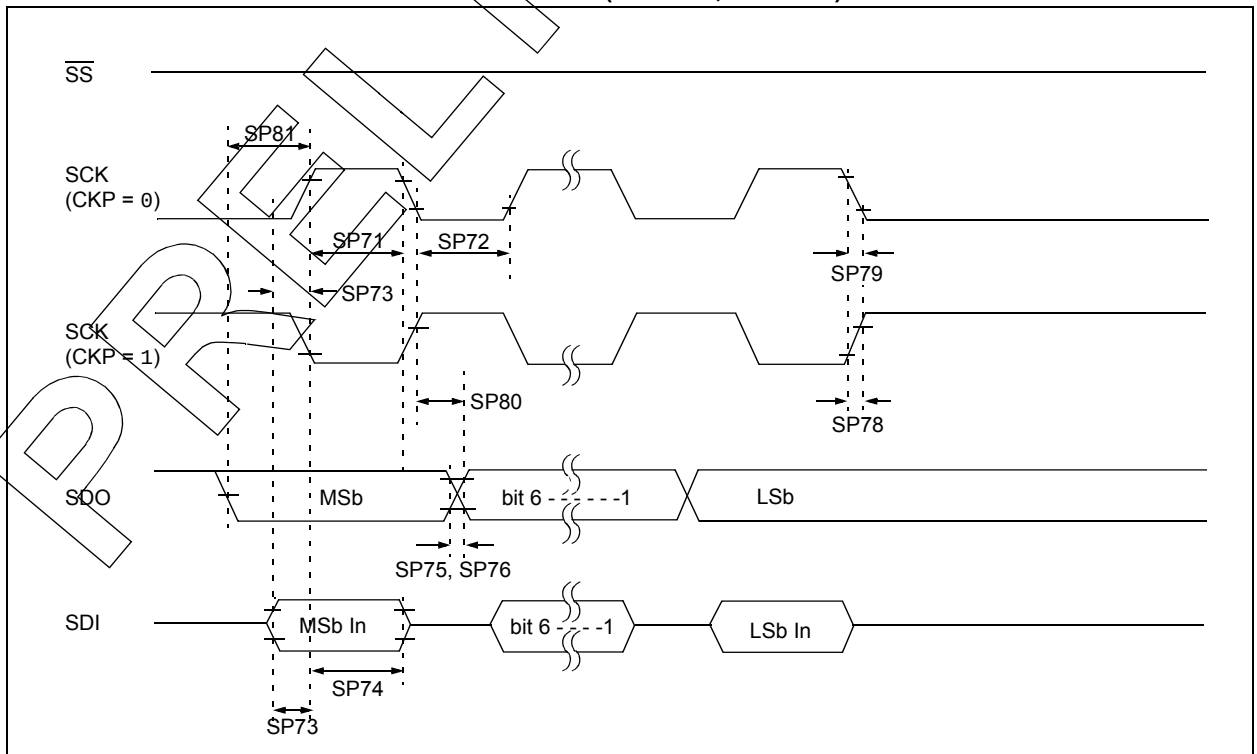


FIGURE 39-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 39-4 for load conditions.