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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19185t-i-pt

TABLE 1-3: PIC16(L)F19175/76 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/C1IN0-/C2IN0-/ANA0/CLCIN0(1)/IOCA0/SEG0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	ANA0	AN	—	ADC Channel input.
	CLCIN0(1)	—	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
	SEG0	—	AN	LCD Analog output.
RA1/C1IN1-/C2IN1-/ANA1/CLCIN1(1)/SEG1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
	ANA1	AN	—	ADC Channel input.
	CLCIN1(1)	—	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
	SEG1	—	AN	LCD Analog output.
RA2/C1IN0+/C2IN0+/ANA2/DAC1OUT1/IOCA2/SEG2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0+	AN	—	Comparator positive input.
	C2IN0+	AN	—	Comparator positive input.
	ANA2	AN	—	ADC Channel input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
	SEG2	—	AN	LCD Analog output.
RA3/C1IN1+/ANA3/SEG3/IOCA3/VREF+ (ADC)/VREF+ (DAC1)	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN1+	AN	—	Comparator positive input.
	ANA3	AN	—	ADC Channel input.
	SEG3	—	AN	LCD Analog output.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
	VREF+ (ADC)	AN	—	ADC positive reference.
	VREF+ (DAC1)	AN	—	DAC positive reference.
RA4/ANA4/T0CKI(1)/IOCA4/SEG4/COM3	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel input.
	T0CKI(1)	—	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
	SEG4	—	AN	LCD Analog output.
	COM3	—	AN	LCD Driver Common Outputs.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input' ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-3: PIC16(L)F19175/76 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC7/DT1(3)/RX1(1)/IOCC7/ANC7/SEG23/VLCD1	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	DT1(3)	—	—	EUSART synchronous data output
	RX1(1)	—	—	EUSART receive input.
	IOCC7	TTL/ST	—	Interrupt-on-change input.
	ANC7	AN	—	ADC Channel input.
	SEG23	—	AN	LCD Analog output.
	VLCD1	AN	—	LCD analog input
RD0/AND0/SEG24	RD0	TTL/ST	CMOS/OD	General purpose I/O.
	AND0	AN	—	ADC Channel input.
	SEG24	AN	—	LCD Analog output.
RD1/AND1/SEG25	RD1	TTL/ST	CMOS/OD	General purpose I/O.
	AND1	AN	—	ADC Channel input.
	SEG25	—	AN	LCD Analog output.
RD2/AND2/COM5	RD2	TTL/ST	CMOS/OD	General purpose I/O.
	AND2	AN	—	ADC Channel input.
	SEG26	—	AN	LCD Analog output.
	COM5	—	AN	LCD Driver Common Outputs.
RD3/AND3/SEG27/COM4	RD3	TTL/ST	CMOS/OD	General purpose I/O.
	AND3	AN	—	ADC Channel input.
	SEG27	—	AN	LCD Analog output.
	COM4	—	AN	LCD Driver Common Outputs.
RD4/AND4/SEG28	RD4	TTL/ST	CMOS/OD	General purpose I/O.
	AND4	AN	—	ADC Channel input.
	SEG28	—	AN	LCD Analog output.
RD5/AND5/SEG29	RD5	TTL/ST	CMOS/OD	General purpose I/O.
	AND5	AN	—	ADC Channel input.
	SEG29	AN	—	LCD Analog output.
RD6/AND6/SEG30	RD6	TTL/ST	CMOS/OD	General purpose I/O.
	AND6	AN	—	ADC Channel input.
	SEG30	—	AN	LCD Analog output.
RD7/AND7/SEG31	RD7	TTL/ST	CMOS/OD	General purpose I/O.
	AND7	AN	—	ADC Channel input.
	SEG31	AN	—	LCD Analog output.
RE0/ANE0/SEG32	RE0	TTL/ST	CMOS/OD	General purpose I/O.
	ANE0	AN	—	ADC Channel input.
	SEG32	—	AN	LCD Analog output.
RE1/ANE2/SEG33/COM6	RE1	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel input.
	SEG33	—	AN	LCD analog input
	COM6	—	AN	LCD Driver Common Outputs.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

4.3.2.1 STATUS Register

The STATUS register, shown in Register 4-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (refer to **Section 37.0 "Instruction Set Summary"**).

Note 1: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 4-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
- 1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
- 0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
- 1 = After power-up or by the `CLRWDT` instruction
- 0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
- 1 = The result of an arithmetic or logic operation is zero
- 0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
- 1 = A carry-out from the 4th low-order bit of the result occurred
- 0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
- 1 = A carry-out from the Most Significant bit of the result occurred
- 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 9											
CPU CORE REGISTERS; see Table 4-3 for specifics											
48Ch	SMT1TMRL	SMT1TMR								0000 0000	0000 0000
48Dh	SMT1TMRH	SMT1TMR								0000 0000	0000 0000
48Eh	SMT1TMRU	SMT1TMR								0000 0000	0000 0000
48Fh	SMT1CPRL	CPR								xxxx xxxx	xxxx xxxx
490h	SMT1CPRH	CPR								xxxx xxxx	xxxx xxxx
491h	SMT1CPRU	CPR								xxxx xxxx	xxxx xxxx
492h	SMT1CPWL	CPW								xxxx xxxx	xxxx xxxx
493h	SMT1CPWH	CPW								xxxx xxxx	xxxx xxxx
494h	SMT1CPWU	CPW								xxxx xxxx	xxxx xxxx
495h	SMT1PRL	SMT1PR								1111 1111	1111 1111
496h	SMT1PRH	SMT1PR								1111 1111	1111 1111
497h	SMT1PRU	SMT1PR								1111 1111	1111 1111
498h	SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		0-00 0000	0-00 0000
499h	SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				00-- 0000	00-- 0000
49Ah	SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	000- -000	000- -000
49Bh	SMT1CLK	—	—	—	—	—	CSEL<2:0>			0000 0000	0000 0000
49Ch	SMT1SIG	—	—	—	SSEL<4:0>					0000 0000	0000 0000
49Dh	SMT1WIN	—	—	—	WSEL<4:0>					0000 0000	0000 0000
49Eh	—	Unimplemented								---- ----	---- ----
49Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

10.6 Register Definitions: Interrupt Control

REGISTER 10-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R/W-1/1
GIE	PEIE	—	—	—	—	—	INTEDG
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

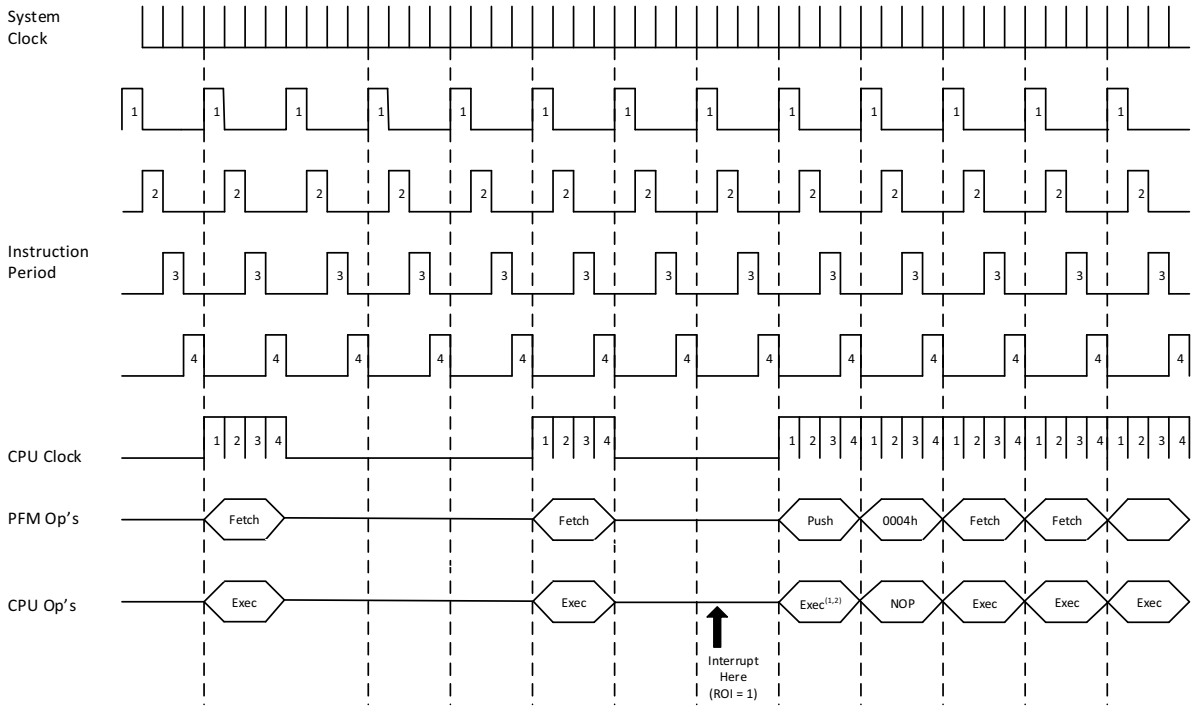
bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 11-1: DOZE MODE OPERATION EXAMPLE



Note 1: Multi-cycle instructions are executed to completion before fetching 0004h.
2: If the pre-fetched instruction clears GIE, the ISR will not occur, but DOZEN is still cleared and the CPU will resume execution at full speed.

11.2 Sleep Mode

Sleep mode is entered by executing the SLEEP instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0). If the SLEEP instruction is executed while the IDLEN bit is set (IDLEN = 1), the CPU will enter the IDLE mode (**Section 11.2.3 "Low-Power Sleep Mode"**).

Upon entering Sleep mode, the following conditions exist:

1. WWDT will be cleared but keeps running if enabled for operation during Sleep
2. The $\overline{PD}$ bit of the STATUS register is cleared
3. The $\overline{TO}$ bit of the STATUS register is set
4. CPU Clock and System Clock
5. 31 kHz LFINTOSC, HFINTOSC and SOSC are unaffected and peripherals using them may continue operation in Sleep.
6. ADC is unaffected if the dedicated FRC oscillator is selected the conversion will be left abandoned if FOSC is selected and ADRES will have an incorrect value
7. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance). This does not apply in the case of any asynchronous peripheral which is active and may affect the I/O port value
8. Resets other than WWDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH WINDOWED WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON1	—	NOSC<2:0>			NDIV<3:0>				152
OSCCON2	—	COSC<2:0>			CDIV<3:0>				152
OSCCON3	CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	154
PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	140
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	50
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	196
WDTCON1	—	WDTCS<2:0>			—	WINDOW<2:0>			197
WDTPSL	PSCNT<7:0>								198
WDTPSH	PSCNT<15:8>								198
WDTTMR	—	WDTTMR<3:0>				STATE	PSCNT<17:16>		198

Legend: – = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 12-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	—	CSWEN	LCDPEN	$\overline{\text{VBATEN}}$	$\overline{\text{CLKOUTEN}}$	120
	7:0	—	RSTOSC<2:0>			—	FEXTOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

13.4.9 WRERR BIT

The WRERR bit can be used to determine if a write error occurred.

WRERR will be set if one of the following conditions occurs:

- If WR is set while the NVMADRH:NMVADRL points to a write-protected address
- A Reset occurs while a self-write operation was in progress
- An unlock sequence was interrupted

The WRERR bit is normally set by hardware, but can be set by the user for test purposes. Once set, WRERR must be cleared in software.

TABLE 13-4: ACTIONS FOR PFM WHEN WR = 1

Free	LWLO	Actions for PFM when WR = 1	Comments
1	x	Erase the 32-word row of NVMADRH:NVMADRL location. See **Section 13.4.4 "NVMREG Erase of PFM"**	• If WP is enabled, WR is cleared and WRERR is set • All 32 words are erased • NVMDATH:NVMDATL is ignored
0	1	Copy NVMDATH:NVMDATL to the write latch corresponding to NVMADR LSBs. See **Section 13.4.4 "NVMREG Erase of PFM"**	• Write protection is ignored • No memory access occurs
0	0	Write the write-latch data to PFM row. See **Section 13.4.4 "NVMREG Erase of PFM"**	• If WP is enabled, WR is cleared and WRERR is set • Write latches are reset to 3FFh • NVMDATH:NVMDATL is ignored

TABLE 15-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
Inputs									
PPSLOCK	—	—	—	—	—	—	—	PPSLOCKED	265
INTPPS	—	—	—	INTPPS<4:0>					264
T0CKIPPS	—	—	—	T0CKIPPS<4:0>					264
T1CKIPPS	—	—	—	T1CKIPPS<4:0>					264
T1GPPS	—	—	—	T1GPPS<4:0>					264
T2INPPS	—	—	—	T2INPPS<4:0>					264
T4INPPS	—	—	—	T4INPPS<4:0>					264
CCP1PPS	—	—	—	CCP1PPS<4:0>					264
CCP2PPS	—	—	—	CCP2PPS<4:0>					264
SMT1WINPPS	—	—	—	SMT1WINPPS<4:0>					264
SMT1SIGPPS	—	—	—	SMT1SIGPPS<4:0>					264
CWG1PPS	—	—	—	CWG1PPS<4:0>					264
CLCIN0PPS	—	—	—	CLCIN0PPS<4:0>					264
CLCIN1PPS	—	—	—	CLCIN1PPS<4:0>					264
CLCIN2PPS	—	—	—	CLCIN2PPS<4:0>					264
CLCIN3PPS	—	—	—	CLCIN3PPS<4:0>					264
ADCACTPPS	—	—	—	ADCACTPPS<4:0>					264
SSP1CLKPPS	—	—	—	SSP1CLKPPS<4:0>					264
SSP1DATPPS	—	—	—	SSP1DATPPS<4:0>					264
SSP1SSPPS	—	—	—	SSP1SSPPS<4:0>					264
RX1PPS	—	—	—	RX1PPS<4:0>					264
TX1PPS	—	—	—	TX1PPS<4:0>					264
RX2PPS	—	—	—	RX2PPS<4:0>					264
TX2PPS	—	—	—	TX2PPS<4:0>					264
Outputs									
RA0PPS	—	—	—	RA0PPS<4:0>					265
RA1PPS	—	—	—	RA1PPS<4:0>					265
RA2PPS	—	—	—	RA2PPS<4:0>					265
RA3PPS	—	—	—	RA3PPS<4:0>					265
RA4PPS	—	—	—	RA4PPS<4:0>					265
RA5PPS	—	—	—	RA5PPS<4:0>					265
RA6PPS	—	—	—	RA6PPS<4:0>					265
RA7PPS	—	—	—	RA7PPS<4:0>					265
RB0PPS	—	—	—	RB0PPS<4:0>					265
RB1PPS	—	—	—	RB1PPS<4:0>					265
RB2PPS	—	—	—	RB2PPS<4:0>					265
RB3PPS	—	—	—	RB3PPS<4:0>					265
RB4PPS	—	—	—	RB4PPS<4:0>					265
RB5PPS	—	—	—	RB5PPS<4:0>					265
RB6PPS	—	—	—	RB6PPS<4:0>					265
RB7PPS	—	—	—	RB7PPS<4:0>					265
RC0PPS	—	—	—	RC0PPS<4:0>					265
RC1PPS	—	—	—	RC1PPS<4:0>					265
RC2PPS	—	—	—	RC2PPS<4:0>					265
RC3PPS	—	—	—	RC3PPS<4:0>					265
RC4PPS	—	—	—	RC4PPS<4:0>					265
RC6PPS	—	—	—	RC6PPS<4:0>					265
RC7PPS	—	—	—	RC7PPS<4:0>					265
RD0PPS	—	—	—	RD0PPS<4:0>					265

16.0 PERIPHERAL MODULE DISABLE (PMD)

The PIC16(L)F19155/56/75/76/85/86 provides the ability to disable selected modules, placing them into the lowest possible Power mode.

For legacy reasons, all modules are ON by default following any Reset.

16.1 Disabling a Module

Disabling a module has the following effects:

- All clock and control inputs to the module are suspended; there are no logic transitions, and the module will not function.
- The module is held in Reset:
  - Writing to SFRs is disabled
  - Reads return 00h

16.2 Enabling a module

When the register bit is cleared, the module is re-enabled and will be in its Reset state; SFR data will reflect the POR Reset values.

Depending on the module, it may take up to one full instruction cycle for the module to become active. There should be no interaction with the module (e.g., writing to registers) for at least one instruction after it has been re-enabled.

16.3 Disabling a Module

When a module is disabled, all the associated PPS selection registers (Registers xxxPPS Register 15-1, 15-2, and 15-3), are also disabled.

16.4 System Clock Disable

Setting SYSCMD (PMD0, Register 16-1) disables the system clock (FOSC) distribution network to the peripherals. Not all peripherals make use of SYSCLK, so not all peripherals are affected. Refer to the specific peripheral description to see if it will be affected by this bit.

REGISTER 16-3: PMD2: PMD CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
RTCCMD	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **RTCCMD:** Disable RTCC bit
1 = RTCC module disabled
0 = RTCC module enabled

bit 6 **DACMD:** Disable DAC bit
1 = DAC module disabled
0 = DAC module enabled

bit 5 **ADCMD:** Disable ADC bit
1 = ADC module disabled
0 = ADC module enabled

bit 4-3 **Unimplemented:** Read as ‘0’

bit 2 **CMP2MD:** Disable Comparator C2 bit
1 = C2 module disabled
0 = C2 module enabled

bit 1 **CMP1MD:** Disable Comparator C1 bit
1 = C1 module disabled
0 = C1 module enabled

bit 0 **ZCDMD:** Disable ZCD
1 = ZCD module disabled
0 = ZCD module enabled

REGISTER 19-8: ADPCH: ADC POSITIVE CHANNEL SELECTION REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ADPCH<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **ADPCH<5:0>**: ADC Positive Input Channel Selection bits

ADPCH <5:0>	Device Pin Count			ADC Input Connection
	28	40	48	
0x00	•	•	•	RA0
0x01	•	•	•	RA1
0x02	•	•	•	RA2
0x03	•	•	•	RA3
0x04	•	•	•	RA4
0x05	—	—	—	RA5
0x06	•	•	•	RA6
0x07	•	•	•	RA7
0x08	•	•	•	RB0
0x09	•	•	•	RB1
0x0A	•	•	•	RB2
0x0B	•	•	•	RB3
0x0C	•	•	•	RB4
0x0D	•	•	•	RB5
0x0E	•	•	•	RB6
0x0F	•	•	•	RB7
0x10	—	—	—	RC0
0x11	—	—	—	RC1
0x12	•	•	•	RC2
0x13	•	•	•	RC3
0x14	•	•	•	RC4
0x15	—	—	—	RC5
0x16	•	•	•	RC6
0x17	•	•	•	RC7
0x18	—	•	•	RD0
0x19	—	•	•	RD1
0x1A	—	•	•	RD2
0x1B	—	•	•	RD3
0x1C	—	•	•	RD4
0x1D	—	•	•	RD5
0x1E	—	•	•	RD6
0x1F	—	•	•	RD7

ADPCH <5:0>	Device Pin Count			ADC Input Connection
	28	40	48	
0x20	—	•	•	RE0
0x21	—	•	•	RE1
0x22	—	•	•	RE2
0x23	—	—	—	RE3
0x24	—	—	—	RE4
0x25	—	—	—	RE5
0x26	—	—	—	RE6
0x27	—	—	—	RE7
0x28	—	—	•	RF0
0x29	—	—	•	RF1
0x2A	—	—	•	RF2
0x2B	—	—	•	RF3
0x2C	—	—	•	RF4
0x2D	—	—	•	RF5
0x2E	—	—	•	RF6
0x2F	—	—	•	RF7
0x30	—	—	—	RG0
0x31	—	—	—	RG1
0x32	—	—	—	RG2
0x33	—	—	—	RG3
0x34	—	—	—	RG4
0x35	—	—	—	RG5
0x36	—	—	—	RG6
0x37	—	—	—	RG7
0x38	—	—	—	—
0x39	VLCD3 divided by 4(4)			
0x3A	VBAT divided by 3(5)			
0x3B	AVSS (Analog Ground)			
0x3C	Temperature Indicator(3)			
0x3D	DAC1 Output(1)			
0x3E	FVR Buffer 1(2)			
0x3F	FVR Buffer 2(2)			

Note 1: See **Section 19.0 "Analog-to-Digital Converter with Computation (ADC2) Module"** for more information.
2: See **Section 18.0 "Fixed Voltage Reference (FVR)"** for more information.
3: See **Section 20.0 "Temperature Indicator Module (TIM)"** for more information.
4: See **Section 35.0 "Liquid Crystal Display (LCD) Controller"** for more information.
5: See **Section 8.0 "Resets and Vbat"** for more information.

20.0 TEMPERATURE INDICATOR MODULE (TIM)

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The main purpose of the temperature indicator module is to provide temperature-dependent voltage that can be measured by the Analog-to-Digital Converter.

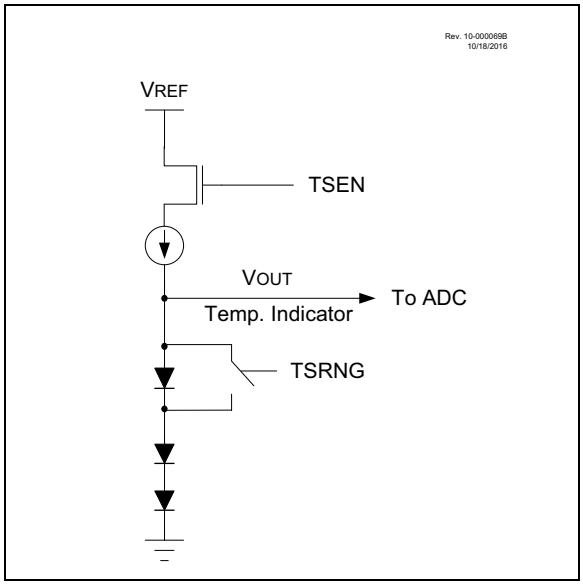
The circuit's range of operating temperature falls between -40°C and +125°C. The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately.

20.1 Module Operation

The temperature indicator module consists of a temperature-sensing circuit that provides a voltage to the device ADC. The analog voltage output, VTSENSE, varies inversely to the device temperature. The output of the temperature indicator is referred to as VOUT.

Figure 20-1 shows a simplified block diagram of the temperature indicator module.

FIGURE 20-1: TEMPERATURE CIRCUIT DIAGRAM



The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 19.0 "Analog-to-Digital Converter with Computation (ADC2) Module"** for detailed information.

The ON/OFF bit for the module is located in the FVRCON register. See **Section 18.0 "Fixed Voltage Reference (FVR)"** for more information. The circuit is enabled by setting the TSEN bit of the FVRCON register. When the module is disabled, the circuit draws no current.

The circuit operates in either High or Low range. Refer to **Section 20.5 "Temperature Indicator Range"** for more details on the range settings.

20.2 Estimation of Temperature

This section describes how the sensor voltage can be used to estimate the temperature of the module. To use the sensor, the output voltage, VTSENSE, is measured and the corresponding temperature is determined. Equation 20-1 provides an estimate for the die temperature based on the VTSENSE value.

EQUATION 20-1: SENSOR TEMPERATURE

$$T_{SENSE} = V_{TSENSE} \times (-Mt) + T_{OFFSET}$$

Where:
Mt = 1/Mv, where Mv = sensor voltage sensitivity (V/°C).
TOFFSET is the temperature difference between the theoretical temperature and the actual temperature.

21.6 Register Definitions: DAC Control

REGISTER 21-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **DAC1EN:** DAC1 Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **DAC1OE1:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT1 pin
0 = DAC voltage level is disconnected from the DAC1OUT1 pin

bit 4 **DAC1OE2:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT2 pin
0 = DAC voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 **DAC1PSS<1:0>:** DAC1 Positive Source Select bits
11 = Reserved, do not use
10 = FVR output
01 = V_{REF+} pin
00 = V_{DD}

bit 1-0 **Unimplemented:** Read as ‘0’

REGISTER 21-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	DAC1R<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DAC1R<4:0>:** DAC1 Voltage Output Select bits
$V_{OUT} = (V_{SRC+} - V_{SRC-})*(DAC1R<4:0>/32) + V_{SRC}$

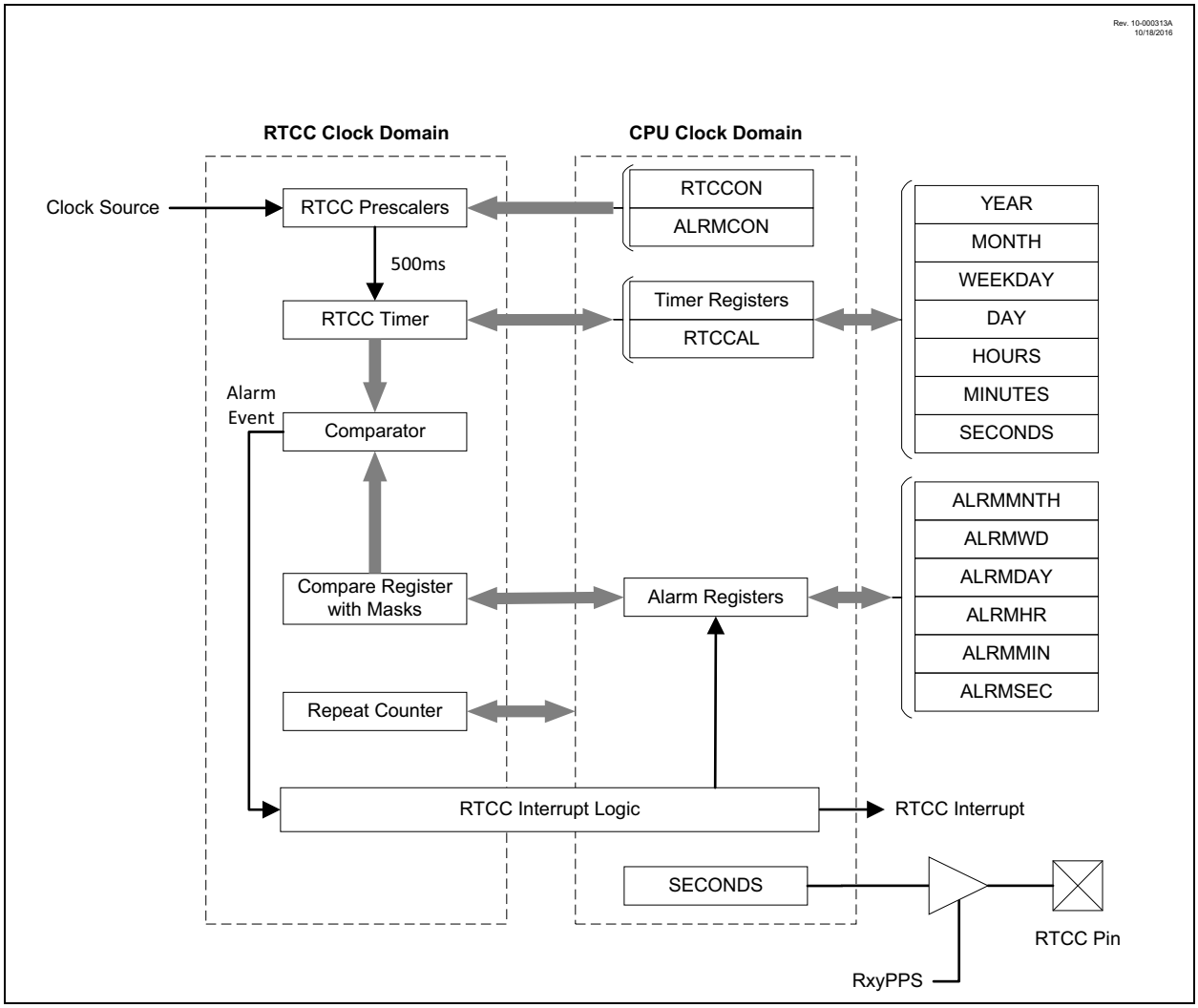
24.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

The PIC16(L)F19155/56/75/76/85/86 family of devices is equipped with a Real-Time Clock and Calendar (RTCC) module, designed to maintain accurate time measurement for extended periods, with little or no intervention from the CPU. The module is optimized for low-power operation in order to provide extended battery life. The key features include:

- Time: Hours, Minutes and Seconds
- 24-hour Format (Military Time)
- Calendar: Weekday, Date, Month and Year
- Year Range: 2000 to 2099
- Leap Year Correction
- Configurable Alarm
- BCD Format for Compact Firmware
- Half-second Synchronization and Visibility
- User Calibration with Auto-Adjust
- Multiple Clock Sources
- Low-Power Optimization

Figure 24-1 is a simplified block diagram of the RTCC module.

FIGURE 24-1: RTCC BLOCK DIAGRAM



27.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

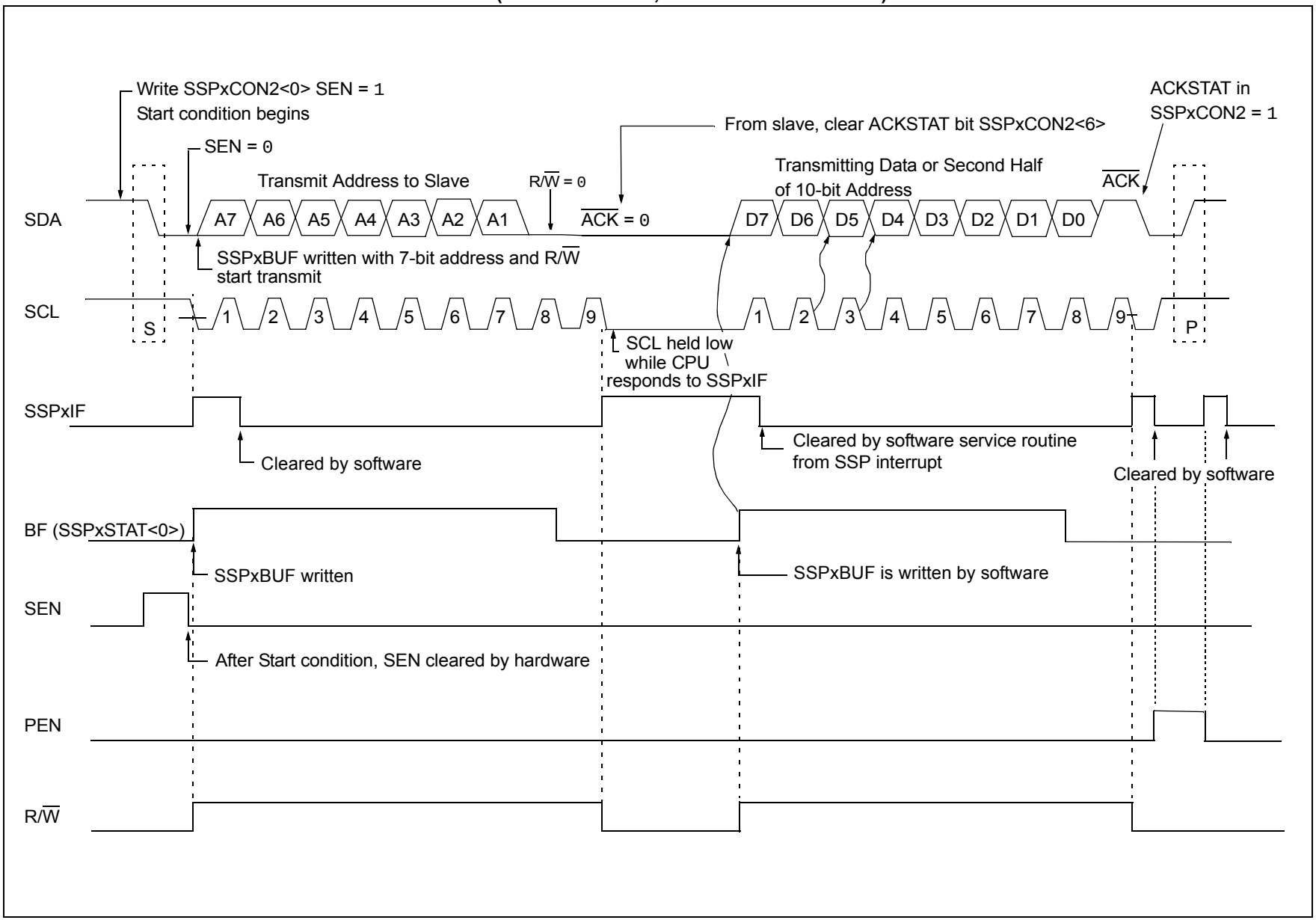
In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = `01110`)
- High Reset level (MODE<4:0> = `01111`)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

FIGURE 33-28: I^2C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



34.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 9.2.2.2 "Internal Oscillator Frequency Adjustment"** for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 34.3.1 "Auto-Baud Detect"**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

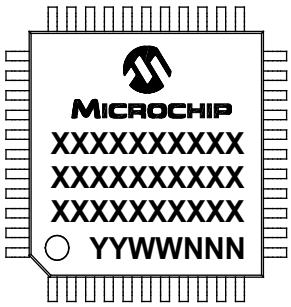
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
994h	CM2CON0	ON	OUT	—	POL	—	—	HYS	SYNC	340
995h	CM2CON1	—	—	—	—	—	—	INTP	INTN	341
996h	CM2NSEL	—	—	—	—	—	NCH<2:0>			342
996h		—	—	—	—	—	NCH2	NCH1	NCH0	342
997h	CM2PSEL	—	—	—	—	—	PCH<2:0>			342
997h		—	—	—	—	—	PCH2	PCH1	PCH0	342
998h	—	Unimplemented								
999h	—	Unimplemented								
99Ah	—	Unimplemented								
99Bh	—	Unimplemented								
99Ch	—	Unimplemented								
99Dh	—	Unimplemented								
99Eh	—	Unimplemented								
99Fh	—	Unimplemented								
A0Ch	—	Unimplemented								
A0Dh	—	Unimplemented								
A0Eh	—	Unimplemented								
A0Fh	—	Unimplemented								
A10h	—	Unimplemented								
A11h	—	Unimplemented								
A12h	—	Unimplemented								
A13h	—	Unimplemented								
A14h	—	Unimplemented								
A15h	—	Unimplemented								
A16h	—	Unimplemented								
A17h	—	Unimplemented								
A18h	—	Unimplemented								
A19h	RC2REG	RC2REG								
A1Ah	TX2REG	TX2REG								
A1Bh	SP2BRGL	SP2BRGL								
A1Ch	SP2BRGH	SP2BRGH								
A1Dh	RC2STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	
A1Eh	TX2STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	
A1Fh	BAUD2CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	
A8Ch — A9Fh	—	Unimplemented								
B0Ch — B1Fh	—	Unimplemented								
B8Ch — B9Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

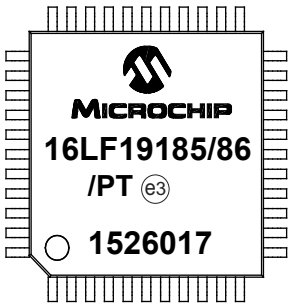
Note 1: Unimplemented data memory locations, read as '0'.

42.1 Package Marking Information (Continued)

48-Lead TQFP (7x7x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.