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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19186t-i-pt

TABLE 1-2: PIC16(L)F19155/56 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/SS(1)/IOCA5/VBAT	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	SS(1)	—	—	MSSP SPI slave select input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.
	VBAT	AN	—	RTCC Back-up Battery.
RA6/ANA6/IOCA6/SEG6/CLKOUT	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN	—	ADC Channel input.
	IOCA6	—	—	Interrupt-on-change input.
	SEG6	—	AN	LCD Analog output.
	CLKOUT	TTL/ST	—	FOSC/4 digital output.
RA7/ANA7/SEG7/CLKIN	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN	—	ADC Channel input.
	SEG7	—	AN	LCD Analog output.
	CLKIN	ST	—	External Clock driver input.
RB0/CWG1IN(1)/C2IN1+/IOCB0/ANB0/SEG8/ZCD	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	CWG1IN(1)	TTL/ST	—	Complementary Waveform Generator input
	C2IN1+	AN	—	Comparator positive input.
	IOCB0	TTL/ST	—	Interrupt-on-change input.
	ANB0	AN	—	ADC Channel input.
	SEG8	-	AN	LCD Analog output.
	ZCD	AN	—	Zero-cross detect input pin (with constant current sink/source).
RB1/C1IN3-/C2IN3-/IOCB1/SCL(3,4)/SCK(1)/ANB1/HIB1/SEG9	RB1	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN3-	AN	—	Comparator negative input.
	C2IN3-	AN	—	Comparator negative input.
	IOCB1	TTL/ST	—	Interrupt-on-change input.
	SCL(3,4)	I2C	OD	MSSP I2Cclock input/output.
	SCK(1)	TTL/ST	—	MSSP SPI clock input/output.
	ANB1	AN	—	ADC Channel input.
	HIB1	TTL/ST	—	High current output.
	SEG9	—	AN	LCD Analog output.
RB2/IOCB2/SDA(3,4)/SDI(1)/ANB2/SEG10/COM7/SEGCFLY1	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB2	TTL/ST	—	Interrupt-on-change input.
	SDA(3,4)	I2C	OD	MSSP I2C data input/output.
	SDI(1)	TTL/ST	—	MSSP SPI serial data in.
	ANB2	AN	—	ADC Channel input.
	SEG10	—	AN	LCD Analog output.
	COM7	—	AN	LCD Driver Common Outputs.
	SEGCFLY1	AN	—	LCD Drive Charge Pump Capacitor Inputs

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I2C = Schmitt Trigger input with I2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I2C specific or SMBus input buffer thresholds.

TABLE 1-4: PIC16(L)F19185/86 PINOUT DESCRIPTION

Name	Function	Input Types	Output Types	Description
RA0/C1IN0-/C2IN0-/ANA0/CLCIN0(1)/IOCA0/SEG0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	ANA0	AN	—	ADC Channel input.
	CLCIN0(1)	—	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
	SEG0	-	AN	LCD Analog output.
RA1/C1IN1-/C2IN1-/ANA1/CLCIN1(1)/SEG1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
	ANA1	AN	—	ADC Channel input.
	CLCIN1(1)	—	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
	SEG1	—	AN	LCD Analog output.
RA2/C1IN0+/C2IN0+/ANA2/DAC1OUT1/IOCA2/SEG2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0+	AN	—	Comparator positive input.
	C2IN0+	AN	—	Comparator positive input.
	ANA2	AN	—	ADC Channel input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
	SEG2	—	AN	LCD Analog output.
RA3/C1IN1+/ANA3/SEG3/IOCA3/VREF+ (ADC)/VREF+ (DAC1)	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN1+	AN	—	Comparator positive input.
	ANA3	AN	—	ADC Channel input.
	SEG3	—	AN	LCD Analog output.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
	VREF+ (ADC)	AN	—	ADC positive reference.
	VREF+ (DAC1)	AN	—	DAC positive reference.
RA4/ANA4/T0CKI(1)/IOCA4/SEG4/COM3	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel input.
	T0CKI(1)	—	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
	SEG4	—	AN	LCD Analog output.
	COM3	—	AN	LCD Driver Common Outputs.
RA5/SS(1)/IOCA5/VBAT	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	SS(1)	TTL/ST	—	MSSP SPI slave select input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.
	VBAT	AN	—	RTCC Back-up Battery.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-4: PIC16(L)F19185/86 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Types	Output Types	Description
RB3/C1IN2-/C2IN2-/IOCB3/ANB3/SEG11/SEGCFLY2	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
	ANB3	AN	—	ADC Channel input.
	SEG11	—	AN	LCD Analog output.
	SEGCFLY2	AN	—	LCD Drive Charge Pump Capacitor Inputs
RB4/ADCACT(1)/IOCB4/ANB4/COM0	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ADCACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input
	IOCB4	TTL/ST	—	Interrupt-on-change input.
	ANB4	AN	—	ADC Channel input.
	COM0	—	AN	LCD Driver Common Outputs.
RB5/T1G(1)/IOCB5/ANB5/SEG13/COM1	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	T1G(1)	—	—	Timer1 Gate input.
	IOCB5	TTL/ST	—	Interrupt-on-change input.
	ANB5	AN	—	ADC Channel input.
	SEG13	—	AN	LCD Analog output.
	COM1	—	AN	LCD Driver Common Outputs.
RB6/CK2(3)/TX2(1)/CLCIN2(1)/IOCB6/ANB6/SEG14/ ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	CK2(3)	—	—	EUSART synchronous clock out
	TX2(1)	—	—	EUSART asynchronous TX data out
	CLCIN2(1)	—	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	ANB6	AN	—	ADC Channel input.
	SEG14	—	AN	LCD Analog output.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
RB7/DK2(3)/RX2(1)/CLCIN3(1)/IOCB7/ANB7/SEG15/ DAC1OUT2/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	DK2(3)	—	—	EUSART synchronous data output
	RX2(1)	—	—	EUSART receive input.
	CLCIN3(1)	—	—	Configurable Logic Cell source input.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	ANB7	—	AN	ADC Channel input.
	SEG15	—	AN	LCD Analog output.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	TTL/ST	TTL/ST	In-Circuit Serial Programming™ and debugging data input/output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 60 (Continued)											
1E37h	CLC4GLS3	LC4G4D4T	LC4G4D4N	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	xxxx xxxx	uuuu uuuu
1E38h	RF0PPS	—	—	—	RF0PPS4	RF0PPS3	RF0PPS2	RF0PPS1	RF0PPS0	---x xxxx	--uu uuuu
1E39h	RF1PPS	—	—	—	RF1PPS4	RF1PPS3	RF1PPS2	RF1PPS1	RF1PPS0	--xx xxxx	--uu uuuu
1E3Ah	RF2PPS	—	—	—	RF2PPS4	RF2PPS3	RF2PPS2	RF2PPS1	RF2PPS0	--xx xxxx	--uu uuuu
1E3Bh	RF3PPS	—	—	—	RF3PPS4	RF3PPS3	RF3PPS2	RF3PPS1	RF3PPS0	--xx xxxx	--uu uuuu
1E3Ch	RF4PPS	—	—	—	RF4PPS4	RF4PPS3	RF4PPS2	RF4PPS1	RF4PPS0	--xx xxxx	--uu uuuu
1E3Dh	RF5PPS	—	—	—	RF5PPS4	RF5PPS3	RF5PPS2	RF5PPS1	RF5PPS0	--xx xxxx	--uu uuuu
1E3Eh	RF6PPS	—	—	—	RF6PPS4	RF6PPS3	RF6PPS2	RF6PPS1	RF6PPS0	--xx xxxx	--uu uuuu
1E3Fh	RF7PPS	—	—	—	RF7PPS4	RF7PPS3	RF7PPS2	RF7PPS1	RF7PPS0	--xx xxxx	--uu uuuu
1E40h	—	Unimplemented								---- ----	---- ----
1E41h	—	Unimplemented								---- ----	---- ----
1E42h	—	Unimplemented								---- ----	---- ----
1E43h	—	Unimplemented								---- ----	---- ----
1E44h	—	Unimplemented								---- ----	---- ----
1E45h	—	Unimplemented								---- ----	---- ----
1E46h	—	Unimplemented								---- ----	---- ----
1E47h	—	Unimplemented								---- ----	---- ----
1E48h	—	Unimplemented								---- ----	---- ----
1E49h	—	Unimplemented								---- ----	---- ----
1E4Ah	—	Unimplemented								---- ----	---- ----
1E4Bh	—	Unimplemented								---- ----	---- ----
1E4Ch	—	Unimplemented								---- ----	---- ----
1E4Dh	—	Unimplemented								---- ----	---- ----
1E4Eh	—	Unimplemented								---- ----	---- ----
1E4Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 62											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1F0Ch	—	Unimplemented								---- ----	---- ----
1F0Dh	—	Unimplemented								---- ----	---- ----
1F0Eh	—	Unimplemented								---- ----	---- ----
1F0Fh	—	Unimplemented								---- ----	---- ----
1F10h	RA0PPS	—	—	—	RA0PPS4	RA0PPS3	RA0PPS2	RA0PPS1	RA0PPS0	0000 0000	--uu uuuu
1F11h	RA1PPS	—	—	—	RA1PPS4	RA1PPS3	RA1PPS2	RA1PPS1	RA1PPS0	0000 0000	--uu uuuu
1F12h	RA2PPS	—	—	—	RA2PPS4	RA2PPS3	RA2PPS2	RA2PPS1	RA2PPS0	0000 0000	--uu uuuu
1F13h	RA3PPS	—	—	—	RA3PPS4	RA3PPS3	RA3PPS2	RA3PPS1	RA3PPS0	0000 0000	--uu uuuu
1F14h	RA4PPS	—	—	—	RA4PPS4	RA4PPS3	RA4PPS2	RA4PPS1	RA4PPS0	0000 0000	--uu uuuu
1F15h	RA5PPS	—	—	—	RA5PPS4	RA5PPS3	RA5PPS2	RA5PPS1	RA5PPS0	0000 0000	--uu uuuu
1F16h	RA6PPS	—	—	—	RA6PPS4	RA6PPS3	RA6PPS2	RA6PPS1	RA6PPS0	0000 0000	--uu uuuu
1F17h	RA7PPS	—	—	—	RA7PPS4	RA7PPS3	RA7PPS2	RA7PPS1	RA7PPS0	0000 0000	--uu uuuu
1F18h	RB0PPS	—	—	—	RB0PPS4	RB0PPS3	RB0PPS2	RB0PPS1	RB0PPS0	0000 0000	--uu uuuu
1F19h	RB1PPS	—	—	—	RB1PPS4	RB1PPS3	RB1PPS2	RB1PPS1	RB1PPS0	0000 0000	--uu uuuu
1F1Ah	RB2PPS	—	—	—	RB2PPS4	RB2PPS3	RB2PPS2	RB2PPS1	RB2PPS0	0000 0000	--uu uuuu
1F1Bh	RB3PPS	—	—	—	RB3PPS4	RB3PPS3	RB3PPS2	RB3PPS1	RB3PPS0	0000 0000	--uu uuuu
1F1Ch	RB4PPS	—	—	—	RB4PPS4	RB4PPS3	RB4PPS2	RB4PPS1	RB4PPS0	0000 0000	--uu uuuu
1F1Dh	RB5PPS	—	—	—	RB5PPS4	RB5PPS3	RB5PPS2	RB5PPS1	RB5PPS0	0000 0000	--uu uuuu
1F1Eh	RB6PPS	—	—	—	RB6PPS4	RB6PPS3	RB6PPS2	RB6PPS1	RB6PPS0	0000 0000	--uu uuuu
1F1Fh	RB7PPS	—	—	—	RB7PPS4	RB7PPS3	RB7PPS2	RB7PPS1	RB7PPS0	0000 0000	--uu uuuu

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

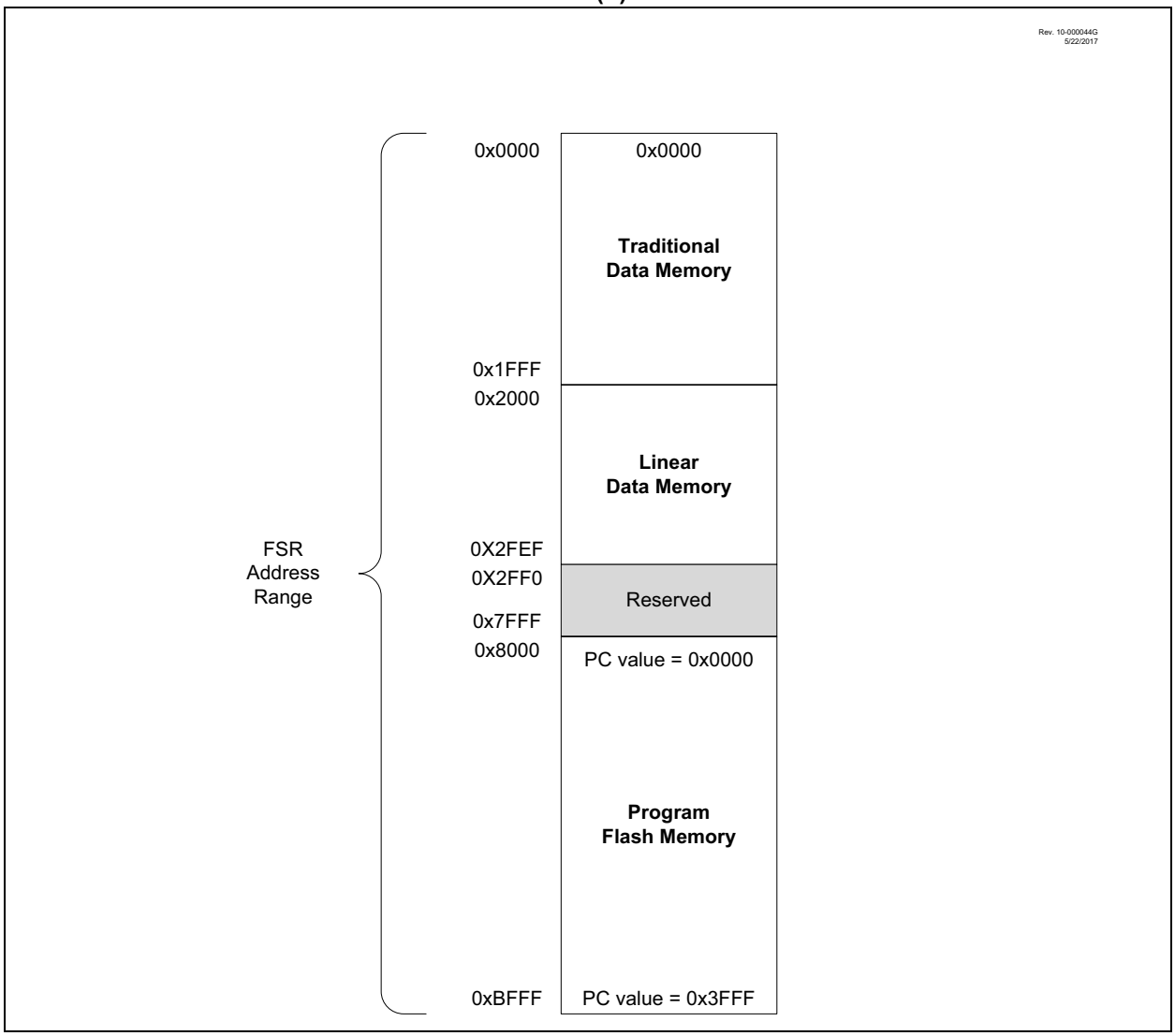
TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 63 (Continued)											
1FB8h	—	Unimplemented								---- ----	---- ----
1FB9h	—	Unimplemented								---- ----	---- ----
1FBAh	—	Unimplemented								---- ----	---- ----
1FBBh	—	Unimplemented								---- ----	---- ----
1FBCh	—	Unimplemented								---- ----	---- ----
1FBDh	—	Unimplemented								---- ----	---- ----
1FBEh	—	Unimplemented								---- ----	---- ----
1FBFh	—	Unimplemented								---- ----	---- ----
1FC0h	—	Unimplemented								---- ----	---- ----
1FC1h	—	Unimplemented								---- ----	---- ----
1FC2h	—	Unimplemented								---- ----	---- ----
1FC3h	—	Unimplemented								---- ----	---- ----
1FC4h	—	Unimplemented								---- ----	---- ----
1FC5h	—	Unimplemented								---- ----	---- ----
1FC6h	—	Unimplemented								---- ----	---- ----
1FC7h	—	Unimplemented								---- ----	---- ----
1FC8h	—	Unimplemented								---- ----	---- ----
1FC9h	—	Unimplemented								---- ----	---- ----
1FCAh	—	Unimplemented								---- ----	---- ----
1FCBh	—	Unimplemented								---- ----	---- ----
1FCCh	—	Unimplemented								---- ----	---- ----
1FCDh	—	Unimplemented								---- ----	---- ----
1FCEh	—	Unimplemented								---- ----	---- ----
1FCFh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

FIGURE 4-9: INDIRECT ADDRESSING PIC16(L)F19156/76/86



6.0 DEVICE INFORMATION AREA

The Device Information Area (DIA) is a dedicated region in the program memory space, it is a new feature in the PIC16(L)F19155/56/75/76/85/86 family of devices. The DIA contains the calibration data for the internal temperature indicator module, stores the Microchip Unique Identifier words and the Fixed Voltage Reference voltage readings measured in mV.

The complete DIA table is shown in Table 6-1, followed by a description of each region and its functionality. The data is mapped from 8100h to 811Fh in the PIC16(L)F19155/56/75/76/85/86 family. These locations are read-only and cannot be erased or modified. The data is programmed into the device during manufacturing.

TABLE 6-1: DEVICE INFORMATION AREA

Address Range	Name of Region	Standard Device Information
8100h-8108h	MUI0	Microchip Unique Identifier (9 Words)
	MUI1	
	MUI2	
	MUI3	
	MUI4	
	MUI5	
	MUI6	
	MUI7	
	MUI8	
8109h	MUI9	1 Word Reserved
810Ah-8111h	EUI0	Unassigned (8 Words)
	EUI1	
	EUI2	
	EUI3	
	EUI4	
	EUI5	
	EUI6	
	EUI7	
8112h	TSLR1	Unassigned (1 word) Temperature indicator ADC reading at 90°C (low-range setting)
8113h	TSLR2	
8114h	TSLR3	Unassigned(1 word)
8115h	TSHR1	Unassigned (1 word) Temperature indicator ADC reading at 90°C (high-range setting)
8116h	TSHR2	
8117h	TSHR3	Unassigned (1 Word)
8118h	FVRA1X	ADC FVR1 Output voltage for 1x setting (in mV)
8119h	FVRA2X	ADC FVR1 Output Voltage for 2x setting (in mV)
811Ah	FVRA4X(1)	ADC FVR1 Output Voltage for 4x setting (in mV)
811Bh	FVRC1X	Comparator FVR2 output voltage for 1x setting (in mV)
811Ch	FVRC2X	Comparator FVR2 output voltage for 2x setting (in mV)
811Dh	FVRC4X(1)	Comparator FVR2 output voltage for 4x setting (in mV)
811Eh-811Fh		Unassigned (1 Word)

Note 1: Value not present on LF devices.

9.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use an internal oscillator block as the system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> bits in the OSCCON1 register to switch the system clock source to the internal oscillator during run-time. See **Section 9.3 "Clock Switching"** for more information.

In **INTOSC** mode, CLKIN is available for general purpose I/O. CLKOUT is available for general purpose I/O or CLKOUT.

The function of the CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

The internal oscillator block has two independent oscillators that can produce two internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates up to 32 MHz. The frequency of HFINTOSC can be selected through the OSCFRQ Frequency Selection register, and fine-tuning can be done via the OSCTUNE register.
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is factory-calibrated and operates at 31 kHz.

9.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a precision digitally-controlled internal clock source that produces a stable clock up to 32 MHz. The HFINTOSC can be enabled through one of the following methods:

- Programming the RSTOSC<2:0> bits in Configuration Word 1 to '110' (1 MHz) or '000' (32 MHz) to set the oscillator upon device Power-up or Reset.
- Write to the NOSC<2:0> bits of the OSCCON1 register during run-time.

The HFINTOSC frequency can be selected by setting the HFFRQ<2:0> bits of the OSCFRQ register.

The MFINTOSC is an internal clock source within the HFINTOSC that provides two (500 kHz, 32 kHz) constant clock outputs. These constant clock outputs are available for selection to various peripherals, internally.

The NDIV<3:0> bits of the OSCCON1 register allow for division of the HFINTOSC output from a range between 1:1 and 1:512.

9.2.2.2 Internal Oscillator Frequency Adjustment

The internal oscillator is factory-calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 9-7).

The default value of the OSCTUNE register is 00h. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WWDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

9.2.2.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a factory calibrated 31 kHz internal clock source.

The LFINTOSC is the frequency for the Power-up Timer (PWRT), Watchdog Timer (WWDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled through one of the following methods:

- Programming the RSTOSC<2:0> bits of Configuration Word 1 to enable LFINTOSC.
- Write to the NOSC<2:0> bits of the OSCCON1 register.

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Windowed Watchdog Timer (WWDT)
- Timer1
- Timer0
- Timer2
- Fail-Safe Clock Monitor (FSCM)
- CLC

9.2.2.4 Oscillator Status and Manual Enable

The 'ready' status of each oscillator is displayed in the OSCSTAT register (Register 9-4). The oscillators can also be manually enabled through the OSCEN register (Register 9-5). Manual enabling makes it possible to verify the operation of the EXTOSC or SOSC crystal oscillators. This can be achieved by enabling the selected oscillator, then watching the corresponding 'ready' state of the oscillator in the OSCSTAT register.

14.4.7 ANALOG CONTROL

The ANSELB register (Register 14-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.4.8 WEAK PULL-UP CONTROL

The WPUB register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.4.9 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 19-5: ADSTAT: ADC STATUS REGISTER

R-0/0	R-0/0	R-0/0	R/HS/HC-0/0	U-0	R-0/0	R-0/0	R-0/0
OV	UTHR	LTHR	MATH	—	STAT<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS/HC = Bit is set/cleared by hardware

bit 7 **OV**: ADC Accumulator Overflow bit
1 = ADC accumulator or ERR calculation have overflowed
0 = ADC accumulator and ERR calculation have not overflowed

bit 6 **UTHR**: ADC Module Greater-than Upper Threshold Flag bit
1 = ERR >UTH
0 = ERR≤UTH

bit 5 **LTHR**: ADC Module Less-than Lower Threshold Flag bit
1 = ERR<LTH
0 = ERR≥LTH

bit 4 **MATH**: ADC Module Computation Status bit
1 = Registers ACC, FLTR, UTH, LTH and the AOV bit are updating or have already updated
0 = Associated registers/bits have not changed since this bit was last cleared

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **STAT<2:0>**: ADC Module Cycle Multistage Status bits(1)
111 = ADC module is in 2nd conversion stage
110 = ADC module is in 2nd acquisition stage
101 = ADC module is in 2nd precharge stage
100 = Not used
011 = ADC module is in 1st conversion stage
010 = ADC module is in 1st acquisition stage
001 = ADC module is in 1st precharge stage
000 = ADC module is not converting

Note 1: If CS = 1, and FOSC<FRC, these bits may be invalid.

TABLE 24-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE RTCC MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182
PMD2	RTCCMD	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	271
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PCON1	—	—	—	—	—	—	$\overline{\text{MEMV}}$	$\overline{\text{VBATBOR}}$	141
RTCCON	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	—	RTCCLKSEL<1:0>		357
RTCCAL	CAL<7:0>								358
ALRMCON	ALRMEN	CHIME	AMASK<3:0>				—	—	361
ALRMRPT	ARPT<7:0>								361
YEAR	YEARH<3:0>				YEARL<3:0>				358
MONTH	—	—	—	MONTHH	MONTHL<3:0>				358
WEEKDAY	—	—	—	—	—	WDAY<2:0>			359
DAY	—	—	DAYH<1:0>		DAYL<3:0>				359
HOURS	—	—	HRH<1:0>		HRL<3:0>				359
MINUTES	—	MINH<2:0>			MINL<3:0>				360
SECONDS	—	SECH<2:0>			SECL<3:0>				360
ALRMMTH	—	—	—	ALRMHMONTH	ALRMLMONTH <3:0>				362
ALRMWD	—	—	—	—	—	ALRMLWDAY<2:0>			362
ALRMDAY	—	—	ALRMHDAY<1:0>		ALRMLDAY<3:0>				362
ALRMHR	—	—	ALRMHHR<1:0>		ALRMLHR<3:0>				363
ALRMMIN	—	ALRMHMIN<2:0>			ALRMLMIN<3:0>				363
ALRMSEC	—	ALRMHSEC<2:0>			ALRMLSEC<3:0>				363

28.1 Register Definitions: SMT Control

Long bit name prefixes for the SMT peripherals are shown in Table 28-1. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information.

TABLE 28-1:

Peripheral	Bit Name Prefix
SMT1	SMT1

REGISTER 28-1: SMTxCON0: SMT CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN(1)	—	STP	WPOL	SPOL	CPOL	SMTxPS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** SMT Enable bit(1)
1 = SMT is enabled
0 = SMT is disabled; internal states are reset, clock requests are disabled

bit 6 **Unimplemented**: Read as '0'

bit 5 **STP:** SMT Counter Halt Enable bit
When SMTxTMR = SMTxPR:
1 = Counter remains SMTxPR; period match interrupt occurs when clocked
0 = Counter resets to 24'h000000; period match interrupt occurs when clocked

bit 4 **WPOL:** SMTxWIN Input Polarity Control bit
1 = SMTxWIN signal is active-low/falling edge enabled
0 = SMTxWIN signal is active-high/rising edge enabled

bit 3 **SPOL:** SMTxSIG Input Polarity Control bit
1 = SMTx_signal is active-low/falling edge enabled
0 = SMTx_signal is active-high/rising edge enabled

bit 2 **CPOL:** SMT Clock Input Polarity Control bit
1 = SMTxTMR increments on the falling edge of the selected clock signal
0 = SMTxTMR increments on the rising edge of the selected clock signal

bit 1-0 **SMTxPS<1:0>:** SMT Prescale Select bits
11 = Prescaler = 1:8
10 = Prescaler = 1:4
01 = Prescaler = 1:2
00 = Prescaler = 1:1

Note 1: Setting EN to '0' does not affect the register contents.

REGISTER 28-4: SMTxCLK: SMT CLOCK SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	CSEL<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **CSEL<2:0>:** SMT Clock Selection bits

111 = Reserved
110 = SOSC
101 = MFINTOSC/16 (31.25 kHz)
100 = MFINTOSC (500 kHz)
011 = LFINTOSC
010 = HFINTOSC
001 = FOSC
000 = FOSC/4

REGISTER 28-7: SMTxTMRL: SMT TIMER REGISTER – LOW BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SMTxTMR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxTMR<7:0>**: Significant bits of the SMT Counter – Low Byte

REGISTER 28-8: SMTxTMRH: SMT TIMER REGISTER – HIGH BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SMTxTMR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxTMR<15:8>**: Significant bits of the SMT Counter – High Byte

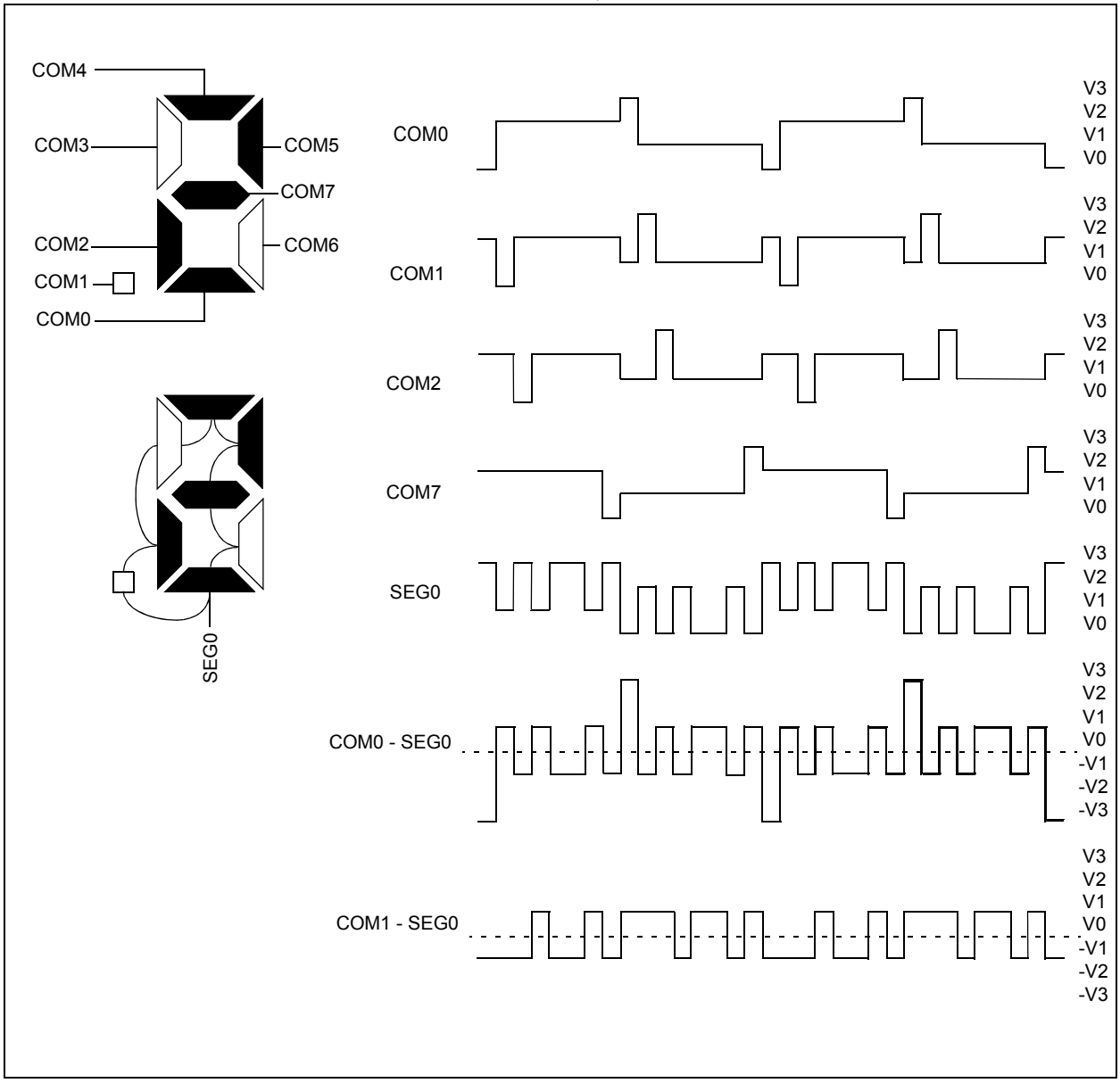
REGISTER 28-9: SMTxTMRU: SMT TIMER REGISTER – UPPER BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SMTxTMR<23:16>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxTMR<23:16>**: Significant bits of the SMT Counter – Upper Byte

FIGURE 35-19: TYPE-B WAVEFORMS IN 1/8 MUX, 1/3 BIAS DRIVE



REGISTER 35-7: LCDRL: LCD INTERNAL REFERENCE LADDER CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
LRLAP1	LRLAP0	LRLBP1	LRLBP0	LCDIRI	LRLAT2	LRLAT1	LRLAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **LRLAP<1:0>**: LCD Reference Ladder A Time Power Control bits

During Time Interval A:

11 = Internal LCD reference is the High-Power (HP) ladder
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 5-4 **LRLBP<1:0>**: LCD Reference Ladder B Time Power Control bits

During Time Interval B:

11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 3 **LCDIRI:** LCD Internal Reference Buffer Idle Enable bit

Allows the Internal reference band gap buffer to shut down when the LCD Reference Ladder is in Power mode 'B'

1 = When the LCD Reference Ladder is in power mode 'B', the LCD Internal Reference Band Gap buffer is disabled
0 = The LCD Internal Reference Buffer ignores the LCD Reference Ladder power mode

bit 2-0 **LRLAT<2:0>**: LCD Reference Ladder A Time Interval Control bits

Sets the number of 32 clock counts when the A Time Interval Power mode is active.

For Type-A Waveforms (WFT = 0):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 9 clocks
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 10 clocks
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 11 clocks
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 12 clocks
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 13 clocks
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 14 clocks
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 15 clocks
000 = Internal LCD reference ladder is always in B Power mode

For Type-B Waveforms (WFT = 1):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 25 clocks
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 26 clocks
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 27 clocks
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 28 clocks
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 29 clocks
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 30 clocks
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 31 clocks
000 = Internal LCD reference ladder is always in B Power mode

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1F5Eh	—	Unimplemented								
1F5Fh	—	Unimplemented								
1F60h	—	Unimplemented								
1F61h	—	Unimplemented								
1F62h	—	Unimplemented								
1F63h	—	Unimplemented								
1F64h	ANSELE	ANSE7	ANSE6	ANSE5	ANSE4	ANSE3	—	ANSE1	ANSE0	249
1F65h	WPUE	WPUE7	WPUE6	WPUE5	WPUE4	WPUE3	—	WPUE1	WPUE0	250
1F66h	ODCONE	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	—	ODCE1	ODCE0	250
1F67h	SLRCONE	SLRE7	SLRE6	SLRE5	SLRE4	SLRE3	—	SLRE1	SLRE0	251
1F68h	INLVLE	INLVLE7	INLVLE6	INLVLE5	INLVLE4	INLVLE3	—	INLVLE1	INLVLE0	251
1F69h	IOCEP	—	—	—	—	IOCEP3	—	—	—	279
1F6Ah	IOCEN	—	—	—	—	IOCEN3	—	—	—	279
1F6Bh	IOCEF	—	—	—	—	IOCEF3	—	—	—	280
1F6Ch	—	Unimplemented								
1F6Dh	—	Unimplemented								
1F6Fh	—	Unimplemented								
1F8Ch	—	Unimplemented								
1F8Dh	—	Unimplemented								
1F8Eh	—	Unimplemented								
1F8Fh	—	Unimplemented								
1F90h	—	Unimplemented								
1F91h	—	Unimplemented								
1F92h	—	Unimplemented								
1F93h	—	Unimplemented								
1F94h	—	Unimplemented								
1F95h	—	Unimplemented								
1F96h	—	Unimplemented								
1F97h	—	Unimplemented								
1F98h	—	Unimplemented								
1F99h	—	Unimplemented								
1F9Ah	—	Unimplemented								
1F9Bh	—	Unimplemented								
1F9Ch	—	Unimplemented								
1F9Dh	—	Unimplemented								
1F9Eh	—	Unimplemented								
1F9Fh	—	Unimplemented								
1FA0h	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

41.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

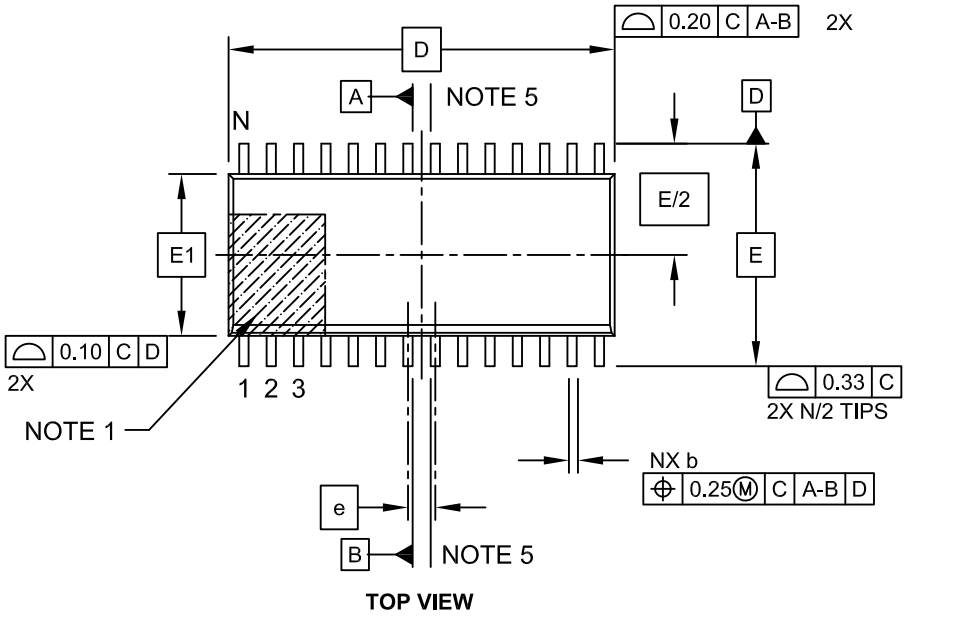
41.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

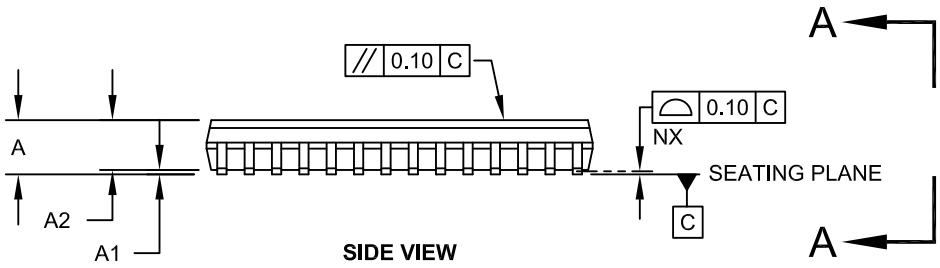
- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

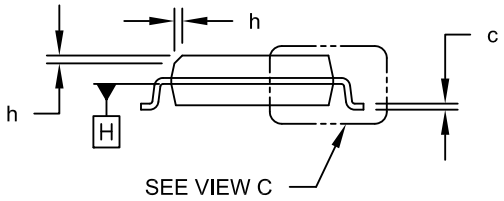
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2