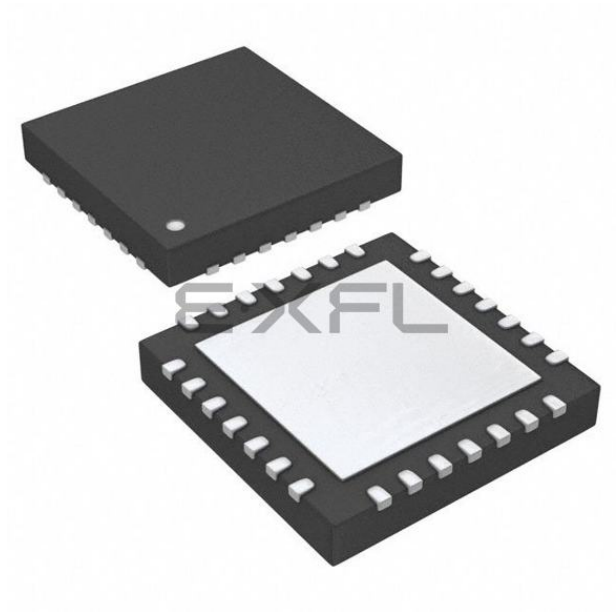

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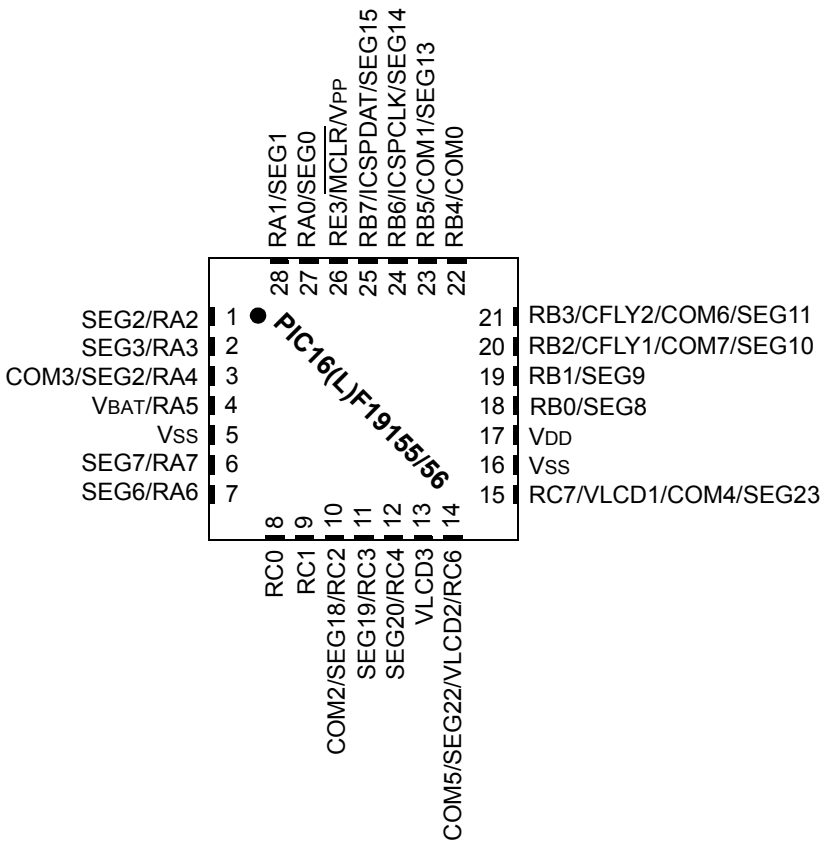
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19155-e-mv

FIGURE 2: 28-PIN UQFN PIN DIAGRAM FOR PIC16(L)F19155/56



Note 1: See Table 3 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

3: The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

TABLE 1-4: PIC16(L)F19185/86 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Types	Output Types	Description
RD7/AND7/SEG31	RD7	TTL/ST	CMOS/OD	General purpose I/O.
	AND7	AN	—	ADC Channel input.
	SEG31	AN	—	LCD Analog output.
RE0/ANE0/SEG32	RE0	TTL/ST	CMOS/OD	General purpose I/O.
	ANE0	AN	—	ADC Channel input.
	SEG32	—	AN	LCD Analog output.
RE1/ANE2/SEG33/COM6	RE1	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel input.
	SEG33	—	AN	LCD analog input
	COM6	—	AN	LCD Driver Common Outputs.
RE2/ANE2/SEG34/COM7	RE2	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel input.
	SEG34	—	AN	LCD analog input
	COM7	—	AN	LCD Driver Common Outputs.
RE3/IOCE3/MCLR	RE3	TTL/ST	CMOS/OD	General purpose I/O.
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	MCLR	ST	—	Master clear input with internal weak pull up resistor.
RF0/ANF0/SEG40	RF0	TTL/ST	CMOS/OD	General purpose I/O.
	ANF0	AN	—	ADC Channel input.
	SEG40	—	AN	LCD Analog output.
RF1/ANF1/SEG41	RF1	TTL/ST	CMOS/OD	General purpose I/O.
	ANF1	AN	—	ADC Channel input.
	SEG41	—	AN	LCD Analog output.
RF2/ANF2/SEG42	RF2	TTL/ST	CMOS/OD	General purpose I/O.
	ANF2	AN	—	ADC Channel input.
	SEG42	—	AN	LCD Analog output.
RF3/ANF3/SEG43	RF3	TTL/ST	CMOS/OD	General purpose I/O.
	ANF3	AN	—	ADC Channel input.
	SEG43	—	AN	LCD Analog output.
RF4/ANF4/SEG44	RF4	TTL/ST	CMOS/OD	General purpose I/O.
	ANF4	AN	—	ADC Channel input.
	SEG44	—	AN	LCD Analog output.
RF5/ANF5/SEG45	RF5	TTL/ST	CMOS/OD	General purpose I/O.
	ANF5	AN	—	ADC Channel input.
	SEG45	—	AN	LCD Analog output.
RF6/ANF6/SEG46	RF6	TTL/ST	CMOS/OD	General purpose I/O.
	ANF6	AN	—	ADC Channel input.
	SEG46	—	AN	LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

8.4 Register Definitions: Brown-out Reset Control

REGISTER 8-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN(1)	—	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-out Reset Enable bit(1)
If BOREN <1:0> in Configuration Words ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN <1:0> in Configuration Words = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

Note 1: BOREN<1:0> bits are located in Configuration Words.

8.5 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) is an essential part of the Rest subsystem. Refer to Figure 8-1 to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external VDD pin. when too low of a voltage is detected, the device is held in Reset. When this occurs, a register bit ($\overline{BOR}$) is changed to indicate that a BOR Reset has occurred. The same bit is set for both the BOR and the LPBOR. Refer to Register 8-2.

8.5.1 ENABLING LPBOR

The LPBOR is controlled by the $\overline{LPBOR}$ bit of the Configuration Word (Register 5-1). When the device is erased, the LPBOR module defaults to disabled.

8.5.2 LPBOR MODULE OUTPUT

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. This signal is OR'd together with the Reset signal of the BOR module to provide the generic $\overline{BOR}$ signal, which goes to the PCON register and to the power control block.

8.6 $\overline{MCLR}$

The $\overline{MCLR}$ is an optional external input that can reset the device. The $\overline{MCLR}$ function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 8-2).

TABLE 8-2: $\overline{MCLR}$ CONFIGURATION

MCLRE	LVP	$\overline{MCLR}$
0	0	Disabled
1	0	Enabled
x	1	Enabled

8.6.1 $\overline{MCLR}$ ENABLED

When $\overline{MCLR}$ is enabled and the pin is held low, the device is held in Reset. The $\overline{MCLR}$ pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

Note:	A Reset does not drive the $\overline{MCLR}$ pin low.

8.6.2 $\overline{MCLR}$ DISABLED

When $\overline{MCLR}$ is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See **Section 14.1 "I/O Priorities"** for more information.

8.7 Windowed Watchdog Timer (WWDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period and the window is open. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register and the $\overline{WDT}$ bit in PCON are changed to indicate a WDT Reset caused by the timer overflowing, and WDTWV bit in the PCON register is changed to indicate a WDT Reset caused by a window violation. See **Section 12.0 "Windowed Watchdog Timer (WWDT)"** for more information.

8.8 RESET Instruction

A RESET instruction will cause a device Reset. The $\overline{RI}$ bit in the PCON register will be set to '0'. See Table 8-4 for default conditions after a RESET instruction has occurred.

8.9 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See **Section 4.5.2 "Overflow/Underflow Reset"** for more information.

8.10 Programming Mode Exit

Upon exit of In-Circuit Serial Programming™ (ICSP™) mode, the device will behave as if a POR had just occurred (the device does not reset upon run time self-programming/erase operations).

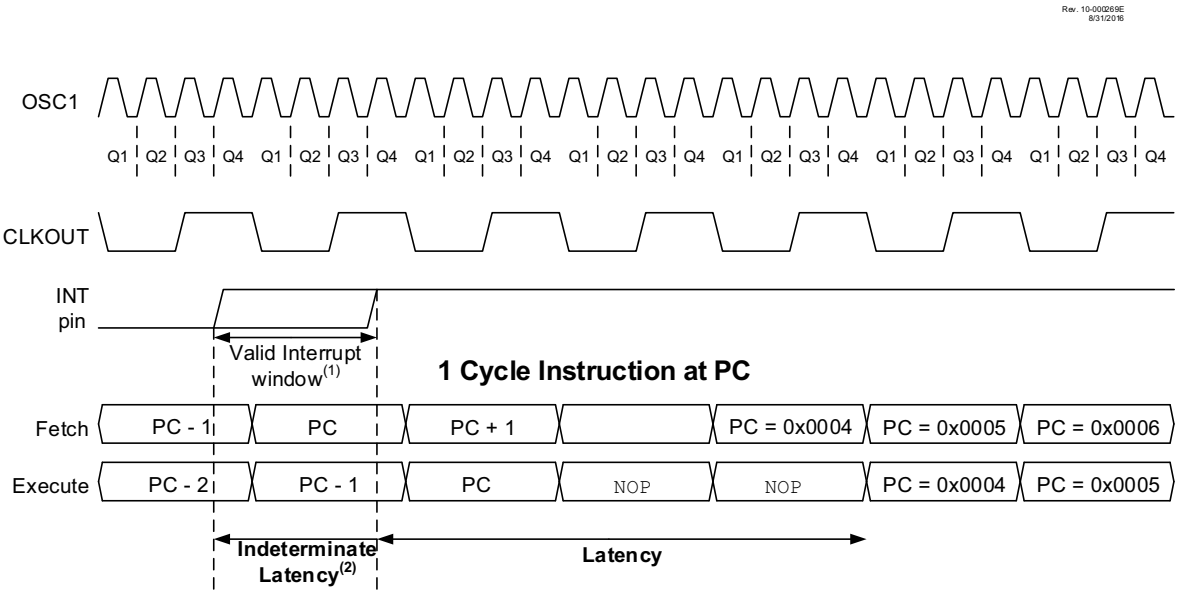
8.11 Power-up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the $\overline{PWRTE}$ bit of the Configuration Words.

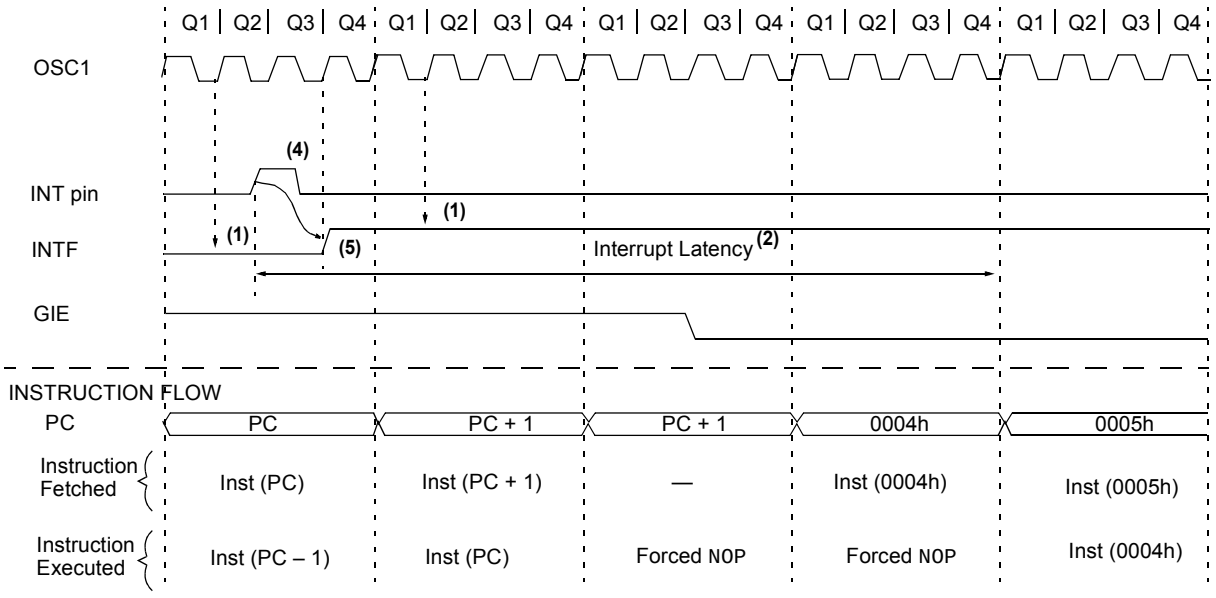
The Power-up Timer provides a nominal 64 ms time out on POR or Brown-out Reset. The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the $\overline{PWRTE}$ bit in the Configuration Words. The Power-up Timer starts after the release of the POR and BOR. For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*" (DS00607).

FIGURE 10-2: INTERRUPT LATENCY



Note 1: An interrupt may occur at any time during the interrupt window.
2: Since an interrupt may occur any time during the interrupt window, the actual latency can vary.

FIGURE 10-3: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: For minimum width of INT pulse, refer to AC specifications in **Section 39.0 "Electrical Specifications"**.

4: INTF is enabled to be set any time during the Q4-Q1 cycles.

10.3 Interrupts During Sleep

Interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 11.0 "Power-Saving Operation Modes"** for more details.

10.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. Refer to Figure 10-3. This interrupt is enabled by setting the INTE bit of the PIE0 register. The INTEDG bit of the INTCON register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the PIR0 register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

10.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for $\overline{TO}$ and $\overline{PD}$)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

REGISTER 14-13: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUB<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 14-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODCB<7:0>:** PORTB Open-Drain Enable bits
For RB<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

TABLE 15-2: PPS INPUT REGISTER VALUES

Desired Input Pin	Value to Write to Register(1)	Desired Input Pin	Value to Write to Register(1)
RA0	0x00	RC7	0x17
RA1	0x01	RD0	0x18
RA2	0x02	RD1	0x19
RA3	0x03	RD2	0x1A
RA4	0x04	RD3	0x1B
RA5	0x05	RD4	0x1C
RA6	0x06	RD5	0x1D
RA7	0x07	RD6	0x1E
RB0	0x08	RD7	0x1F
RB1	0x09	RE0	0x20
RB2	0x0A	RE1	0x21
RB3	0x0B	RE2	0x22
RB4	0x0C	RE3	0x23
RB5	0x0D	RF0	0x28
RB6	0x0E	RF1	0x29
RB7	0x0F	RF2	0x2A
RC0	0x10	RF3	0x2B
RC1	0x11	RF4	0x2C
RC2	0x12	RF5	0x2D
RC3	0x13	RF6	0x2E
RC4	0x14	RF7	0x2F
RC6	0x16		

Note 1: Only a few of the values in this column are valid for any given signal. For example, since the INT signal can only be mapped to PORTA or PORTB pins, only the register values 0x00-0x0F (corresponding to RA<7:0> and RB<7:0>) are valid values to write to the INTPPS register.

TABLE 15-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE (CONTINUED)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
RD1PPS	—	—	—	RD1PPS<4:0>					265
RD2PPS	—	—	—	RD2PPS<4:0>					265
RD3PPS	—	—	—	RD3PPS<4:0>					265
RD4PPS	—	—	—	RD4PPS<4:0>					265
RD5PPS	—	—	—	RD5PPS<4:0>					265
RD6PPS	—	—	—	RD6PPS<4:0>					265
RD7PPS	—	—	—	RD7PPS<4:0>					265
RE0PPS	—	—	—	RE0PPS<4:0>					265
RE1PPS	—	—	—	RE1PPS<4:0>					265
RE2PPS	—	—	—	RE2PPS<4:0>					265
RF0PPS	—	—	—	RF0PPS<4:0>					265
RF1PPS	—	—	—	RF1PPS<4:0>					265
RF2PPS	—	—	—	RF2PPS<4:0>					265
RF3PPS	—	—	—	RF3PPS<4:0>					265
RF4PPS	—	—	—	RF4PPS<4:0>					265
RF5PPS	—	—	—	RF5PPS<4:0>					265
RF6PPS	—	—	—	RF6PPS<4:0>					265
RF7PPS	—	—	—	RF7PPS<4:0>					265

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PPS module.

REGISTER 16-5: PMD4: PMD CONTROL REGISTER 4

R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
UART2MD	UART1MD	—	MSSP1MD	—	—	—	CWG1MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **UART2MD:** Disable EUSART2 bit
1 = EUSART2 module disabled
0 = EUSART2 module enabled

bit 6 **UART1MD:** Disable EUSART1 bit
1 = EUSART1 module disabled
0 = EUSART1 module enabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **MSSP1MD:** Disable MSSP1 bit
1 = MSSP1 module disabled
0 = MSSP1 module enabled

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **CWG1MD:** Disable CWG1 bit
1 = CWG1 module disabled
0 = CWG1 module enabled

REGISTER 19-3: ADCON2: ADC CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0	R/W-0/0	R/W-0/0	R/W-0/0
PSIS	CRS<2:0>			ACLR	MD<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **PSIS:** ADC Previous Sample Input Select bits
1 = PREV is the FLTR value at start-of-conversion
0 = PREV is the RES value at start-of-conversion

bit 6-4 **CRS<2:0>:** ADC Accumulated Calculation Right Shift Select bits
If ADMD = 100:
Low-pass filter time constant is 2^{ADCRS}, filter gain is 1:1
If ADMD = 001, 010 or 011:
The accumulated value is right-shifted by CRS (divided by 2^{ADCRS})**(1,2)**
Otherwise:
Bits are ignored

bit 3 **ACLR:** A/D Accumulator Clear Command bit**(3)**
1 = ACC, AOV and CNT registers are cleared
0 = Clearing action is complete (or not started)

bit 2-0 **MD<2:0>:** ADC Operating Mode Selection bits**(4)**
111-101 = Reserved
100 = Low-pass Filter mode
011 = Burst Average mode
010 = Average mode
001 = Accumulate mode
000 = Basic mode

Note 1: To correctly calculate an average, the number of samples (set in RPT) must be 2^{ADCRS}.
2: ADCRS = 3'b111 is a reserved option.
3: This bit is cleared by hardware when the accumulator operation is complete; depending on oscillator selections, the delay may be many instructions.
4: See Table 19-2 for Full mode descriptions.

20.2.1 CALIBRATION

20.2.1.1 Single-Point Calibration

Single-point calibration is performed by application software using Equation 20-1 and the assumed Mt. A reading of VTSENSE at a known temperature is taken, and the theoretical temperature is calculated by temporarily setting TOFFSET = 0. Then TOFFSET is computed as the difference of the actual and calculated temperatures. Finally, TOFFSET is stored in nonvolatile memory within the device, and is applied to future readings to gain a more accurate measurement.

20.2.1.2 Higher-Order Calibration

If the application requires more precise temperature measurement, additional calibrations steps will be necessary. For these applications, two-point or three-point calibration is recommended.

Note 1:	The TOFFSET value may be determined by the user with a temperature test.
2:	Although the measurement range is -40°C to +125 °C, due to the variations in offset error, the single-point uncalibrated calculated TSENSE value may indicate a temperature from -140°C to +225°C, before the calibration offset is applied.
3:	The user must take into consideration self-heating of the device at different clock frequencies and output pin loading. For package related thermal characteristics information, refer to Table 39-13.

20.2.2 TEMPERATURE RESOLUTION

The resolution of the ADC reading, Ma (°C/count), depends on both the ADC resolution N and the reference voltage used for conversion, as shown in Equation 20-2. It is recommended to use the smallest VREF value, such as 2.048 FVR reference voltage, instead of VDD.

Note:	Refer to Table 39-17 for FVR reference voltage accuracy.

EQUATION 20-2: TEMPERATURE RESOLUTION (°C/LSb)

$$Ma = \frac{V_{REF}}{2^N} \times Mt$$

$$Ma = \frac{\frac{V_{REF}}{2^N}}{Mv}$$

Where:

Mv = sensor voltage sensitivity (V/°C)

VREF = Reference voltage of the ADC module (in Volts)

N = Resolution of the ADC

The typical Mv value for a single diode is approximately -1.267 to -1.32 mV/C.

The typical Mv value for a stack of two diodes (Low Range setting) is approximately -2.533 mV/C.

The typical Mv value for a stack of three diodes (High range setting) is approximately -3.8 mV/C.

20.3 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait a minimum of 25 μs for the ADC value to settle, after the ADC input multiplexer is connected to the temperature indicator output, before the conversion is performed.

21.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC1) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DAC1OUT pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DAC1EN bit of the DAC1CON0 register.

21.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DAC1R<4:0> bits of the DAC1CON1 register.

The DAC output voltage is determined by Equation 21-1:

EQUATION 21-1: DAC OUTPUT VOLTAGE

$$V_{OUT} = \left(V_{SOURCE+} - V_{SOURCE-} \times \frac{DAC1R\langle 4:0 \rangle}{2^5} \right) + (V_{SOURCE-})$$

$$V_{SOURCE+} = V_{DD} \text{ or } V_{REF+} \text{ or } FVR$$

$$V_{SOURCE-} = V_{SS} \text{ or } V_{REF-}$$

21.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in Table 39-16.

21.3 DAC Voltage Reference Output

The DAC voltage can be output to the DAC1OUT1/2 pins by setting the DAC1OE1/2 bits of the DAC1CON0 register, respectively. Selecting the DAC reference voltage for output on the DAC1OUT1/2 pins automatically overrides the digital output buffer and digital input threshold detector functions, disables the weak pull-up, and disables the current-controlled drive function of that pin. Reading the DAC1OUT1/2 pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to the DAC1OUT1/2 pins. Figure 21-2 shows an example buffering technique.

24.1 OPERATION

The RTCC consists of a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1st, 2000 to 23:59:59 on December 31st, 2099.

The hours use the 24-hour time format (military time) with no hardware provisions for regular time format (AM/PM). The clock provides a granularity of one second with additional visibility to the half-second.

The user has visibility to the half second field of the counter. This value is read-only and can be reset only by writing to the lower half of the SECONDS register.

24.1.1 REGISTER INTERFACE

The RTCC register set is divided into the following categories:

Control Registers

- RTCCON
- RTCCAL
- ALRMCON
- ALRMRPT

Clock Value Registers

- YEAR
- MONTH
- DAY
- WEEKDAY
- HOURS
- MINUTES
- SECONDS

Alarm Value Registers

- ALRMMNTH
- ALRMDAY
- ALRMWD
- ALRMHR
- ALRMMIN
- ALRMSEC

Note:	The WEEKDAY register is not automatically derived from the date, but it must be correctly set by the user.

The register interface for the RTCC and alarm values is implemented using the Binary Coded Decimal (BCD) format. This simplifies the firmware when using the module, as each of the digits is contained within its own 4-bit value (see **Section 24.1.3 "Clock Sources"** and Figure 24-3).

All timer registers containing a value of seconds or greater are writable. The user can configure the initial start date and time by writing the year, month, day, hour, minutes and seconds into the clock value registers and the timer will then proceed to count from the newly written values.

The RTCC module is enabled by setting the RTCEN bit (RTCCON<7>). Once the RTCC is enabled, the timer will continue incrementing, even while the clock value registers are being re-written. However, any time the SECONDS register is written to, all of the clock value prescalers are reset to '0'. This allows lower granularity of timer adjustments.

The Timer registers are updated in the same cycle as the `WRITE` instruction's execution by the CPU. The user must ensure that when RTCEN = `1`, the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- By checking the RTCSYNC bit (RTCCON<4>)
- By checking the preceding digits from which a carry can occur
- By updating the registers immediately following the seconds pulse (or alarm interrupt)

24.1.2 WRITE LOCK

To perform a write to any of the RTCC timer registers, the RTCWREN bit must be set. To avoid accidental writes to the timer, it is recommended that the RTCWREN bit is kept clear at any other time.

The RTCEN bit can only be written to when RTCWREN = `1`. A write attempt to this bit while RTCWREN = `0` will be ignored. The RTCC timer registers can be written with RTCEN = `0` or `1`.

REGISTER 24-10: ALRMCON: ALARM CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ALRMEN:** Alarm Enable bit(1)
- 1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 0000 0000 and CHIME = 0)
- 0 = Alarm is disabled

bit 6 **CHIME:** Chime Enable bit
- 1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 00h to FFh
- 0 = Chime is disabled; ARPT<7:0> bits stop once they reach 00h

bit 5-2 **AMASK<3:0>:** Alarm Mask Configuration bits
- 0000 = Every half second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29th, once every four years)
- 101x = Reserved – do not use
- 11xx = Reserved – do not use

bit 1-0 **Unimplemented:** Read as '0'

Note 1: ALRMEN is cleared automatically any time an alarm event occurs when ARPT<7:0> = 00 and CHIME = 0

REGISTER 24-11: ALRMRPT: ALARM REPEAT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(1)
- 00000000 = Alarm will repeat 0 more times
- .
- .
- .
- 11111111 = Alarm will repeat 255 more times

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '255' to '0' unless CHIME = 1.

27.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = `01110`)
- High Reset level (MODE<4:0> = `01111`)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

REGISTER 35-2: LCDPS: LCD PHASE REGISTER

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
WFT	—	LCDA	WA	LP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WFT**: Waveform Type Select bit
1 = Type-B waveform (phase changes on each frame boundary)
0 = Type-A waveform (phase changes within each common type)

bit 6 **Reserved:** Read as '0'

bit 5 **LCDA**: LCD Active Status bit
1 = LCD driver module is active
0 = LCD driver module is inactive

bit 4 **WA**: LCD Write Allow Status bit
This Status bit reflects the value of write_allow signal.
1 = Writes into the LCDDATAx registers are allowed
0 = Writes into the LCDDATAx registers are not allowed

bit 3-0 **LP<3:0>**: LCD Prescaler Select bits
Work with LMUX<3:0> bits to select frame clock prescaler value.
4-Bit Programmable Prescaler = (LP<3:0> + 1)
1111 = 1:16
1110 = 1:15
1101 = 1:14
1100 = 1:13
1011 = 1:12
1010 = 1:11
1001 = 1:10
1000 = 1:9
0111 = 1:8
0110 = 1:7
0101 = 1:6
0100 = 1:5
0011 = 1:4
0010 = 1:3
0001 = 1:2
0000 = 1:1

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1EBEh	CLCIN3PPS	—	—	—	CLCIN3PPS<4:0>					264
1EBFh	—	Unimplemented								
1EC0h	—	Unimplemented								
1EC1h	—	Unimplemented								
1EC2h	—	Unimplemented								
1EC3h	ADCACTPPS	—	—	ADCACTPPS<5:0>						264
1EC4h	—	Unimplemented								
1EC5h	SSP1CLKPPS	—	—	—	SSP1CLKPPS<4:0>					264
1EC6h	SSP1DATPPS	—	—	—	SSP1DATPPS<4:0>					264
1EC7h	SSP1SSPPS	—	—	—	SSP1SSPPS<4:0>					264
1EC8h	—	Unimplemented								
1EC9h	—	Unimplemented								
1ECAh	—	Unimplemented								
1ECBh	RX1PPS	—	—	—	RX1PPS<4:0>					264
1ECCh	TX1PPS	—	—	—	TX1PPS<4:0>					264
1ECDh	RX2PPS	—	—	—	RX2PPS<4:0>					264
1ECEh	TX2PPS	—	—	—	TX2PPS<4:0>					264
1ECFh	—	Unimplemented								
1ED0h	—	Unimplemented								
1ED1h	—	Unimplemented								
1ED2h	—	Unimplemented								
1ED3h	—	Unimplemented								
1ED4h	—	Unimplemented								
1ED5h	—	Unimplemented								
1ED6h	—	Unimplemented								
1ED7h	—	Unimplemented								
1ED8h	—	Unimplemented								
1ED9h	—	Unimplemented								
1EDAh	—	Unimplemented								
1EDBh	—	Unimplemented								
1EDCh	—	Unimplemented								
1EDDh	—	Unimplemented								
1EDEh	—	Unimplemented								
1EDFh	—	Unimplemented								
1EE0h	—	Unimplemented								
1EE1h	—	Unimplemented								
1EE2h	—	Unimplemented								
1EE3h	—	Unimplemented								
1EE4h	—	Unimplemented								
1EE5h	—	Unimplemented								
1EE6h	—	Unimplemented								
1EE7h	—	Unimplemented								
1EE8h	—	Unimplemented								
1EE9h	—	Unimplemented								
1EEAh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

41.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
  - MPLAB® XPRESS IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

41.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

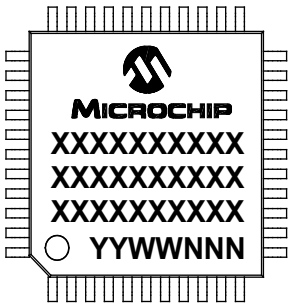
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

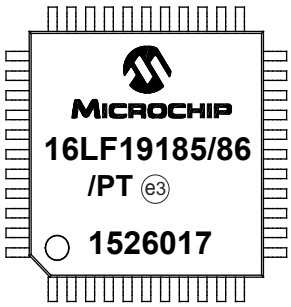
- Local file history feature
- Built-in support for Bugzilla issue tracker

42.1 Package Marking Information (Continued)

48-Lead TQFP (7x7x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.