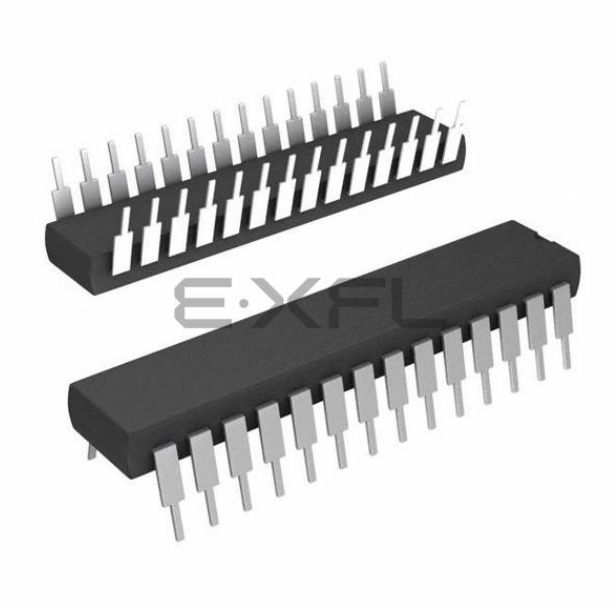

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19155-i-sp

1.0 DEVICE OVERVIEW

The PIC16(L)F19155/56/75/76/85/86 are described within this data sheet. The PIC16(L)F19155/56/75/76/85/86 devices are available in 48-pin TQFP and UQFN, 44-pin TQFP and UQFN, 40-pin PDIP and 28-pin SPDIP, SOIC, SSOP and UQFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F19155/56/75/76/85/86 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F19155/56/75/76/85/86
Analog-to-Digital Converter with Computation (ADC^2)		•
Digital-to-Analog Converter (DAC1)		•
Fixed Voltage Reference (FVR)		•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1 and EUSART2)		•
Temperature Indicator Module (TIM)		•
Zero-Cross Detect (ZCD1)		•
Real-Time Calendar and Clock (RTCC)		•
Liquid Crystal Display (LCD)		•
Capture/Compare/PWM Modules (CCP)		
	CCP1	•
	CCP2	•
Comparator Module (Cx)		
	C1	•
	C2	•
Configurable Logic Cell (CLC)		
	CLC1	•
	CLC2	•
	CLC3	•
	CLC4	•
Complementary Waveform Generator (CWG)		
	CWG1	•
Master Synchronous Serial Ports (MSSP)		
	MSSP1	•
Pulse-Width Modulator (PWM)		
	PWM3	•
	PWM4	•
Signal Measure Timer (SMT)		
	SMT1	•
Timers		
	Timer0	•
	Timer1	•
	Timer2	•
	Timer4	•

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 9											
CPU CORE REGISTERS; see Table 4-3 for specifics											
48Ch	SMT1TMRL	SMT1TMR								0000 0000	0000 0000
48Dh	SMT1TMRH	SMT1TMR								0000 0000	0000 0000
48Eh	SMT1TMRU	SMT1TMR								0000 0000	0000 0000
48Fh	SMT1CPRL	CPR								xxxx xxxx	xxxx xxxx
490h	SMT1CPRH	CPR								xxxx xxxx	xxxx xxxx
491h	SMT1CPRU	CPR								xxxx xxxx	xxxx xxxx
492h	SMT1CPWL	CPW								xxxx xxxx	xxxx xxxx
493h	SMT1CPWH	CPW								xxxx xxxx	xxxx xxxx
494h	SMT1CPWU	CPW								xxxx xxxx	xxxx xxxx
495h	SMT1PRL	SMT1PR								1111 1111	1111 1111
496h	SMT1PRH	SMT1PR								1111 1111	1111 1111
497h	SMT1PRU	SMT1PR								1111 1111	1111 1111
498h	SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		0-00 0000	0-00 0000
499h	SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				00-- 0000	00-- 0000
49Ah	SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	000- -000	000- -000
49Bh	SMT1CLK	—	—	—	—	—	CSEL<2:0>			0000 0000	0000 0000
49Ch	SMT1SIG	—	—	—	SSEL<4:0>					0000 0000	0000 0000
49Dh	SMT1WIN	—	—	—	WSEL<4:0>					0000 0000	0000 0000
49Eh	—	Unimplemented								---- ----	---- ----
49Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 15											
CPU CORE REGISTERS; see Table 4-3 for specifics											
78Ch	—	Unimplemented								---- ----	---- ----
78Dh	—	Unimplemented								---- ----	---- ----
78Eh	—	Unimplemented								---- ----	---- ----
78Fh	—	Unimplemented								---- ----	---- ----
790h	—	Unimplemented								---- ----	---- ----
791h	—	Unimplemented								---- ----	---- ----
792h	—	Unimplemented								---- ----	---- ----
793h	—	Unimplemented								---- ----	---- ----
794h	—	Unimplemented								---- ----	---- ----
795h	—	Unimplemented								---- ----	---- ----
796h	PMD0	SYSCMD	FVRMD	ACTMD	—	—	NVMMD	—	IOCMD	000- -0-0	000- -0-0
797h	PMD1	—	—	—	TMR4MD	—	TMR2MD	TMR1MD	TMR0MD	---0 -000	0000 0000
798h	PMD2	RTCCMD	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	000- -000	000- -000
799h	PMD3	—	—	—	—	PWM4MD	PWM3MD	CCP2MD	CCP1MD	0000 0000	0000 0000
79Ah	PMD4	UART2MD	UART1MD	—	MSSP1MD	—	—	—	CWG1MD	00-0 ---0	00-0 ---0
79Bh	PMD5	—	SMT1MD	LCDMD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	-000 000-	-000 000-
79Ch	—	Unimplemented								---- ----	---- ----
79Dh	—	Unimplemented								---- ----	---- ----
79Eh	—	Unimplemented								---- ----	---- ----
79Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

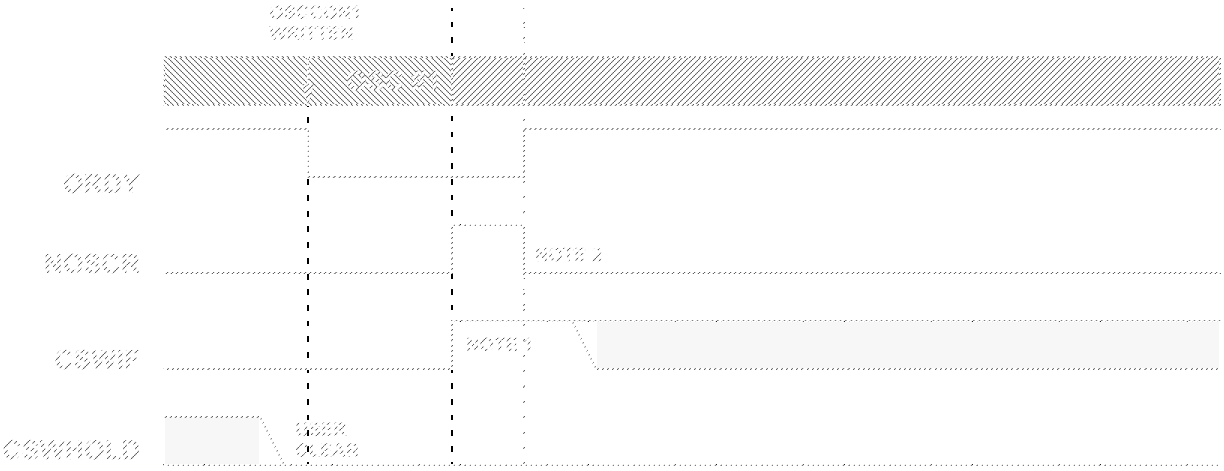
TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 61 (Continued)											
1ECFh	—	Unimplemented								---- ----	---- ----
1ED0h	—	Unimplemented								---- ----	---- ----
1ED1h	—	Unimplemented								---- ----	---- ----
1ED2h	—	Unimplemented								---- ----	---- ----
1ED3h	—	Unimplemented								---- ----	---- ----
1ED4h	—	Unimplemented								---- ----	---- ----
1ED5h	—	Unimplemented								---- ----	---- ----
1ED6h	—	Unimplemented								---- ----	---- ----
1ED7h	—	Unimplemented								---- ----	---- ----
1ED8h	—	Unimplemented								---- ----	---- ----
1ED9h	—	Unimplemented								---- ----	---- ----
1EDAh	—	Unimplemented								---- ----	---- ----
1EDBh	—	Unimplemented								---- ----	---- ----
1EDCh	—	Unimplemented								---- ----	---- ----
1EDDh	—	Unimplemented								---- ----	---- ----
1EDEh	—	Unimplemented								---- ----	---- ----
1EDFh	—	Unimplemented								---- ----	---- ----
1EE0h	—	Unimplemented								---- ----	---- ----
1EE1h	—	Unimplemented								---- ----	---- ----
1EE2h	—	Unimplemented								---- ----	---- ----
1EE3h	—	Unimplemented								---- ----	---- ----
1EE4h	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

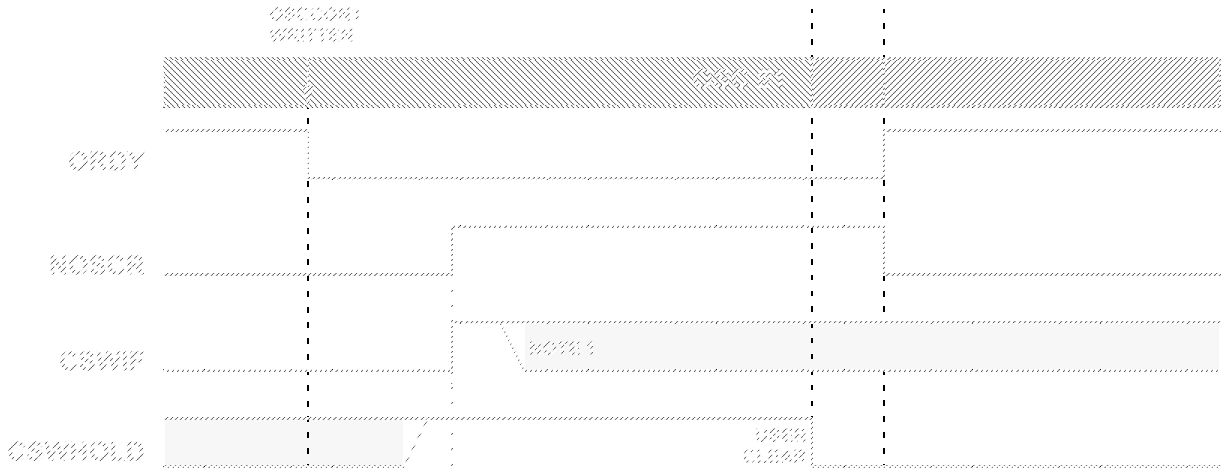
Note 1: Unimplemented data memory locations, read as '0'.

FIGURE 9-4: CLOCK SWITCH (CSWHOLD = 0)



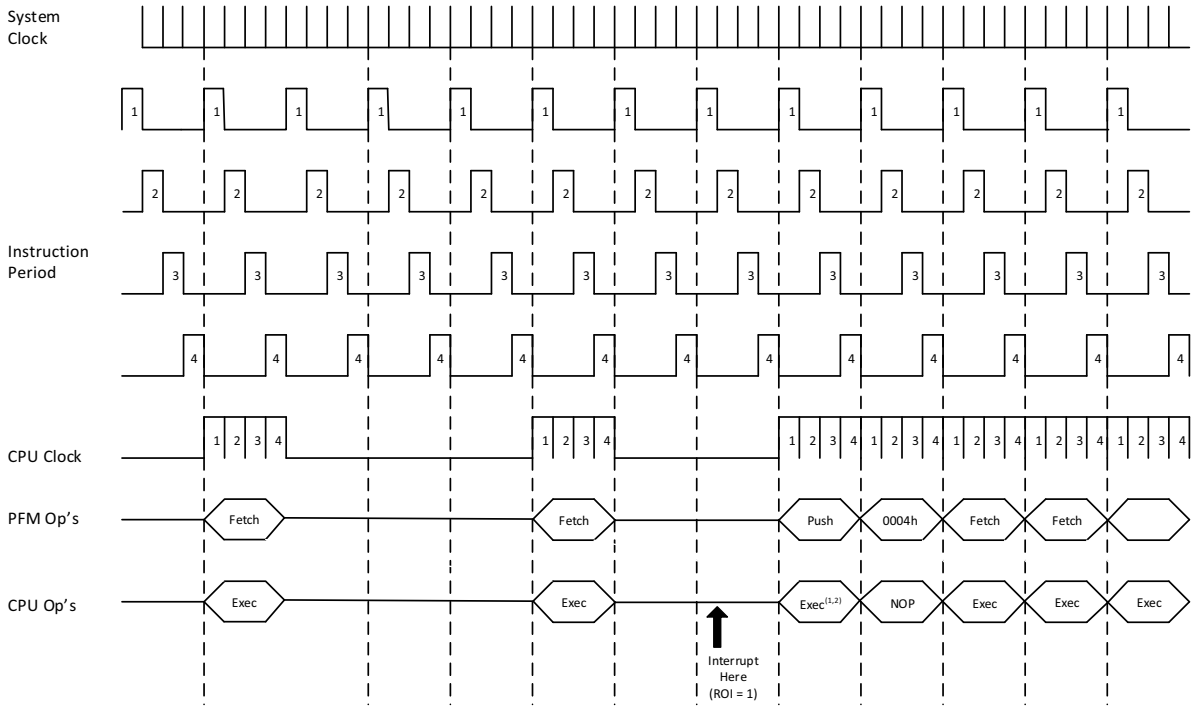
Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 9-5: CLOCK SWITCH (CSWHOLD = 1)



Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

FIGURE 11-1: DOZE MODE OPERATION EXAMPLE



Note 1: Multi-cycle instructions are executed to completion before fetching 0004h.
2: If the pre-fetched instruction clears GIE, the ISR will not occur, but DOZEN is still cleared and the CPU will resume execution at full speed.

11.2 Sleep Mode

Sleep mode is entered by executing the SLEEP instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0). If the SLEEP instruction is executed while the IDLEN bit is set (IDLEN = 1), the CPU will enter the IDLE mode (**Section 11.2.3 "Low-Power Sleep Mode"**).

Upon entering Sleep mode, the following conditions exist:

1. WWDT will be cleared but keeps running if enabled for operation during Sleep
2. The $\overline{PD}$ bit of the STATUS register is cleared
3. The $\overline{TO}$ bit of the STATUS register is set
4. CPU Clock and System Clock
5. 31 kHz LFINTOSC, HFINTOSC and SOSC are unaffected and peripherals using them may continue operation in Sleep.
6. ADC is unaffected if the dedicated FRC oscillator is selected the conversion will be left abandoned if FOSC is selected and ADRES will have an incorrect value
7. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance). This does not apply in the case of any asynchronous peripheral which is active and may affect the I/O port value
8. Resets other than WWDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

EXAMPLE 13-1: PFM PROGRAM MEMORY READ

```
* This code block will read 1 word of program
* memory at the memory address:
    PROG_ADDR_HI : PROG_ADDR_LO
*   data will be returned in the variables;
*   PROG_DATA_HI, PROG_DATA_LO

    BANKSEL  NVMADRL          ; Select Bank for NVMCON registers
    MOVLW    PROG_ADDR_LO     ;
    MOVWF    NVMADRL          ; Store LSB of address
    MOVLW    PROG_ADDR_HI     ;
    MOVWF    NVMADRH          ; Store MSB of address

    BCF      NVMCON1,NVMREGS  ; Do not select Configuration Space
    BSF      NVMCON1,RD       ; Initiate read

    MOVF     NVMDATL,W        ; Get LSB of word
    MOVWF    PROG_DATA_LO     ; Store in user location
    MOVF     NVMDATH,W        ; Get MSB of word
    MOVWF    PROG_DATA_HI     ; Store in user location
```

REGISTER 17-9: IOCCF: INTERRUPT-ON-CHANGE PORTC FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCCF7	IOCCF6	—	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6 **IOCCF<7:6>:** Interrupt-on-Change PORTC Flag bits
1 = An enabled change was detected on the associated pin
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.
0 = No change was detected, or the user cleared the detected change

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **IOCCF<4:0>:** Interrupt-on-Change PORTC Flag bits
1 = An enabled change was detected on the associated pin
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.
0 = No change was detected, or the user cleared the detected change

REGISTER 17-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3(1)	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEP3:** Interrupt-on-Change PORTE Positive Edge Enable bit
1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCEFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

bit 2-0 **Unimplemented:** Read as '0'

Note 1: If MCLRE = 1 or LVP = 1, RC port functionality is disabled and IOC is not available on RE3.

19.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port Configuration
- Channel Selection
- ADC Voltage Reference Selection
- ADC Conversion Clock Source
- Interrupt Control
- Result Formatting
- Conversion Trigger Selection
- ADC Acquisition Time
- ADC Precharge Time
- Additional Sample and Hold Capacitor
- Single/Double Sample Conversion
- Guard Ring Outputs

19.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 14.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

19.1.2 CHANNEL SELECTION

There are several channel selections available:

- Seven PORTA pins
- Eight PORTB pins
- Eight PORTD pins
- Temperature Indicator
- Seven PORTE pins
- Eight PORTF pins
- Seven PORTG pins
- VLCD3 Voltage divided by 4
- V_{BAT} Voltage divided by 3
- DAC output
- Fixed Voltage Reference (FVR)
- V_{SS} (ground)

The ADPCH register determines which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion.

Refer to **Section 19.2 "ADC Operation"** for more information.

19.1.3 ADC VOLTAGE REFERENCE

The PREF<1:0> bits of the ADREF register provide control of the positive voltage reference (V_{REF+}). The positive voltage reference can be:

- V_{REF+} pin
- V_{DD}
- FVR outputs

The negative voltage reference (V_{REF-}) source is:

- V_{SS}

See **Section 18.0 "Fixed Voltage Reference (FVR)"** for more details on the Fixed Voltage Reference.

19.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCLK register and the CS bits of the ADCON0 register. If F_{OSC} is selected as the ADC clock, there is a prescaler available to divide the clock so that it meets the ADC clock period specification. The ADC clock source options are the following:

- $F_{OSC}/(2*n)$(where n is from 1 to 128)
- FRC (dedicated RC oscillator)

The time to complete one bit conversion is defined as T_{AD}. Refer to Figure 19-2 for the complete timing details of the ADC conversion.

For correct conversion, the appropriate T_{AD} specification must be met. Refer to Table 39-13 for more information. Table 19-1 gives examples of appropriate ADC clock selections.

Note 1:	Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.
2:	The internal control logic of the ADC runs off of the clock selected by the CS bit of ADCON0. What this can mean is when the CS bit of ADCON0 is set to '1' (ADC runs on FRC), there may be unexpected delays in operation when setting ADC control bits.

22.9 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Table 39-14 and Table 39-15 for more details.

22.10 Analog Input Connection Considerations

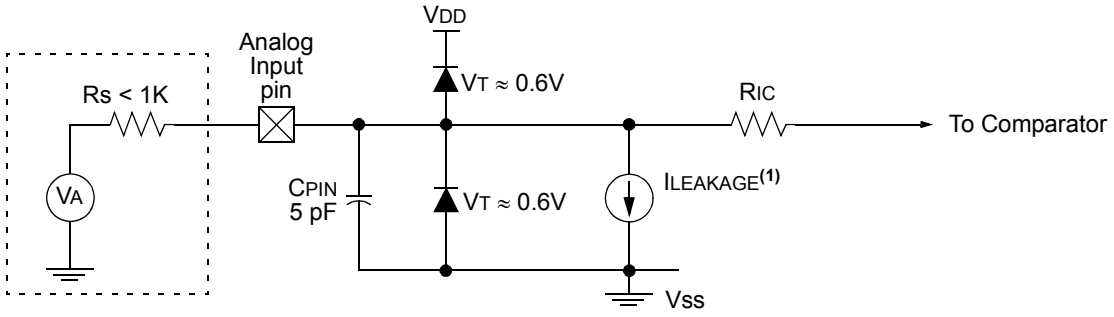
A simplified circuit for an analog input is shown in Figure 22-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to V_{DD} and V_{SS}. The analog input, therefore, must be between V_{SS} and V_{DD}. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 1kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 22-3: ANALOG INPUT MODEL



Legend: C_{PIN} = Input Capacitance
$I_{LEAKAGE}$ = Leakage Current at the pin due to various junctions
R_{IC} = Interconnect Resistance
R_S = Source Impedance
V_A = Analog Voltage
V_T = Threshold Voltage

Note 1: See I/O Ports in Table 39-4.

REGISTER 22-5: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
—	—	—	—	—	—	MC2OUT	MC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **MC2OUT:** Mirror Copy of C2OUT bit

bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

TABLE 22-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CMxCON0	ON	OUT	—	POL	—	—	HYS	SYNC	340
CMxCON1	—	—	—	—	—	—	INTP	INTN	341
CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	343
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		285
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	—	332
DAC1CON1	—	—	—	DAC1R<4:0>					332
INTCON	GIE	PEIE	—					INTEDG	164
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	167
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	176
CLCINxPPS	—	—	—	CLCIN0PPS<4:0>					264
T1GPPS	—	—	—	T1GPPS<4:0>					264

Legend: — = unimplemented location, read as ‘0’. Shaded cells are unused by the comparator module.

REGISTER 25-2: T0CON1: TIMER0 CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0CS<2:0>			T0ASYNC	T0CKPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **T0CS<2:0>:** Timer0 Clock Source select bits
111 = CLC1
110 = SOSC
101 = MFINTOSC (500 kHz)
100 = LFINTOSC
011 = HFINTOSC
010 = FOSC/4
001 = T0CKIPPS (Inverted)
000 = T0CKIPPS (True)

bit 4 **T0ASYNC:** TMR0 Input Asynchronization Enable bit
1 = The input to the TMR0 counter is not synchronized to system clocks
0 = The input to the TMR0 counter is synchronized to FOSC/4

bit 3-0 **T0CKPS<3:0>:** Prescaler Rate Select bit
1111 = 1:32768
1110 = 1:16384
1101 = 1:8192
1100 = 1:4096
1011 = 1:2048
1010 = 1:1024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

27.5.2 HARDWARE GATE MODE

The Hardware Gate modes operate the same as the Software Gate mode except the TMRx_ers external signal gates the timer. When used with the CCP the gating extends the PWM period. If the timer is stopped when the PWM output is high then the duty cycle is also extended.

When MODE<4:0> = 00001 then the timer is stopped when the external signal is high. When MODE<4:0> = 00010 then the timer is stopped when the external signal is low.

Figure 27-5 illustrates the Hardware Gating mode for MODE<4:0> = 00001 in which a high input level starts the counter.

FIGURE 27-5: HARDWARE GATE MODE TIMING DIAGRAM (MODE = 00001)

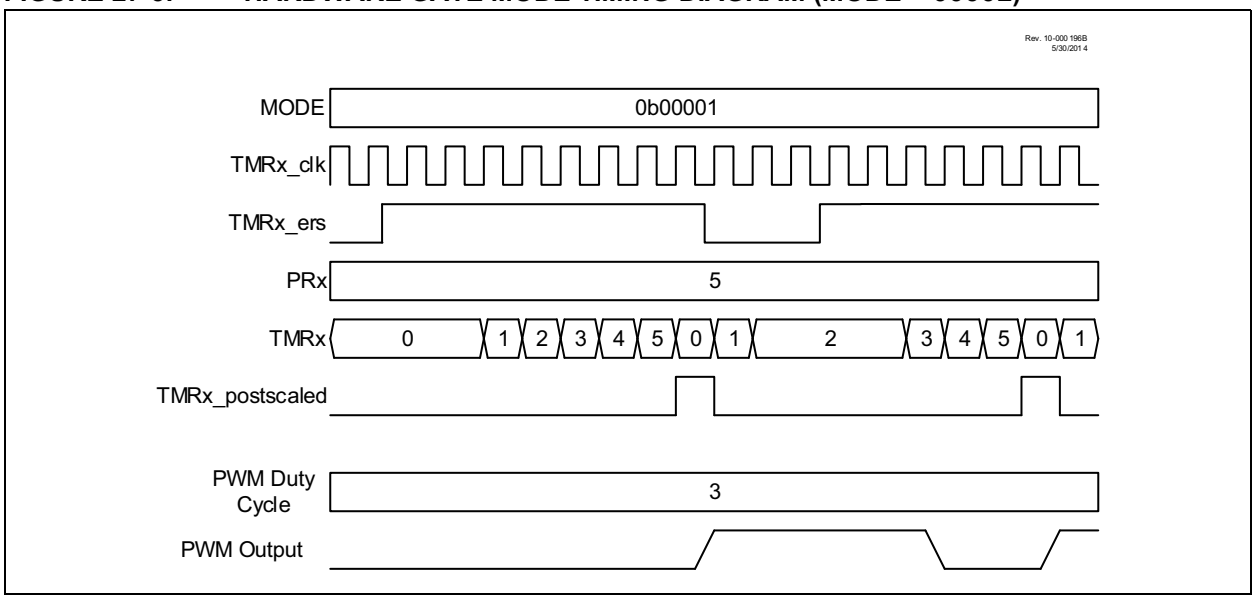
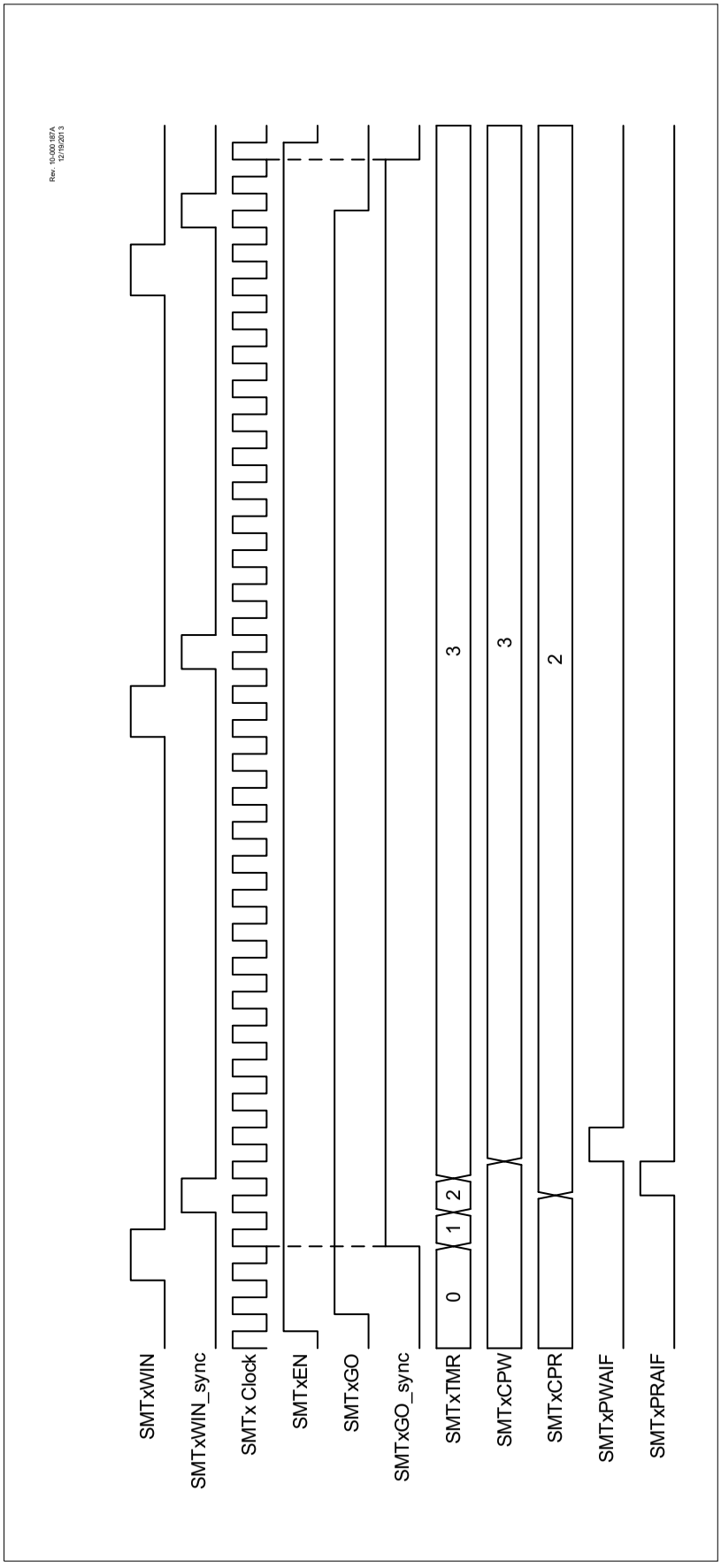


FIGURE 28-17: CAPTURE MODE SINGLE ACQUISITION TIMING DIAGRAM

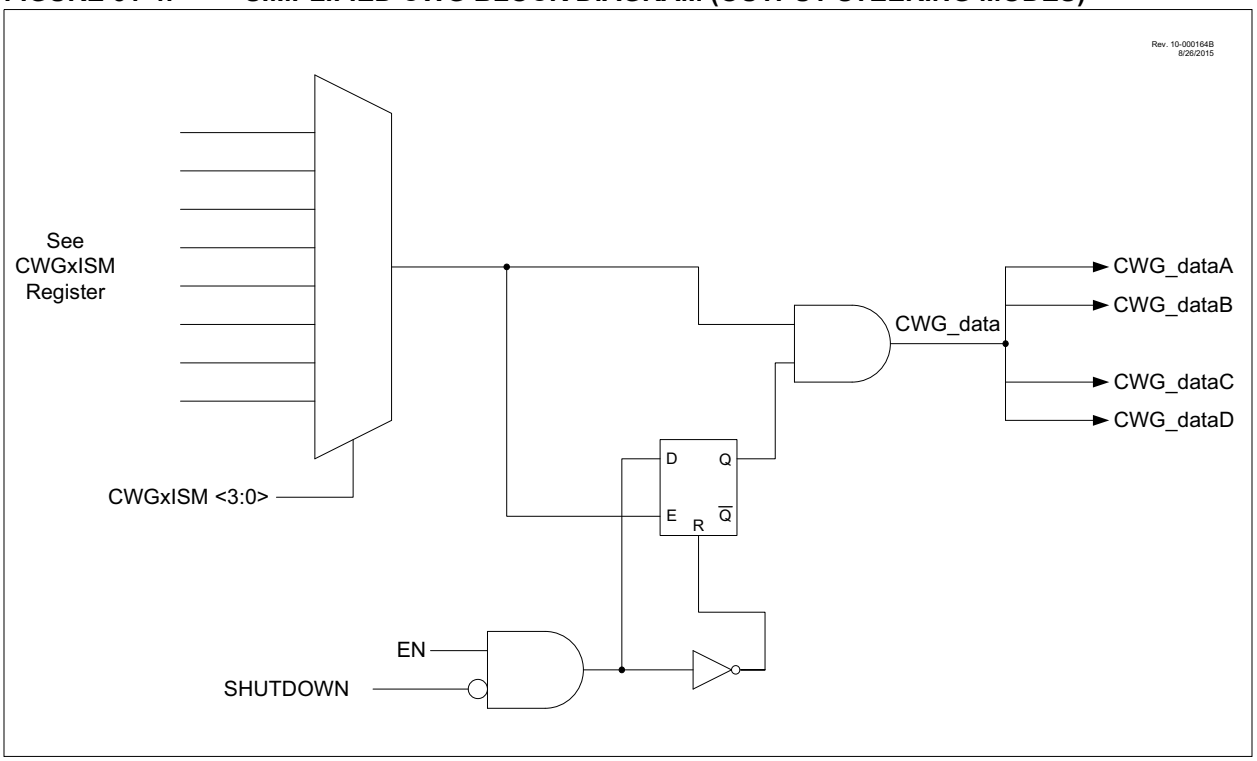


31.1.4 STEERING MODES

In Steering modes, the data input can be steered to any or all of the four CWG output pins. In Synchronous Steering mode, changes to steering selection registers take effect on the next rising input.

In Non-Synchronous mode, steering takes effect on the next instruction cycle. Additional details are provided in **Section 31.9 "CWG Steering Mode"**.

FIGURE 31-4: SIMPLIFIED CWG BLOCK DIAGRAM (OUTPUT STEERING MODES)



31.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the CS bit of the CWG1CLKCON register.

31.13 Register Definitions: CWG Control

Long bit name prefixes for the CWG peripherals are shown in **Section 1.1 "Register and Bit Naming Conventions"**.

REGISTER 31-1: CWG1CON0: CWG1 CONTROL REGISTER 0

R/W-0/0	R/W/HC-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
EN	LD(1)	—	—	—	MODE<2:0>		
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **EN:** CWG1 Enable bit
- 1 = Module is enabled
- 0 = Module is disabled

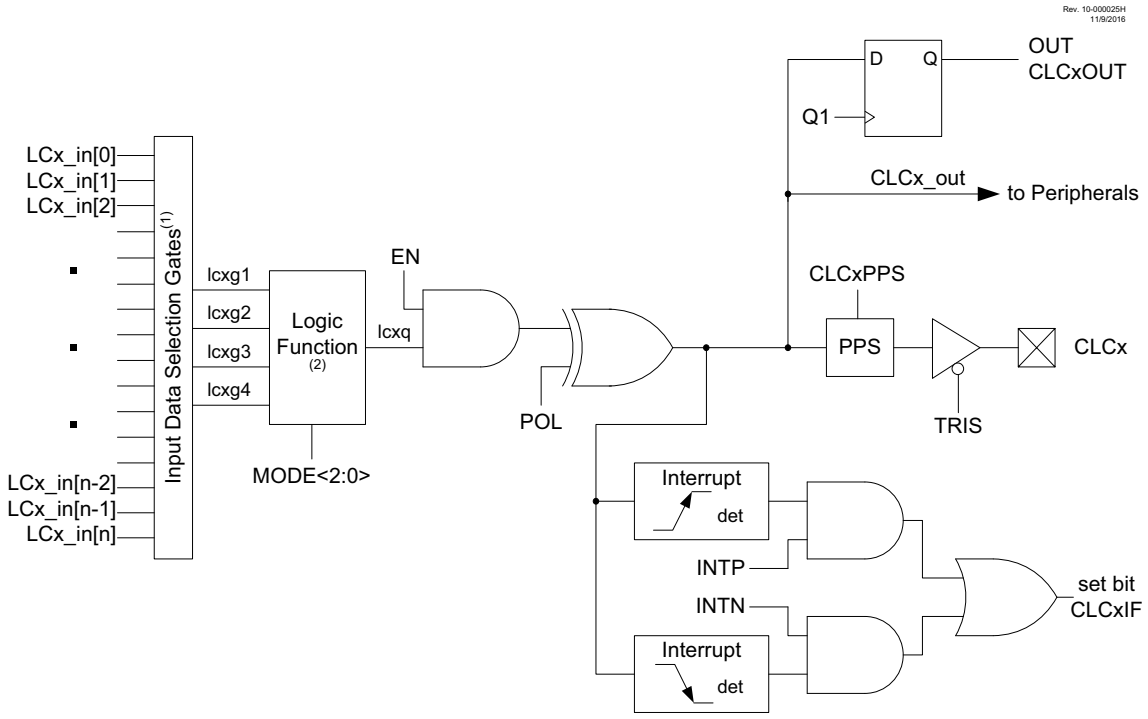
bit 6 **LD:** CWG1 Load Buffer bits(1)
- 1 = Buffers to be loaded on the next rising/falling event
- 0 = Buffers not loaded

bit 5-3 **Unimplemented**: Read as '0'

bit 2-0 **MODE<2:0>:** CWG1 Mode bits
- 111 = Reserved
- 110 = Reserved
- 101 = CWG outputs operate in Push-Pull mode
- 100 = CWG outputs operate in Half-Bridge mode
- 011 = CWG outputs operate in Reverse Full-Bridge mode
- 010 = CWG outputs operate in Forward Full-Bridge mode
- 001 = CWG outputs operate in Synchronous Steering mode
- 000 = CWG outputs operate in Steering mode

Note 1: This bit can only be set after EN = 1 and cannot be set in the same instruction that EN is set.

FIGURE 32-1: CLCx SIMPLIFIED BLOCK DIAGRAM



Note 1: See Figure 32-2: Input Data Selection and Gating
2: See Figure 32-3: Programmable Logic Functions

FIGURE 39-11: ADC CONVERSION TIMING (ADC CLOCK FROM ADCRC)

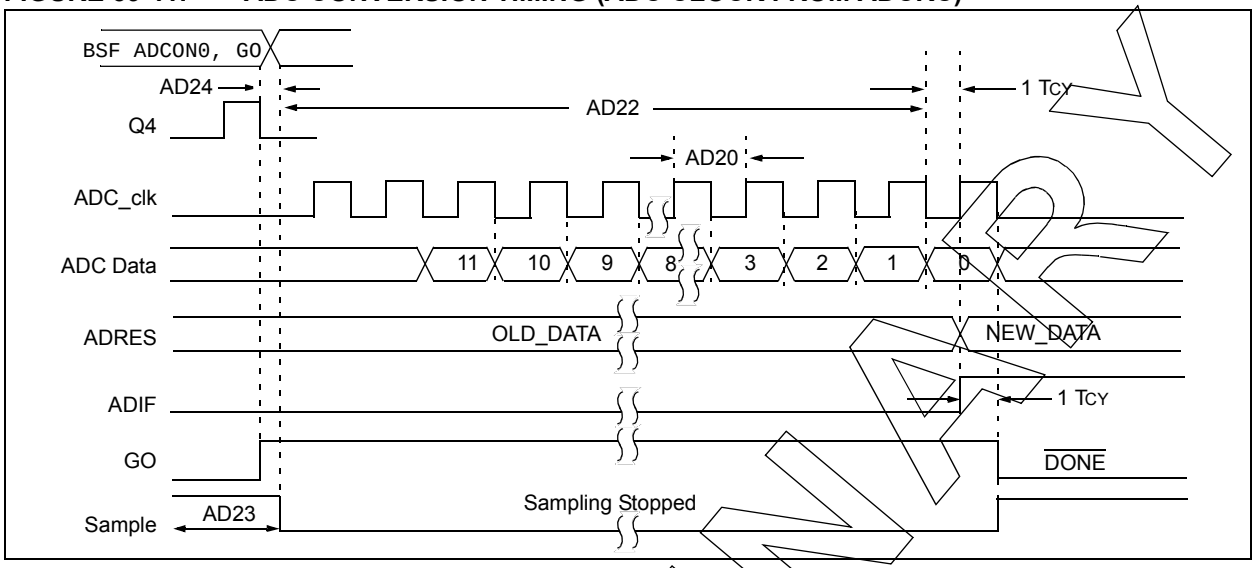


TABLE 39-14: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM01	VIOFF	Input Offset Voltage	—	±30	—	mV	VICM = VDD/2
CM02	VICM	Input Common Mode Range	GND	—	VDD	V	
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM04	VHYST	Comparator Hysteresis	—	25	—	mV	
CM05	TRESP(1)	Response Time, Rising Edge	—	300	600	ns	
		Response Time, Falling Edge	—	220	500	ns	
CMOS6	TMCV2VO(2)	Mode Change to Valid Output	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at VDD/2, while the other input transitions from VSS to VDD.

2: A mode change includes changing any of the control register values, including module enable.

TABLE 39-15: LOW-POWERED CLOCKED COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM07	VIOFF	Input Offset Voltage	—	±30	—	mV	VICM = VDD/2
CM08	VICM	Input Common Mode Range	GND	—	VDD	V	
CM09	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM010	VHYST	Comparator Hysteresis	—	25	—	mV	
CM011	TRESP(1)(3)	Response Time, Rising Edge	—	300	—	ns	
		Response Time, Falling Edge	—	220	—	ns	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at VDD/2, while the other input transitions from VSS to VDD.

2: A mode change includes changing any of the control register values, including module enable.

3: Comparator output state change occurs on the rising edge of LFINTOSC.

TABLE 39-16: 5-BIT DAC SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DSB01	V_{LSB}	Step Size	—	($V_{DACREF+}$ - $V_{DACREF-}$) /32	—	V	
DSB01	V_{ACC}	Absolute Accuracy	—	—	± 0.5	LSb	
DSB03*	R_{UNIT}	Unit Resistor Value	—	5000	—	Ω	
DSB04*	T_{ST}	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '00000' to '01111'.

FIGURE 39-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

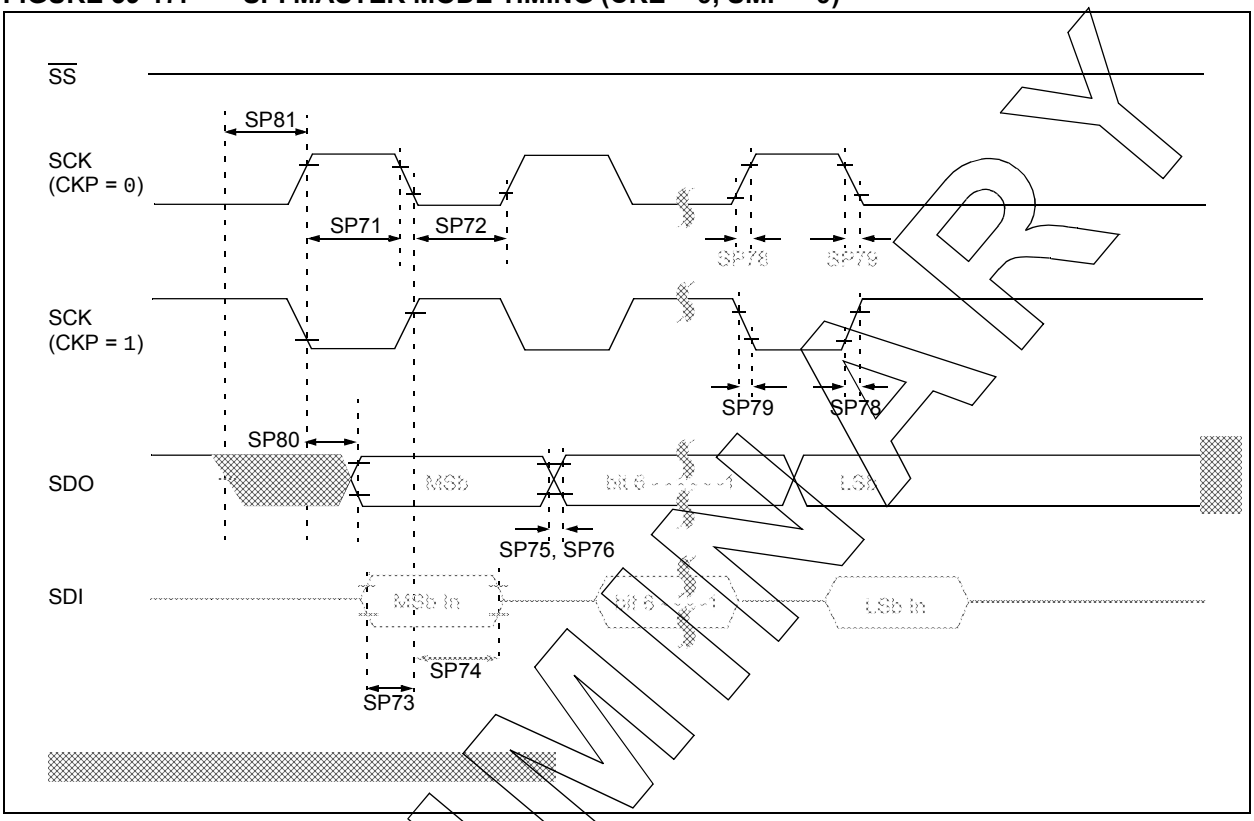
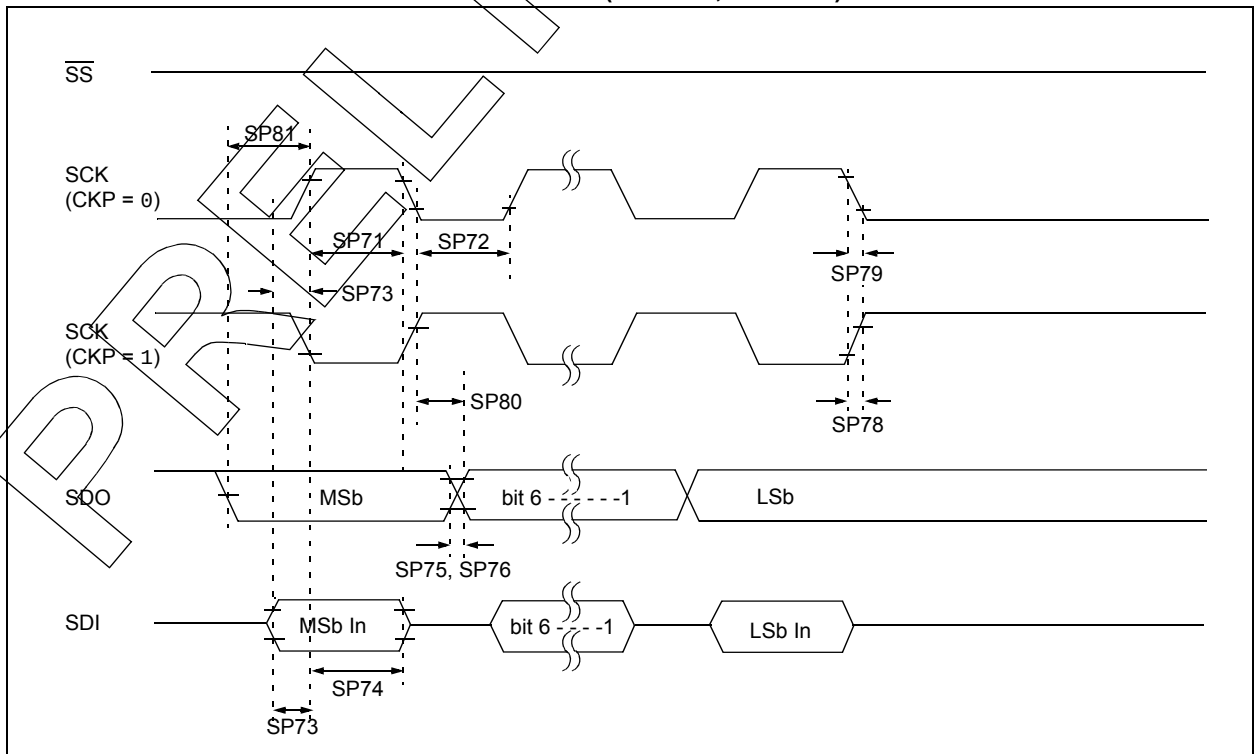


FIGURE 39-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 39-4 for load conditions.