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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19155t-i-ss

TABLE 1-2: PIC16(L)F19155/56 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/C1IN2-/C2IN2-/IOCB3/ANB3/SEG11/COM6/ SEGCFLY2	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
	ANB3	AN	—	ADC Channel input.
	SEG11	—	AN	LCD Analog output.
	COM6	—	AN	LCD Driver Common Outputs.
	SEGCFLY2	AN	—	LCD Drive Charge Pump Capacitor Inputs
RB4/ADCACT(1)/IOCB4/ANB4/COM0	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ADCACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input
	IOCB4	TTL/ST	—	Interrupt-on-change input.
	ANB4	AN	—	ADC Channel input.
	COM0	—	AN	LCD Driver Common Outputs.
RB5/T1G(1)/IOCB5/ANB5/SEG13/COM1	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	T1G(1)	—	—	Timer1 Gate input.
	IOCB5	TTL/ST	—	Interrupt-on-change input.
	ANB5	AN	—	ADC Channel input.
	SEG13	—	AN	LCD Analog output.
	COM1	—	AN	LCD Driver Common Outputs.
RB6/CK2(3)/TX2(1)/CLCIN2(1)/IOCB6/ANB6/SEG14/ ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	CK2(3)	—	—	EUSART synchronous clock out
	TX2(1)	—	—	EUSART asynchronous TX data out
	CLCIN2(1)	—	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	ANB6	AN	—	ADC Channel input.
	SEG14	—	AN	LCD Analog output.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
RB7/DK2(3)/RX2(1)/CLCIN3(1)/IOCB7/ANB7/SEG15/ DAC1OUT2/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	DK2(3)	—	—	EUSART synchronous data output
	RX2(1)	—	—	EUSART receive input.
	CLCIN3(1)	—	—	Configurable Logic Cell source input.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	ANB7	AN	—	ADC Channel input.
	SEG15	—	AN	LCD Analog output.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	TTL/ST	TTL/ST	In-Circuit Serial Programming™ and debugging data input/output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-4: PIC16(L)F19185/86 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Types	Output Types	Description
RF7/ANF7/SEG47	RF7	TTL/ST	CMOS/OD	General purpose I/O.
	ANF7	AN	—	ADC Channel input.
	SEG47	—	AN	LCD Analog output.
VLCD3	VLCD3	AN	—	LCD analog input
VDD	VDD	Power	P	Positive supply voltage input.
VSS	VDD	Power	P	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input'; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

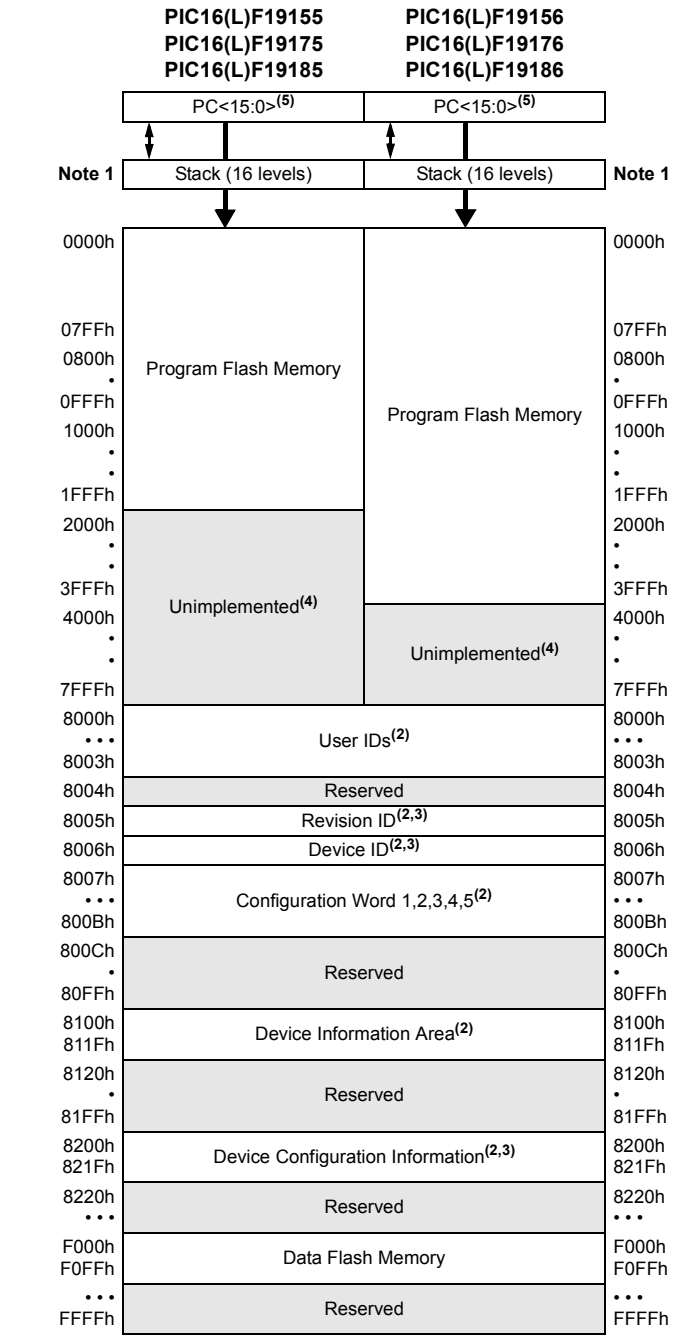
Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F19155/56/75/76/85/86



Note 1: The stack is a separate SRAM panel, apart from all user memory panels.
2: Not code-protected.
3: Device Configuration Information, Device/Revision IDs are hard-coded in silicon.
4: The addresses do not roll over. The region is read as '0'.
5: For the purposes of instruction fetching during program execution, only 15 bits (PC<14:0>) are used. However, for the purposes of nonvolatile memory reading and writing through ICSP™ programming operations, the PC uses all 16 bits (PC<15:0>), and the "Load PC Address" command requires a full 16-bit data payload.

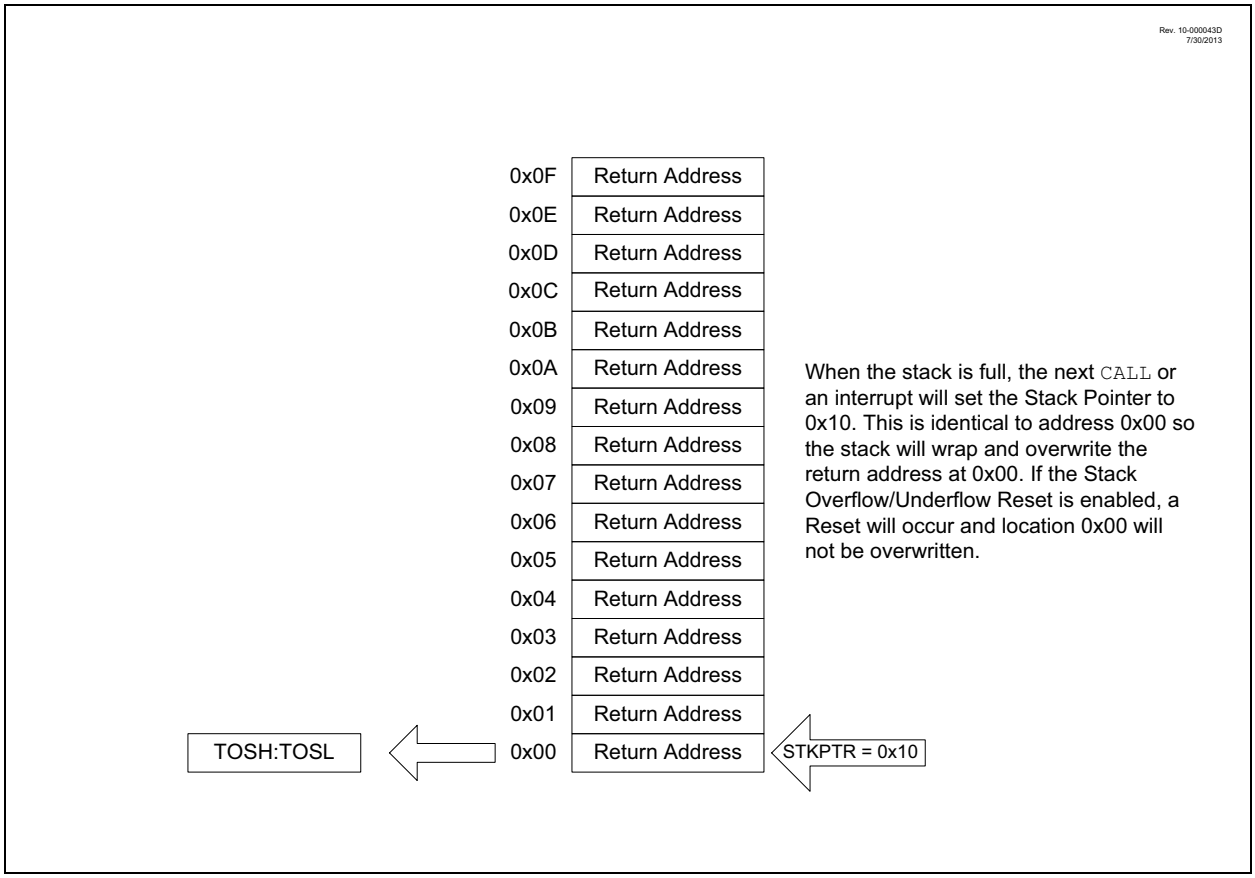
TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 61 (Continued)											
1EE5h	—	Unimplemented								---- ----	---- ----
1EE6h	—	Unimplemented								---- ----	---- ----
1EE7h	—	Unimplemented								---- ----	---- ----
1EE8h	—	Unimplemented								---- ----	---- ----
1EE9h	—	Unimplemented								---- ----	---- ----
1EEAh	—	Unimplemented								---- ----	---- ----
1EEBh	—	Unimplemented								---- ----	---- ----
1EECh	—	Unimplemented								---- ----	---- ----
1EEDh	—	Unimplemented								---- ----	---- ----
1EEEh	—	Unimplemented								---- ----	---- ----
1EEFh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

FIGURE 4-7: ACCESSING THE STACK EXAMPLE 4



4.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words (Register 5-2) is programmed to '1', the device will be Reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

4.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into four memory regions:

- Traditional/Banked Data Memory
- Linear Data Memory
- Program Flash Memory
- EEPROM

REGISTER 10-8: PIE6: PERIPHERAL INTERRUPT ENABLE REGISTER 6

R/W-0/0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
CRIE	—	—	—	—	—	CCP2IE	CCP1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **CRIE:** Clock Recovery Interrupt Enable bit
1 = Clock Recovery interrupt is enabled
0 = Clock Recovery interrupt is disabled

bit 6-2 **Unimplemented:** Read as '0'

bit 1 **CCP2IE:** CCP2 Interrupt Enable bit
1 = CCP2 interrupt is enabled
0 = CCP2 interrupt is disabled

bit 0 **CCP1IE:** CCP1 Interrupt Enable bit
1 = CCP1 interrupt is enabled
0 = CCP1 interrupt is disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

REGISTER 10-14: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

R-0	R-0	R-0	R-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware clearable

bit 7 **RC2IF:** EUSART2 Receive Interrupt Flag (read-only) bit(1)
- 1 = The EUSART2 receive buffer is not empty (contains at least one byte)
- 0 = The EUSART2 receive buffer is empty

bit 6 **TX2IF:** EUSART2 Transmit Interrupt Flag (read-only) bit(1)
- 1 = The EUSART2 transmit buffer contains at least one unoccupied space
- 0 = The EUSART2 transmit buffer is currently full. The application firmware should not write to TXxREG

bit 5 **RC1IF:** EUSART1 Receive Interrupt Flag (read-only) bit (1)
- 1 = The EUSART1 receive buffer is not empty (contains at least one byte)
- 0 = The EUSART1 receive buffer is empty

bit 4 **TX1IF:** EUSART1 Transmit Interrupt Flag (read-only) bit(2)
- 1 = The EUSART1 transmit buffer contains at least one unoccupied space
- 0 = The EUSART1 transmit buffer is currently full. The application firmware should not write to TXxREG again, until more room becomes available in the transmit buffer.

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **BCL1IF:** MSSP1 Bus Collision Interrupt Flag bit
- 1 = A bus collision was detected (must be cleared in software)
- 0 = No bus collision was detected

bit 0 **SSP1IF:** Synchronous Serial Port (MSSP1) Interrupt Flag bit
- 1 = The Transmission/Reception/Bus Condition is complete (must be cleared in software)
- 0 = Waiting for the Transmission/Reception/Bus Condition in progress

Note 1: The RCxIF flag is a read-only bit. To clear the RCxIF flag, the firmware must read from RCxREG enough times to remove all bytes from the receive buffer.

2: The TXxIF flag is a read-only bit, indicating if there is room in the transmit buffer. To clear the TXxIF flag, the firmware must write enough data to TXxREG to completely fill all available bytes in the buffer. The TXxIF flag does not indicate transmit completion (use TRMT for this purpose instead).

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

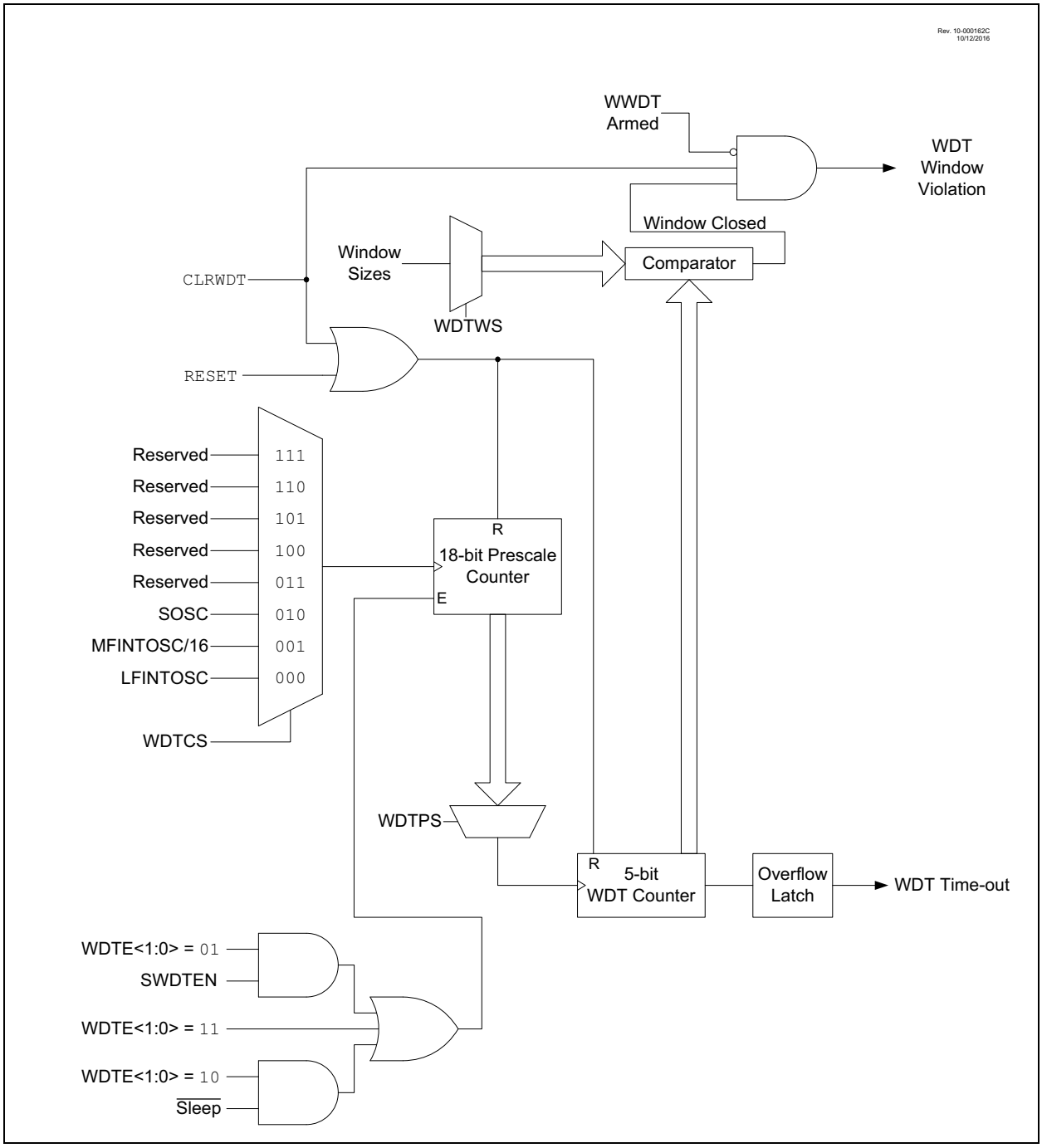
12.0 WINDOWED WATCHDOG TIMER (WWDT)

The Windowed Watchdog Timer (WWDT) is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that CLRWDT instructions are only accepted when they are performed within a specific window during the time-out period.

The WWDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WWDT is always on
  - WWDT is off when in Sleep
  - WWDT is controlled by software
  - WWDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Configurable window size from 12.5 to 100 percent of the time-out period
- Multiple Reset conditions
- Operation during Sleep

FIGURE 12-1: WATCHDOG TIMER BLOCK DIAGRAM



14.7 Register Definitions: PORTC

REGISTER 14-18: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC7	RC6	—	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **RC<7:6>**: PORTC General Purpose I/O Pin bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

bit 5 **Unimplemented:** Read as '0'.

bit 4-0 **RC<4:0>**: PORTC General Purpose I/O Pin bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

REGISTER 14-19: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC7	TRISC6	—	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **TRISC<7:6>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

bit 5 **Unimplemented:** Read as '0'.

bit 4-0 **TRISC<4:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

14.10.6 ANALOG CONTROL

The ANSELE register (Register 14-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELE bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELE bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELE bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.10.7 WEAK PULL-UP CONTROL

The WPUE register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.10.8 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each PORTE pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 19-2: ADCON1: ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0
PPOL	IPEN	GPOL	—	—	—	—	DSEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PPOL:** Precharge Polarity bit
If PRE>0x00:

PPOL	Action During 1st Precharge Stage	
	External (selected analog I/O pin)	Internal (AD sampling capacitor)
1	Connected to V_{DD}	C_{HOLD} connected to V_{SS}
0	Connected to V_{SS}	C_{HOLD} connected to V_{DD}

Otherwise:
The bit is ignored

bit 6 **IPEN:** A/D Inverted Precharge Enable bit
If DSEN = 1
1 = The precharge and guard signals in the second conversion cycle are the opposite polarity of the first cycle
0 = Both Conversion cycles use the precharge and guards specified by ADPPOL and ADGPOL
Otherwise:
The bit is ignored

bit 5 **GPOL:** Guard Ring Polarity Selection bit
1 = ADC guard Ring outputs start as digital high during Precharge stage
0 = ADC guard Ring outputs start as digital low during Precharge stage

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **DSEN:** Double-sample enable bit
1 = Two conversions are performed on each trigger. Data from the first conversion appears in PREV
0 = One conversion is performed for each trigger

26.1 Timer1 Operation

The Timer1 modules are 16-bit incrementing counters which are accessed through the TMR1H:TMR1L register pairs. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

The timer is enabled by configuring the TMR1ON and GE bits in the T1CON and T1GCON registers, respectively. Table 26-1 displays the Timer1 enable selections.

TABLE 26-1: TIMER1 ENABLE SELECTIONS

TMR1ON	TMR1GE	Timer1 Operation
1	1	Count Enabled
1	0	Always On
0	1	Off
0	0	Off

26.2 Clock Source Selection

The T1CLK register is used to select the clock source for the timer. Register 26-3 shows the possible clock sources that may be selected to make the timer increment.

26.2.1 INTERNAL CLOCK SOURCE

When the internal clock source FOSC is selected, the TMR1H:TMR1L register pair will increment on multiples of FOSC as determined by the respective Timer1 prescaler.

When the FOSC internal clock source is selected, the timer register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the TMR1H:TMR1L value. To utilize the full resolution of the timer in this mode, an asynchronous input signal must be used to gate the timer clock input.

Out of the total timer gate signal sources, the following subset of sources can be asynchronous and may be useful for this purpose:

- CLC4 output
- CLC3 output
- CLC2 output
- CLC1 output
- Zero-Cross Detect output
- Comparator2 output
- Comparator1 output
- TxG PPS remappable input pin

26.2.2 EXTERNAL CLOCK SOURCE

When the timer is enabled and the external clock input source (ex: T1CKI PPS remappable input) is selected as the clock source, the timer will increment on the rising edge of the external clock input.

When using an external clock source, the timer can be configured to run synchronously or asynchronously, as described in **Section 26.5 "Timer Operation in Asynchronous Counter Mode"**.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used connected to the SOSCI/SOSCO pins.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- The timer is first enabled after POR
- Firmware writes to TMR1H or TMR1L
- The timer is disabled
- The timer is re-enabled (e.g., TMR1ON-->1) when the T1CKI signal is currently logic low.

REGISTER 28-10: SMTxCPRL: SMT CAPTURED PERIOD REGISTER – LOW BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
SMTxCPR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxCPR<7:0>**: Significant bits of the SMT Period Latch – Low Byte

REGISTER 28-11: SMTxCPRH: SMT CAPTURED PERIOD REGISTER – HIGH BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
SMTxCPR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxCPR<15:8>**: Significant bits of the SMT Period Latch – High Byte

REGISTER 28-12: SMTxCPRU: SMT CAPTURED PERIOD REGISTER – UPPER BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
SMTxCPR<23:16>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxCPR<23:16>**: Significant bits of the SMT Period Latch – Upper Byte

FIGURE 31-6: DEAD-BAND OPERATION CWG1DBR = 0X01, CWG1DBF = 0X02

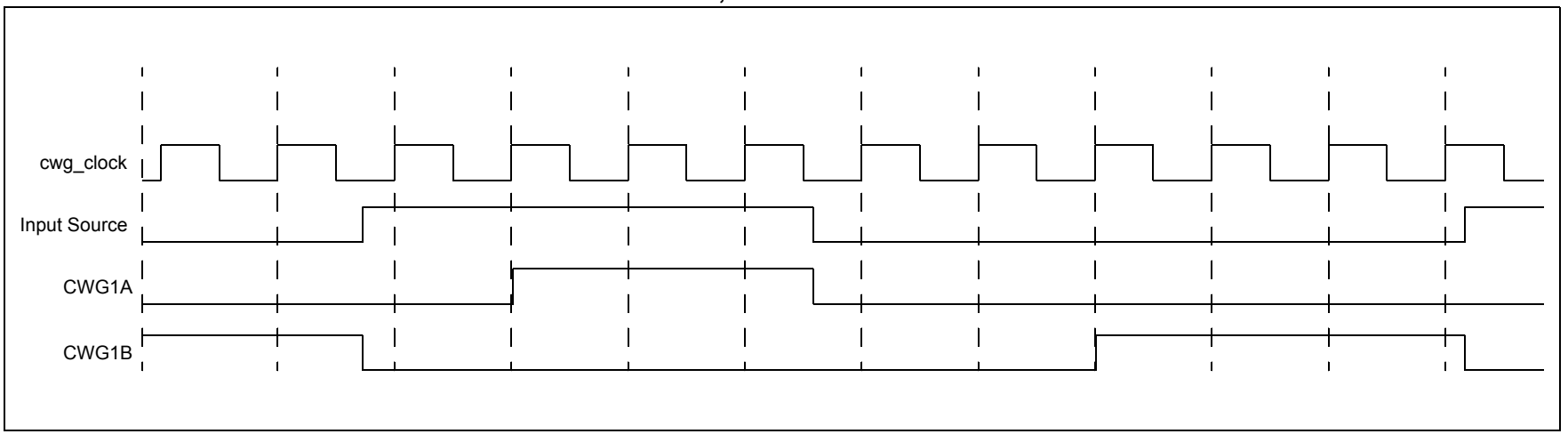
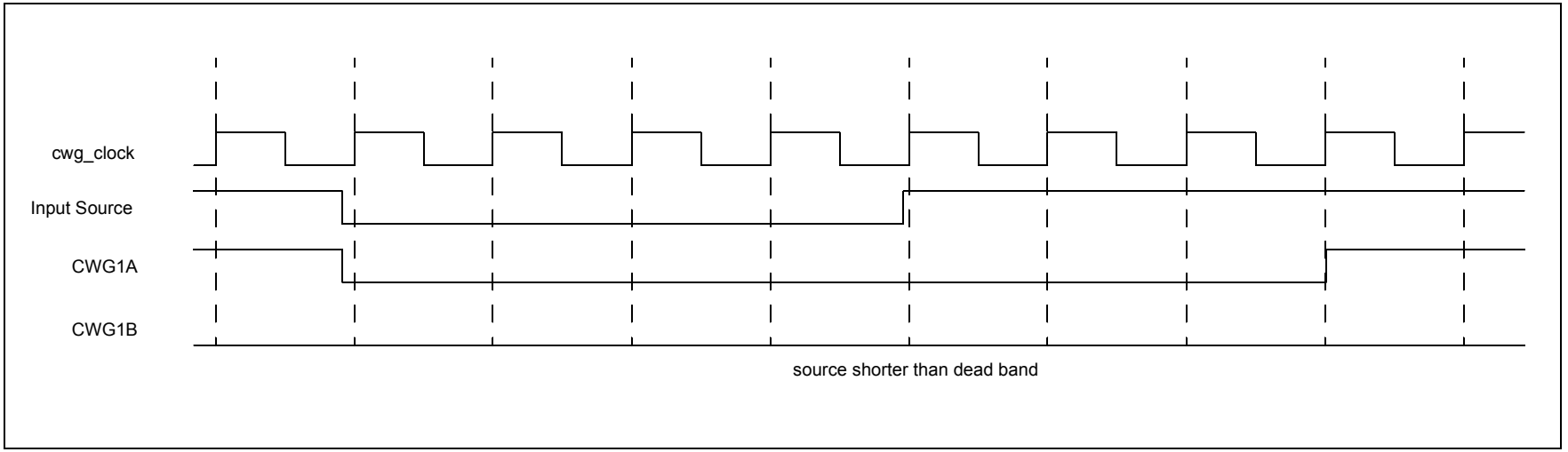


FIGURE 31-7: DEAD-BAND OPERATION, CWG1DBR = 0X03, CWG1DBF = 0X04, SOURCE SHORTER THAN DEAD BAND



33.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPxADD register (Register 33-6). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

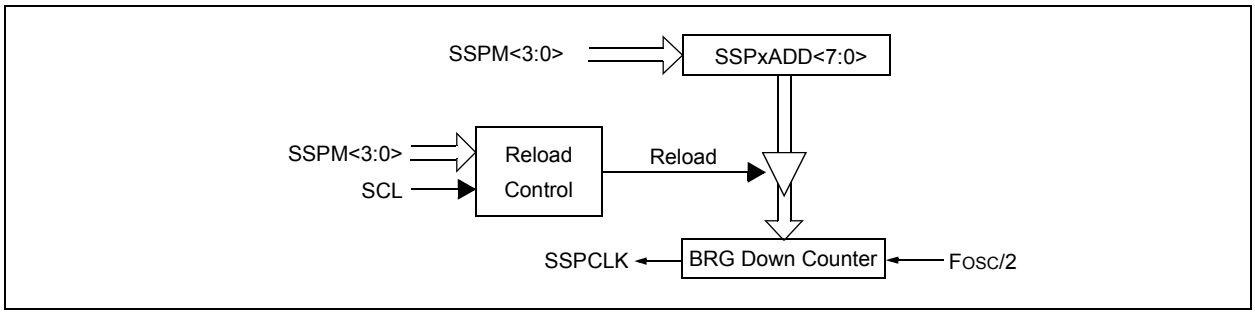
An internal signal “Reload” in Figure 33-40 triggers the value from SSPxADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 33-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

EQUATION 33-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSP1ADD + 1)(4)}$$

FIGURE 33-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of `0x00`, `0x01` and `0x02` are not valid for SSPxADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

TABLE 33-2: MSSP CLOCK RATE W/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in Table 39-4 to ensure the system is designed to support I/O requirements.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
51Bh	—	Unimplemented								
51Ch	—	Unimplemented								
51Dh	—	Unimplemented								
51Eh	—	Unimplemented								
51Fh	—	Unimplemented								
58Ch	—	Unimplemented								
58Dh	—	Unimplemented								
58Eh	—	Unimplemented								
58Fh	—	Unimplemented								
590h	—	Unimplemented								
591h	—	Unimplemented								
592h	—	Unimplemented								
593h	—	Unimplemented								
594h	—	Unimplemented								
595h	—	Unimplemented								
596h	—	Unimplemented								
597h	—	Unimplemented								
598h	—	Unimplemented								
599h	—	Unimplemented								
59Ah	—	Unimplemented								
59Bh	—	Unimplemented								
59Ch	TMR0L	TMR0L								
59Dh	TMR0H	TMR0H								
		T0PR								
59Eh	T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				368
59Fh	T0CON1	T0CS<2:0>			T0ASYNC	T0CKPS<3:0>				369
60Ch	CWG1CLKCON	—	—	—	—	—	—	—	CS	492
60Dh	CWG1ISM	—	—	—	—	IS<3:0>				492
60Eh	CWG1DBR	—	—	DBR<5:0>						488
60Fh	CWG1DBF	—	—	DBF<5:0>						488
610h	CWG1CON0	EN	LD	—	—	—	MODE<2:0>			486
611h	CWG1CON1	—	—	IN	—	POLD	POLC	POLB	POLA	487
612h	CWG1AS0	SHUT-DOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	489
613h	CWG1AS1	—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	490
614h	CWG1STR	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	491
615h	—	Unimplemented								
616h	—	Unimplemented								
617h	—	Unimplemented								
618h	—	Unimplemented								
619h	—	Unimplemented								
61Ah	—	Unimplemented								
61Bh	—	Unimplemented								
61Ch	—	Unimplemented								
61Dh	—	Unimplemented								
61Eh	—	Unimplemented								
61Fh	—	Unimplemented								
68Ch	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

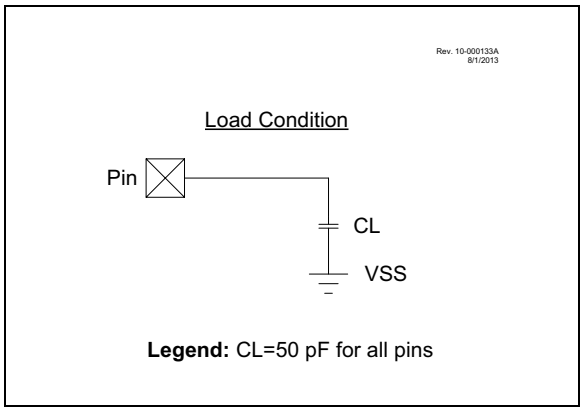
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1EEBh	—	Unimplemented								
1EECh	—	Unimplemented								
1EEDh	—	Unimplemented								
1EEEh	—	Unimplemented								
1EEFh	—	Unimplemented								
1F0Ch	—	Unimplemented								
1F0Dh	—	Unimplemented								
1F0Eh	—	Unimplemented								
1F0Fh	—	Unimplemented								
1F10h	RA0PPS	—	—	—	RA0PPS4	RA0PPS3	RA0PPS2	RA0PPS1	RA0PPS0	265
1F11h	RA1PPS	—	—	—	RA1PPS4	RA1PPS3	RA1PPS2	RA1PPS1	RA1PPS0	265
1F12h	RA2PPS	—	—	—	RA2PPS4	RA2PPS3	RA2PPS2	RA2PPS1	RA2PPS0	265
1F13h	RA3PPS	—	—	—	RA3PPS4	RA3PPS3	RA3PPS2	RA3PPS1	RA3PPS0	265
1F14h	RA4PPS	—	—	—	RA4PPS4	RA4PPS3	RA4PPS2	RA4PPS1	RA4PPS0	265
1F15h	RA5PPS	—	—	—	RA5PPS4	RA5PPS3	RA5PPS2	RA5PPS1	RA5PPS0	265
1F16h	RA6PPS	—	—	—	RA6PPS4	RA6PPS3	RA6PPS2	RA6PPS1	RA6PPS0	265
1F17h	RA7PPS	—	—	—	RA7PPS4	RA7PPS3	RA7PPS2	RA7PPS1	RA7PPS0	265
1F18h	RB0PPS	—	—	—	RB0PPS4	RB0PPS3	RB0PPS2	RB0PPS1	RB0PPS0	265
1F19h	RB1PPS	—	—	—	RB1PPS4	RB1PPS3	RB1PPS2	RB1PPS1	RB1PPS0	265
1F1Ah	RB2PPS	—	—	—	RB2PPS4	RB2PPS3	RB2PPS2	RB2PPS1	RB2PPS0	265
1F1Bh	RB3PPS	—	—	—	RB3PPS4	RB3PPS3	RB3PPS2	RB3PPS1	RB3PPS0	265
1F1Ch	RB4PPS	—	—	—	RB4PPS4	RB4PPS3	RB4PPS2	RB4PPS1	RB4PPS0	265
1F1Dh	RB5PPS	—	—	—	RB5PPS4	RB5PPS3	RB5PPS2	RB5PPS1	RB5PPS0	265
1F1Eh	RB6PPS	—	—	—	RB6PPS4	RB6PPS3	RB6PPS2	RB6PPS1	RB6PPS0	265
1F1Fh	RB7PPS	—	—	—	RB7PPS4	RB7PPS3	RB7PPS2	RB7PPS1	RB7PPS0	265
1F20h	RC0PPS	—	—	—	RC0PPS4	RC0PPS3	RC0PPS2	RC0PPS1	RC0PPS0	265
1F21h	RC1PPS	—	—	—	RC1PPS4	RC1PPS3	RC1PPS2	RC1PPS1	RC1PPS0	265
1F22h	RC2PPS	—	—	—	RC2PPS4	RC2PPS3	RC2PPS2	RC2PPS1	RC2PPS0	265
1F23h	RC3PPS	—	—	—	RC3PPS4	RC3PPS3	RC3PPS2	RC3PPS1	RC3PPS0	265
1F24h	RC4PPS	—	—	—	RC4PPS4	RC4PPS3	RC4PPS2	RC4PPS1	RC4PPS0	265
1F25h	—	Unimplemented								
1F26h	RC6PPS	—	—	—	RC6PPS4	RC6PPS3	RC6PPS2	RC6PPS1	RC6PPS0	265
1F27h	RC7PPS	—	—	—	RC7PPS4	RC7PPS3	RC7PPS2	RC7PPS1	RC7PPS0	265
1F28h	RD0PPS	—	—	—	RD0PPS4	RD0PPS3	RD0PPS2	RD0PPS1	RD0PPS0	265
1F29h	RD1PPS	—	—	—	RD1PPS4	RD1PPS3	RD1PPS2	RD1PPS1	RD1PPS0	265
1F2Ah	RD2PPS	—	—	—	RD2PPS4	RD2PPS3	RD2PPS2	RD2PPS1	RD2PPS0	265
1F2Bh	RD3PPS	—	—	—	RD3PPS4	RD3PPS3	RD3PPS2	RD3PPS1	RD3PPS0	265
1F2Ch	RD4PPS	—	—	—	RD4PPS4	RD4PPS3	RD4PPS2	RD4PPS1	RD4PPS0	265
1F2Dh	RD5PPS	—	—	—	RD5PPS4	RD5PPS3	RD5PPS2	RD5PPS1	RD5PPS0	265
1F2Eh	RD6PPS	—	—	—	RD6PPS4	RD6PPS3	RD6PPS2	RD6PPS1	RD6PPS0	265
1F2Fh	RD7PPS	—	—	—	RD7PPS4	RD7PPS3	RD7PPS2	RD7PPS1	RD7PPS0	265
1F30h	RE0PPS	—	—	—	RE0PPS4	RE0PPS3	RE0PPS2	RE0PPS1	RE0PPS0	265
1F31h	RE1PPS	—	—	—	RE1PPS4	RE1PPS3	RE1PPS2	RE1PPS1	RE1PPS0	265
1F32h	RE2PPS	—	—	—	RE2PPS4	RE2PPS3	RE2PPS2	RE2PPS1	RE2PPS0	265

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

39.4 AC Characteristics

FIGURE 39-4: LOAD CONDITIONS



Legend: CL=50 pF for all pins

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F19155, PIC16(L)F19155 PIC16F19156, PIC16(L)F19156 PIC16F19175, PIC16(L)F19175 PIC16F19176, PIC16(L)F19176 PIC16F19185, PIC16(L)F19185 PIC16F19186, PIC16(L)F19186	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:(2)	SS SO SP MV P MV PT MV PT	= 28-lead SSOP = 28-lead SOIC = 28-lead SPDIP = 28-lead UQFN = 40-lead PDIP = 40-lead UQFN = 44-lead TQFP = 48-lead UQFN = 48-lead TQFP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16(L)F19185/86 - I/PT
Industrial temperature
TQFP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.