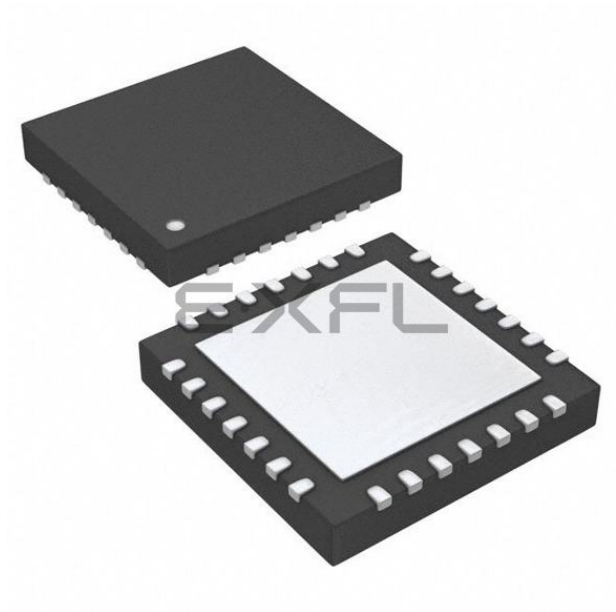

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19156-e-mv

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 60 (Continued)											
1E22h	CLC2GLS2	LC2G3D4T	LC1G3D4N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	xxxx xxxx	uuuu uuuu
1E23h	CLC2GLS3	LC2G4D4T	LC1G4D4N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	xxxx xxxx	uuuu uuuu
1E24h	CLC3CON	LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE<2:0>			0-00 0000	0-00 0000
1E25h	CLC3POL	LC3POL	—	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	0--- xxxx	0--- uuuu
1E26h	CLC3SEL0	—	—	LC3D1S						xxxx xxxx	uuuu uuuu
1E27h	CLC3SEL1	—	—	LC3D2S						xxxx xxxx	uuuu uuuu
1E28h	CLC3SEL2	—	—	LC3D3S						xxxx xxxx	uuuu uuuu
1E29h	CLC3SEL3	—	—	LC3D4S						xxxx xxxx	uuuu uuuu
1E2Ah	CLC3GLS0	LC3G1D4T	LC3G1D4N	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	xxxx xxxx	uuuu uuuu
1E2Bh	CLC3GLS1	LC3G2D4T	LC3G2D4N	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	xxxx xxxx	uuuu uuuu
1E2Ch	CLC3GLS2	LC3G3D4T	LC3G3D4N	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	xxxx xxxx	uuuu uuuu
1E2Dh	CLC3GLS3	LC3G4D4T	LC3G4D4N	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	xxxx xxxx	uuuu uuuu
1E2Eh	CLC4CON	LC4EN	—	LC4OUT	LC4INTP	LC4INTN	LC4MODE<2:0>			0-00 0000	0-00 0000
1E2Fh	CLC4POL	LC4POL	—	—	—	LC4G4POL	LC4G3POL	LC4G2POL	LC4G1POL	0--- xxxx	0--- uuuu
1E30h	CLC4SEL0	—	—	LC4D1S<5:0>						xxxx xxxx	uuuu uuuu
1E31h	CLC4SEL1	—	—	LC4D2S<5:0>						--xx xxxx	uuuu uuuu
1E32h	CLC4SEL2	—	—	LC4D3S<5:0>						xxxx xxxx	uuuu uuuu
1E33h	CLC4SEL3	—	—	LC4D4S<5:0>						xxxx xxxx	uuuu uuuu
1E34h	CLC4GLS0	LC4G1D4T	LC4G1D4N	LC4G1D3T	LC4G1D3N	LC4G1D2T	LC4G1D2N	LC4G1D1T	LC4G1D1N	xxxx xxxx	uuuu uuuu
1E35h	CLC4GLS1	LC4G2D4T	LC4G2D4N	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	xxxx xxxx	uuuu uuuu
1E36h	CLC4GLS2	LC4G3D4T	LC4G3D4N	LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

REGISTER 10-12: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **OSFIF**: Oscillator Fail-Safe Interrupt Flag bit
1 = Oscillator fail-safe interrupt has occurred (must be cleared in software)
0 = No oscillator fail-safe interrupt

bit 6 **CSWIF:** Clock Switch Complete Interrupt Flag bit
1 = The clock switch module indicates an interrupt condition and is ready to complete the clock switch operation (must be cleared in software)
0 = The clock switch does not indicate an interrupt condition

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **ADTIF:** Analog-to-Digital Converter (ADC) Threshold Compare Interrupt Flag bit
1 = An A/D measurement was beyond the configured threshold (must be cleared in software)
0 = A/D measurements have been within the configured threshold

bit 0 **ADIF**: Analog-to-Digital Converter (ADC) Interrupt Flag bit
1 = An A/D conversion or complex operation has completed (must be cleared in software)
0 = An A/D conversion or complex operation is not complete

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	165
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	166
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	167
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	168
PIE4	—	—	—	—	TMR4IE	—	TMR2IE	TMR1IE	169
PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	170
PIE6	CRIE	—	—	—	—	—	CCP2IE	CCP1IE	171
PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	172
PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	174
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	176
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	177
PIR4	—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF	178
PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	179
PIR6	CRIF	—	—	—	—	—	CCP2IF	CCP1IF	180
PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	181
PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

11.2.3.2 Peripheral Usage in Sleep

Some peripherals that can operate in Sleep mode will not operate properly with the Low-Power Sleep mode selected. The Low-Power Sleep mode is intended for use with these peripherals:

- Brown-out Reset (BOR)
- Windowed Watchdog Timer (WWDT)
- External interrupt pin/interrupt-on-change pins
- Timer1 (with external clock source)

It is the responsibility of the end user to determine what is acceptable for their application when setting the VREGPM settings in order to ensure operation in Sleep.

Note:	The PIC16LF19155/56/75/76/85/86 does not have a configurable Low-Power Sleep mode. PIC16LF19155/56/75/76/85/86 is an unregulated device and is always in the lowest power state when in Sleep, with no wake-up time penalty. This device has a lower maximum V_{DD} and I/O voltage than the PIC16F19155/56/75/76/85/86. See **Section 39.0 "Electrical Specifications"** for more information.

11.3 IDLE Mode

When the Idle Enable (IDLEN) bit is clear (IDLEN = 0), the SLEEP instruction will put the device into full Sleep mode (see **Section 11.2 "Sleep Mode"**). When IDLEN is set (IDLEN = 1), the SLEEP instruction will put the device into IDLE mode. In IDLE mode, the CPU and memory operations are halted, but the peripheral clocks continue to run. This mode is similar to DOZE mode, except that in IDLE both the CPU and PFM are shut off.

Note:	Peripherals using FOSC will continue running while in Idle (but not in Sleep). Peripherals using HFINTOSC, LFINTOSC, or SOSC will continue running in both Idle and Sleep.

Note:	If CLKOUT is enabled (CLKOUT = 0, Configuration Word 1), the output will continue operating while in Idle.

11.3.0.1 Idle and Interrupts

IDLE mode ends when an interrupt occurs (even if GIE = 0), but IDLEN is not changed. The device can re-enter IDLE by executing the SLEEP instruction.

If Recover-on-Interrupt is enabled (ROI = 1), the interrupt that brings the device out of Idle also restores full-speed CPU execution when doze is also enabled.

11.3.0.2 Idle and WWDT

When in IDLE, the WWDT Reset is blocked and will instead wake the device. The WWDT wake-up is not an interrupt, therefore ROI does not apply.

Note:	The WWDT can bring the device out of IDLE, in the same way it brings the device out of Sleep. The DOZEN bit is not affected.

15.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I^2C)

Note:	The I^2C SCLx and SDAx functions can be remapped through PPS. However, only the RB1, RB2, RC3 and RC4 pins have the I^2C and SMBus specific input buffers implemented (I^2C mode disables INLVL and sets thresholds that are specific for I^2C). If the SCLx or SDAx functions are mapped to some other pin (other than RB1, RB2, RC3 or RC4), the general purpose TTL or ST input buffers (as configured based on INLVL register setting) will be used instead. In most applications, it is therefore recommended only to map the SCLx and SDAx pin functions to the RB1, RB2, RC3 or RC4 pins.

15.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 15-1.

EXAMPLE 15-1: PPS LOCK/UNLOCK SEQUENCE

```
; suspend interrupts
    BCF     INTCON,GIE
;   BANKSEL PPSLOCK     ; set bank
; required sequence, next 5 instructions
    MOVLW   0x55
    MOVWF   PPSLOCK
    MOVLW   0xAA
    MOVWF   PPSLOCK
; Set PPSLOCKED bit to disable writes or
; Clear PPSLOCKED bit to enable writes
    BSF     PPSLOCK,PPSLOCKED
; restore interrupts
    BSF     INTCON,GIE
```

15.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

15.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

15.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values (Permanent Lock Removed). All other Resets leave the selections unchanged. Default input selections are shown in Table 15-1 and Table 15-2.

REGISTER 19-4: ADCON3: ADC CONTROL REGISTER 3

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0	R/W-0/0	R/W-0/0	R/W-0/0
—	CALC<2:0>			SOI	TMD<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **CALC<2:0>:** ADC Error Calculation Mode Select bits

CALC	DSEN = 0 Single-Sample Mode	DSEN = 1 CVD Double-Sample Mode(1)	Application
111	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
101	FLTR-STPT	FLTR-STPT	Average/filtered value vs. setpoint
100	PREV-FLTR	PREV-FLTR	First derivative of filtered value(3) (negative)
011	Reserved	Reserved	Reserved
010	RES-FLTR	(RES-PREV)-FLTR	Actual result vs. averaged/filtered value
001	RES-STPT	(RES-PREV)-STPT	Actual result vs.setpoint
000	RES-PREV	RES-PREV	First derivative of single measurement(2)
			Actual CVD result in CVD mode(2)

bit 3 **SOI:** ADC Stop-on-Interrupt bit

If CONT = 1:
1 = GO is cleared when the threshold conditions are met, otherwise the conversion is retriggered
0 = GO is not cleared by hardware, must be cleared by software to stop retriggers

bit 2-0 **TMD<2:0>:** Threshold Interrupt Mode Select bits

111 = Interrupt regardless of threshold test results
110 = Interrupt if ERR>UTH
101 = Interrupt if ERR≤UTH
100 = Interrupt if ERR<LTH or ERR>UTH
011 = Interrupt if ERR>LTH and ERR<UTH
010 = Interrupt if ERR≥LTH
001 = Interrupt if ERR<LTH
000 = Never interrupt

Note 1: When PSIS = 0, the value of (RES-PREV) is the value of (S2-S1) from Table 19-2.
2: When ADPSIS = 0.
3: When ADPSIS = 1.

REGISTER 19-36: ADCP: ADC CHARGE PUMP CONTROL REGISTER

R/W-0/0	U-0	U-0	U-0	U-0	U-0	U-0	R-0/0
CPON	—	—	—	—	—	—	CPRDY
bit 7							bit 0

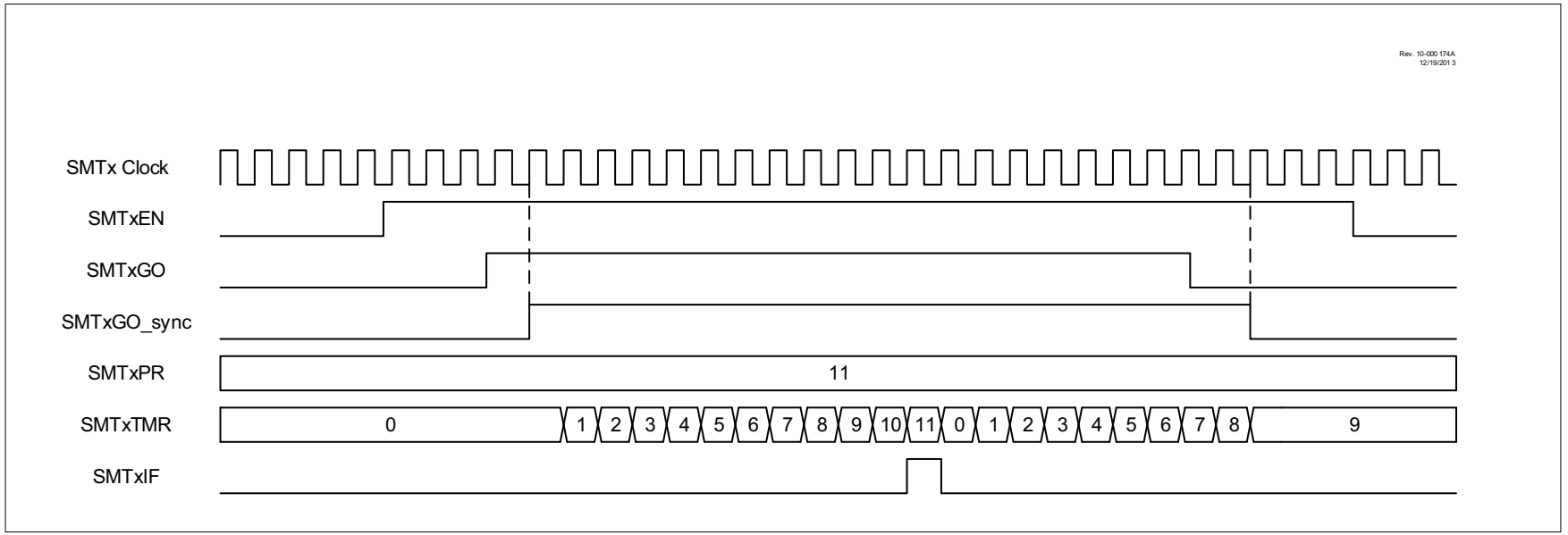
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS= Hardware set

bit 7 **CPON**: Charge Pump On Control bit
1 = Charge Pump On when requested by the ADC
0 = Charge Pump Off

bit 6-1 **Unimplemented:** Read as ‘0’

bit 0 CPRDY: Charge Pump Ready Status bit
1 = Charge Pump is ready
0 = Charge Pump is not ready (or never started)

FIGURE 28-3: TIMER MODE TIMING DIAGRAM



REGISTER 32-6: CLCxSEL3: GENERIC CLCx DATA 3 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LCxD4S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **LCxD4S<5:0>:** CLCx Data 4 Input Selection bits
See Table 32-2.

33.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit of the SSPxCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

33.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 33-7 shows the block diagram of a typical daisy-chain connection when operating in SPI mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPxCON3 register will enable writes to the SSPxBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

33.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission.

The $\overline{SS}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{SS}$ pin control enabled (SSPxCON1<3:0> = 0100).

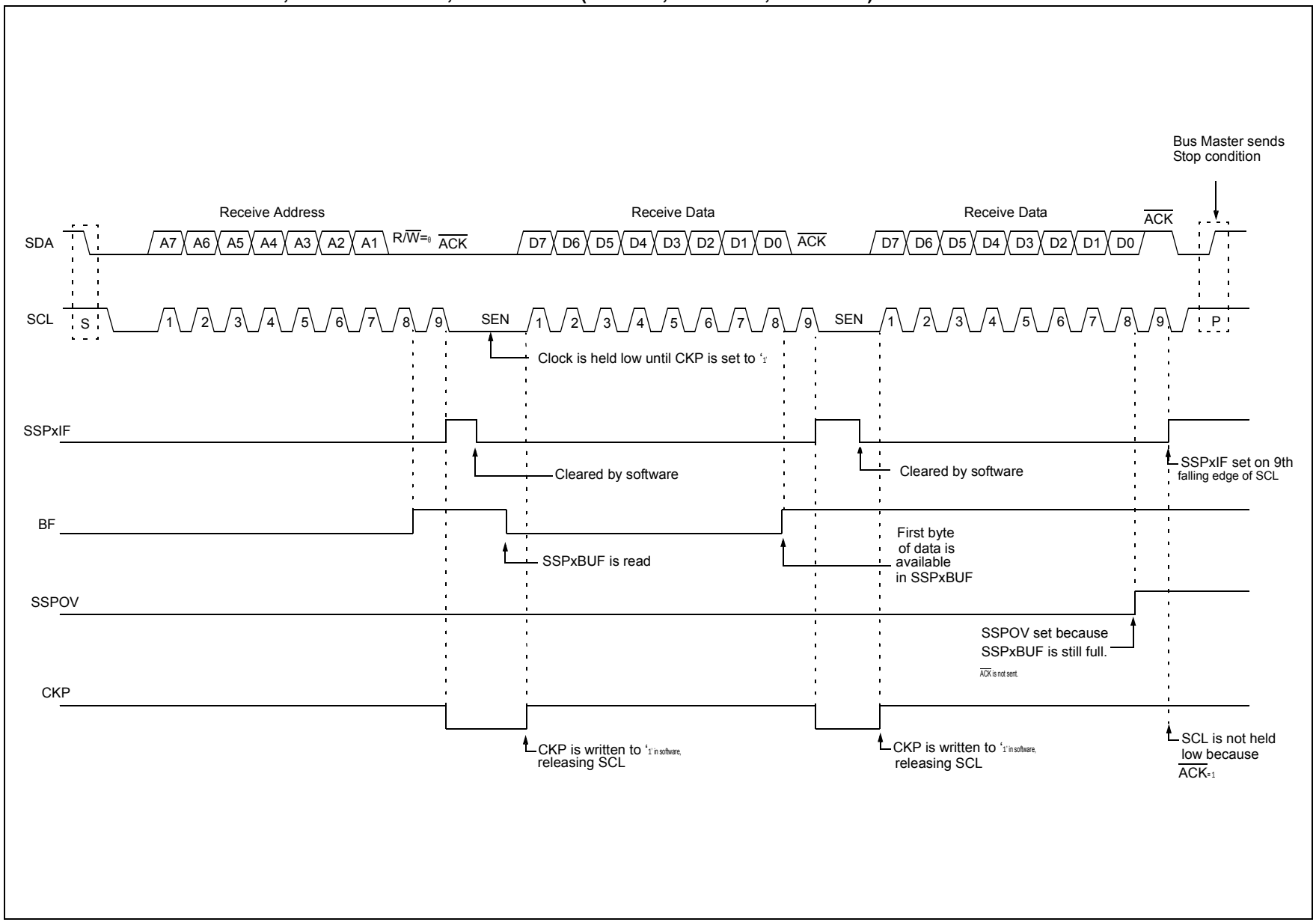
When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven.

When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1:	When the SPI is in Slave mode with $\overline{SS}$ pin control enabled (SSPxCON1<3:0> = 0100), the SPI module will reset if the $\overline{SS}$ pin is set to VDD.
2:	When the SPI is used in Slave mode with CKE set; the user must enable $\overline{SS}$ pin control.
3:	While operated in SPI Slave mode the SMP bit of the SSPxSTAT register must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit.

FIGURE 33-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



34.4.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 34.4.1.5 "Synchronous Master Reception"**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCxREG register. If the RXxIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

34.4.2.4 Synchronous Slave Reception Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for both the CK and DT pins (if applicable).
3. If interrupts are desired, set the RXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
4. If 9-bit reception is desired, set the RX9 bit.
5. Set the CREN bit to enable reception.
6. The RXxIF bit will be set when reception is complete. An interrupt will be generated if the RXxIE bit was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCxSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCxREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

34.5 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

34.5.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCxSTA and TXxSTA Control registers must be configured for Synchronous Slave Reception (see **Section 34.4.2.4 "Synchronous Slave Reception Set-up:"**).
- If interrupts are desired, set the RXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
- The RXxIF interrupt flag must be cleared by reading RCxREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RXxIF interrupt flag bit of the PIR3 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

34.5.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- The RCxSTA and TXxSTA Control registers must be configured for synchronous slave transmission (see **Section 34.4.2.2 "Synchronous Slave Transmission Set-up:"**).
- The TXxIF interrupt flag must be cleared by writing the output data to the TXxREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXxIE bit of the PIE3 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXxIE of the PIE3 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXxREG will transfer to the TSR and the TXxIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXxREG is available to accept another character for transmission, which will clear the TXxIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

TABLE 35-5: LCDDATAX REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS (48-PIN)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDDATA0	SEG7 COM0	SEG6 COM0	—	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	—	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0
LCDDATA2	SEG23 COM0	SEG22 COM0	—	SEG20 COM0	SEG19 COM0	SEG18 COM0	—	—
LCDDATA3	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
LCDDATA4	—	—	—	—	—	SEG34 COM0	SEG33 COM0	SEG32 COM0
LCDDATA5	SEG47 COM0	SEG46 COM0	SEG45 COM0	SEG44 COM0	SEG43 COM0	SEG42 COM0	SEG41 COM0	SEG40 COM0
LCDDATA6	SEG7 COM1	SEG6 COM1	—	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1
LCDDATA7	SEG15 COM1	SEG14 COM1	SEG13 COM1	—	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1
LCDDATA8	SEG23 COM1	SEG22 COM1	—	SEG20 COM1	SEG19 COM1	SEG18 COM1	—	—
LCDDATA9	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
LCDDATA10	—	—	—	—	—	SEG34 COM1	SEG33 COM1	SEG32 COM1
LCDDATA11	SEG47 COM1	SEG46 COM1	SEG45 COM1	SEG44 COM1	SEG43 COM1	SEG42 COM1	SEG41 COM1	SEG40 COM1
LCDDATA12	SEG7 COM2	SEG6 COM2	—	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2
LCDDATA13	SEG15 COM2	SEG14 COM2	SEG13 COM2	—	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2
LCDDATA14	SEG23 COM2	SEG22 COM2	—	SEG20 COM2	SEG19 COM2	SEG18 COM2	—	—
LCDDATA15	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
LCDDATA16	—	—	—	—	—	SEG34 COM2	SEG33 COM2	SEG32 COM2
LCDDATA17	SEG47 COM2	SEG46 COM2	SEG45 COM2	SEG44 COM2	SEG43 COM2	SEG42 COM2	SEG41 COM2	SEG40 COM2
LCDDATA18	SEG7 COM3	SEG6 COM3	—	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3
LCDDATA19	SEG15 COM3	SEG14 COM3	SEG13 COM3	—	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3
LCDDATA20	SEG23 COM3	SEG22 COM3	—	SEG20 COM3	SEG19 COM3	SEG18 COM3	—	—
LCDDATA21	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3
LCDDATA22	—	—	—	—	—	SEG34 COM3	SEG33 COM3	SEG32 COM3
LCDDATA23	SEG47 COM3	SEG46 COM3	SEG45 COM3	SEG44 COM3	SEG43 COM3	SEG42 COM3	SEG41 COM3	SEG40 COM3
LCDDATA24	SEG7 COM4	SEG6 COM4	—	SEG4 COM4	SEG3 COM4	SEG2 COM4	SEG1 COM4	SEG0 COM4
LCDDATA25	SEG15 COM4	SEG14 COM4	SEG13 COM4	—	SEG11 COM4	SEG10 COM4	SEG9 COM4	SEG8 COM4
LCDDATA26	SEG23 COM4	SEG22 COM4	—	SEG20 COM4	SEG19 COM4	SEG18 COM4	—	—
LCDDATA27	SEG31 COM4	SEG30 COM4	SEG29 COM4	SEG28 COM4	SEG27 COM4	SEG26 COM4	SEG25 COM4	SEG24 COM4
LCDDATA28	—	—	—	—	—	SEG34 COM4	SEG33 COM4	SEG32 COM4
LCDDATA29	SEG47 COM4	SEG46 COM4	SEG45 COM4	SEG44 COM4	SEG43 COM4	SEG42 COM4	SEG41 COM4	SEG40 COM4
LCDDATA30	SEG7 COM5	SEG6 COM5	—	SEG4 COM5	SEG3 COM5	SEG2 COM5	SEG1 COM5	SEG0 COM5
LCDDATA31	SEG15 COM5	SEG14 COM5	SEG13 COM5	—	SEG11 COM5	SEG10 COM5	SEG9 COM5	SEG8 COM5
LCDDATA32	SEG23 COM5	SEG22 COM5	—	SEG20 COM5	SEG19 COM5	SEG18 COM5	—	—
LCDDATA33	SEG31 COM5	SEG30 COM5	SEG29 COM5	SEG28 COM5	SEG27 COM5	SEG26 COM5	SEG25 COM5	SEG24 COM5
LCDDATA34	—	—	—	—	—	SEG34 COM5	SEG33 COM5	SEG32 COM5
LCDDATA35	SEG47 COM5	SEG46 COM5	SEG45 COM5	SEG44 COM5	SEG43 COM5	SEG42 COM5	SEG41 COM5	SEG40 COM5
LCDDATA36	SEG7 COM6	SEG6 COM6	—	SEG4 COM6	SEG3 COM6	SEG2 COM6	SEG1 COM6	SEG0 COM6
LCDDATA37	SEG15 COM6	SEG14 COM6	SEG13 COM6	—	SEG11 COM6	SEG10 COM6	SEG9 COM6	SEG8 COM6
LCDDATA38	SEG23 COM6	SEG22 COM6	—	SEG20 COM6	SEG19 COM6	SEG18 COM6	—	—
LCDDATA39	SEG31 COM6	SEG30 COM6	SEG29 COM6	SEG28 COM6	SEG27 COM6	SEG26 COM6	SEG25 COM6	SEG24 COM6
LCDDATA40	—	—	—	—	—	SEG34 COM6	SEG33 COM6	SEG32 COM6
LCDDATA41	SEG47 COM6	SEG46 COM6	SEG45 COM6	SEG44 COM6	SEG43 COM6	SEG42 COM6	SEG41 COM6	SEG40 COM6
LCDDATA42	SEG7 COM7	SEG6 COM7	—	SEG4 COM7	SEG3 COM7	SEG2 COM7	SEG1 COM7	SEG0 COM7
LCDDATA43	SEG15 COM7	SEG14 COM7	SEG13 COM7	—	SEG11 COM7	SEG10 COM7	SEG9 COM7	SEG8 COM7
LCDDATA44	SEG23 COM7	SEG22 COM7	—	SEG20 COM7	SEG19 COM7	SEG18 COM7	—	—
LCDDATA45	SEG31 COM7	SEG30 COM7	SEG29 COM7	SEG28 COM7	SEG27 COM7	SEG26 COM7	SEG25 COM7	SEG24 COM7
LCDDATA46	—	—	—	—	—	SEG34 COM7	SEG33 COM7	SEG32 COM7
LCDDATA47	SEG47 COM7	SEG46 COM7	SEG45 COM7	SEG44 COM7	SEG43 COM7	SEG42 COM7	SEG41 COM7	SEG40 COM7

TABLE 39-4: I/O PORTS

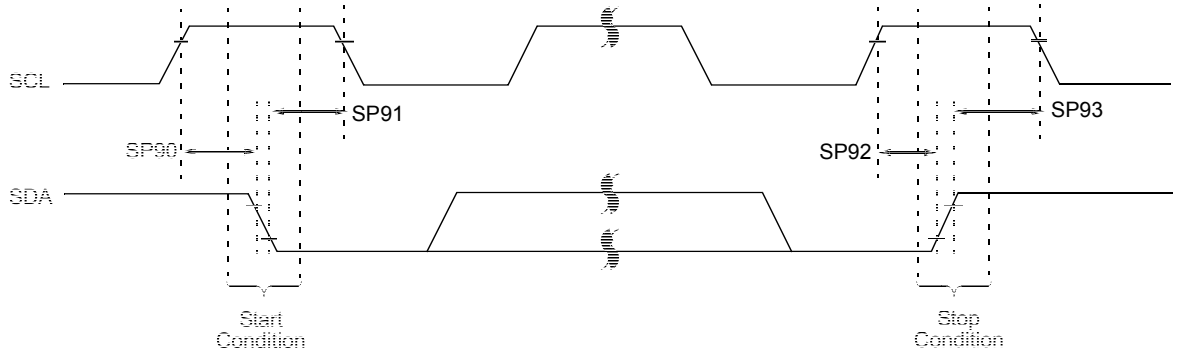
Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**					
		I/O PORT:					
D300		with TTL buffer	—	—	0.8	V	$4.5V \le V_{DD} \le 5.5V$
D301			—	—	0.15 V_{DD}	V	$1.8V \le V_{DD} \le 4.5V$
D302		with Schmitt Trigger buffer	—	—	0.2 V_{DD}	V	$2.0V \le V_{DD} \le 5.5V$
D303		with I^2C levels	—	—	0.3 V_{DD}	V	
D304		with SMBus levels	—	—	0.8	V	$2.7V \le V_{DD} \le 5.5V$
D305		$\overline{MCLR}$	—	—	0.2 V_{DD}	V	
	V_{IH}	**Input High Voltage**					
		I/O PORT:					
D320		with TTL buffer	2.0	—	—	V	$4.5V \le V_{DD} \le 5.5V$
D321			0.25 V_{DD} + 0.8	—	—	V	$1.8V \le V_{DD} \le 4.5V$
D322		with Schmitt Trigger buffer	0.8 V_{DD}	—	—	V	$2.0V \le V_{DD} \le 5.5V$
D323		with I^2C levels	0.7 V_{DD}	—	—	V	
D324		with SMBus levels	2.1	—	—	V	$2.7V \le V_{DD} \le 5.5V$
D325		$\overline{MCLR}$	0.7 V_{DD}	—	—	V	
	I_{IL}	**Input Leakage Current(1)**					
D340		I/O Ports	—	± 5	± 125	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C
D341			—	± 5	± 1000	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 125°C
D342		$\overline{MCLR}$(2)	—	± 50	± 200	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C
	I_{PUR}	**Weak Pull-up Current**					
D350			25	120	200	µA	V_{DD} = 3.0V, V_{PIN} = V_{SS}
	V_{OL}	**Output Low Voltage**					
D080		Standard I/O ports	—	—	0.6	V	I_{OL} = 8 mA, V_{DD} = 5.0V I_{OL} = 6 mA, V_{DD} = 3.3V I_{OL} = 1.8 mA, V_{DD} = 1.8V
D080A		High-Drive I/O Ports	— — —	— 0.6 0.6	0.6 — —	V V V	I_{OH} = 10 mA, V_{DD} = 2.3V, HIDCx = 1 I_{OH} = 32 mA, V_{DD} = 3.0V, HIDCx = 1 I_{OH} = 51 mA, V_{DD} = 5.0V, HIDCx = 1
D090	V_{OH}	**Output High Voltage**					
		Standard I/O Ports	V_{DD} - 0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5.0V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 1 mA, V_{DD} = 1.8V
D090A		High-Drive I/O Ports	V_{DD} - 0.7	— V_{DD} - 0.7 V_{DD} - 0.7	— — —	V V V	I_{OH} = 10 mA, V_{DD} = 2.3V, HIDCx = 1 I_{OH} = 37 mA, V_{DD} = 3.0V, HIDCx = 1 I_{OH} = 54 mA, V_{DD} = 5.0V, HIDCx = 1
D380	C_{IO}	**All I/O pins**	—	5	50	pF	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

FIGURE 39-21: I²C BUS START/STOP BITS TIMING



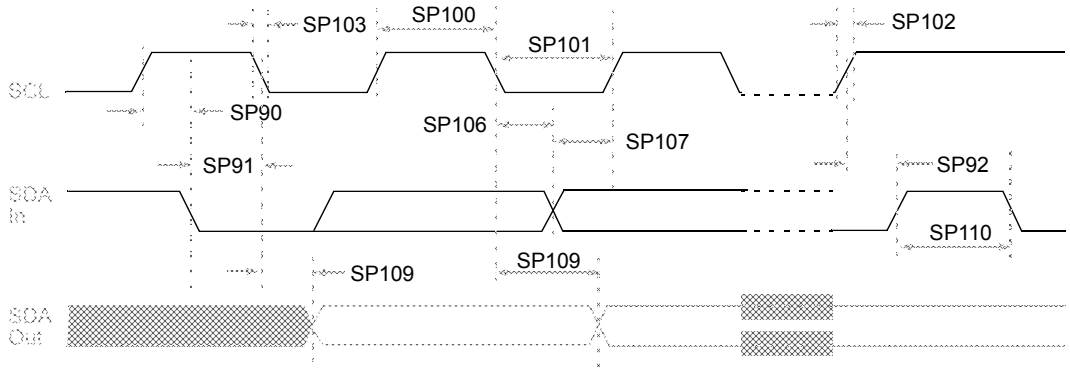
Note: Refer to Figure 39-4 for load conditions.

TABLE 39-25: I²C BUS START/STOP BITS REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
SP90*	TSU:STA	Start condition	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
		Setup time	400 kHz mode	600	—	—		
SP91*	THD:STA	Start condition	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
SP92*	TSU:STO	Stop condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
SP93	THD:STO	Stop condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

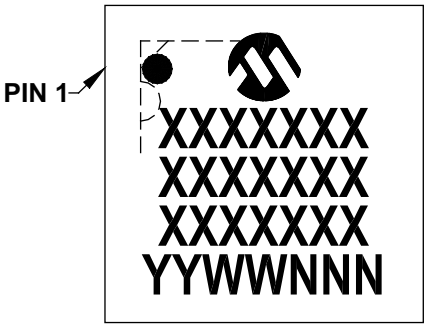
FIGURE 39-22: I²C BUS DATA TIMING



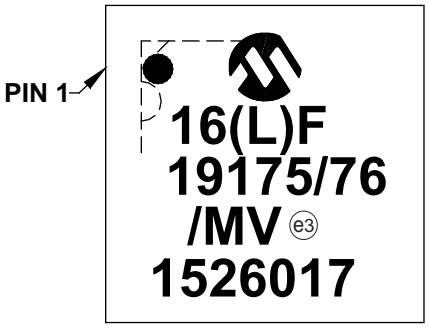
Note: Refer to Figure 39-4 for load conditions.

42.1 Package Marking Information (Continued)

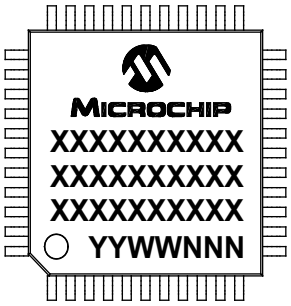
40-Lead UQFN (5x5x0.5 mm)



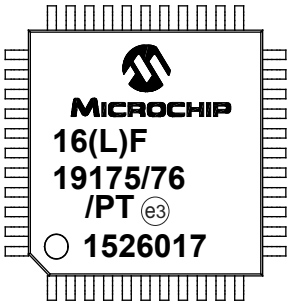
Example



44-Lead TQFP (10x10x1 mm)



Example



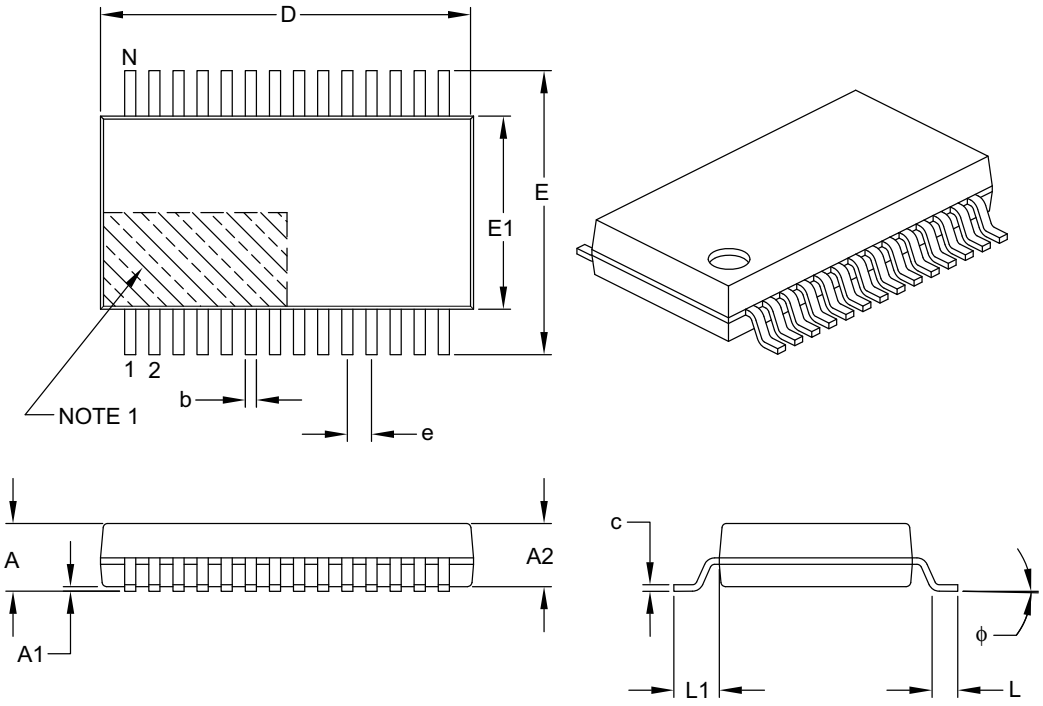
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

The following sections give the technical details of the packages.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

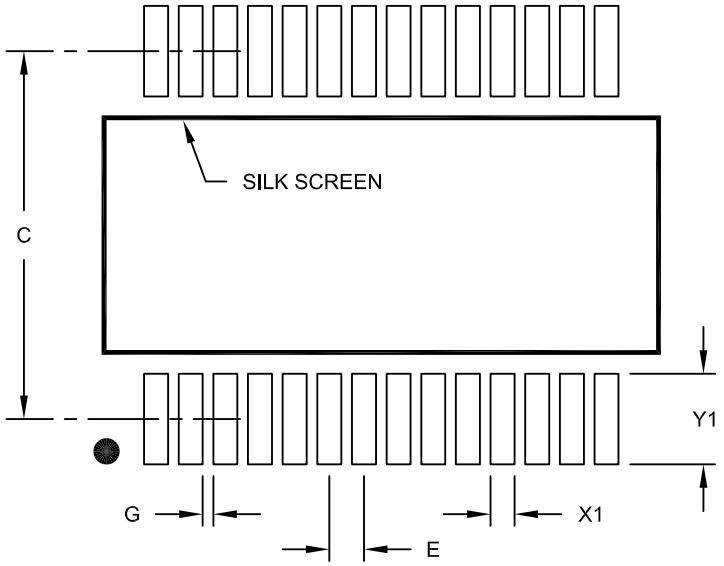
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

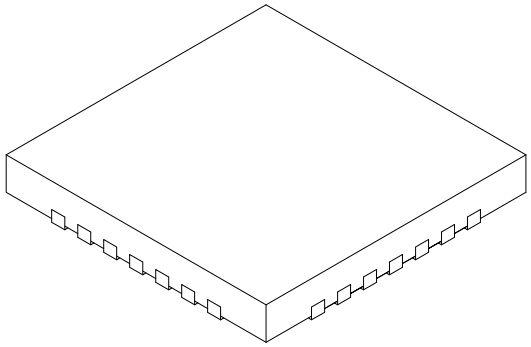
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2