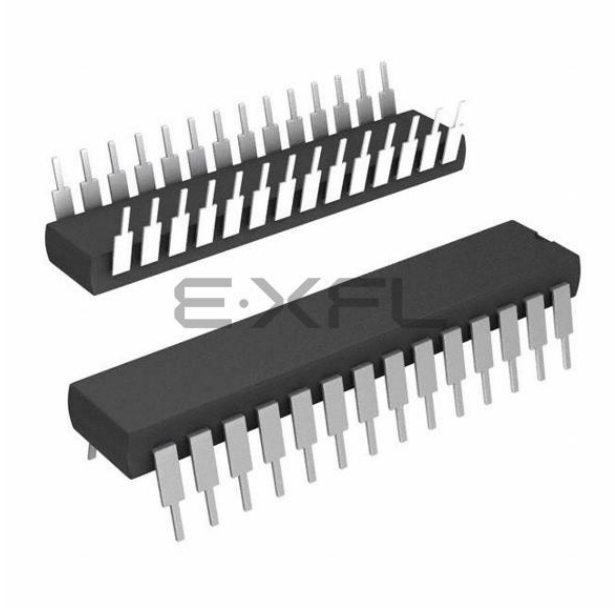


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19156-e-sp

1.0 DEVICE OVERVIEW

The PIC16(L)F19155/56/75/76/85/86 are described within this data sheet. The PIC16(L)F19155/56/75/76/85/86 devices are available in 48-pin TQFP and UQFN, 44-pin TQFP and UQFN, 40-pin PDIP and 28-pin SPDIP, SOIC, SSOP and UQFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F19155/56/75/76/85/86 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F19155/56/75/76/85/86
Analog-to-Digital Converter with Computation (ADC^2)		•
Digital-to-Analog Converter (DAC1)		•
Fixed Voltage Reference (FVR)		•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1 and EUSART2)		•
Temperature Indicator Module (TIM)		•
Zero-Cross Detect (ZCD1)		•
Real-Time Calendar and Clock (RTCC)		•
Liquid Crystal Display (LCD)		•
Capture/Compare/PWM Modules (CCP)		
	CCP1	•
	CCP2	•
Comparator Module (Cx)		
	C1	•
	C2	•
Configurable Logic Cell (CLC)		
	CLC1	•
	CLC2	•
	CLC3	•
	CLC4	•
Complementary Waveform Generator (CWG)		
	CWG1	•
Master Synchronous Serial Ports (MSSP)		
	MSSP1	•
Pulse-Width Modulator (PWM)		
	PWM3	•
	PWM4	•
Signal Measure Timer (SMT)		
	SMT1	•
Timers		
	Timer0	•
	Timer1	•
	Timer2	•
	Timer4	•

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 20											
CPU CORE REGISTERS; see Table 4-3 for specifics											
A0Ch	—	Unimplemented								---- ----	---- ----
A0Dh	—	Unimplemented								---- ----	---- ----
A0Eh	—	Unimplemented								---- ----	---- ----
A0Fh	—	Unimplemented								---- ----	---- ----
A10h	—	Unimplemented								---- ----	---- ----
A11h	—	Unimplemented								---- ----	---- ----
A12h	—	Unimplemented								---- ----	---- ----
A13h	—	Unimplemented								---- ----	---- ----
A14h	—	Unimplemented								---- ----	---- ----
A15h	—	Unimplemented								---- ----	---- ----
A16h	—	Unimplemented								---- ----	---- ----
A17h	—	Unimplemented								---- ----	---- ----
A18h	—	Unimplemented								---- ----	---- ----
A19h	RC2REG	RC2REG								0000 0000	0000 0000
A1Ah	TX2REG	TX2REG								0000 0000	0000 0000
A1Bh	SP2BRGL	SP2BRGL								0000 0000	0000 0000
A1Ch	SP2BRGH	SP2BRGH								0000 0000	0000 0000
A1Dh	RC2STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
A1Eh	TX2STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
A1Fh	BAUD2CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 63 (Continued)											
1FD0h	—	Unimplemented								---- ----	---- ----
1FD1h	—	Unimplemented								---- ----	---- ----
1FD2h	—	Unimplemented								---- ----	---- ----
1FD3h	—	Unimplemented								---- ----	---- ----
1FD4h	—	Unimplemented								---- ----	---- ----
1FD5h	—	Unimplemented								---- ----	---- ----
1FD6h	—	Unimplemented								---- ----	---- ----
1FD7h	—	Unimplemented								---- ----	---- ----
1FD8h	—	Unimplemented								---- ----	---- ----
1FD9h	—	Unimplemented								---- ----	---- ----
1FDAh	—	Unimplemented								---- ----	---- ----
1FDBh	—	Unimplemented								---- ----	---- ----
1FDCh	—	Unimplemented								---- ----	---- ----
1FDDh	—	Unimplemented								---- ----	---- ----
1FDEh	—	Unimplemented								---- ----	---- ----
1FDFh	—	Unimplemented								---- ----	---- ----
1FE0h	—	Unimplemented								---- ----	---- ----
1FE1h	—	Unimplemented								---- ----	---- ----
1FE2h	—	Unimplemented								---- ----	---- ----
1FE3h	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

8.15 Power Control (PCON) Registers

The Power Control (PCON) registers contain flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Reset Instruction Reset ($\overline{RI}$)
- $\overline{MCLR}$ Reset ($\overline{RMCLR}$)
- Watchdog Timer Reset ($\overline{RWDT}$)
- Watchdog Timer Window Violation Reset ($\overline{WDTWV}$)
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)
- Memory Violation Reset ($\overline{MEMV}$)
- V_{BAT} Reset ($\overline{VBATBOR}$)

The PCON0 register bits are shown in Register 8-2.

The PCON1 register bits are shown in Register 8-3.

Hardware will change the corresponding register bit during the Reset process; if the Reset was not caused by the condition, the bit remains unchanged (Table 8-4).

Software should reset the bit to the inactive state after the restart (hardware will not reset the bit).

Software may also set any PCON bit to the active state, so that user code may be tested, but no reset action will be generated.

All bits in PCON1 and PCON0 will maintain their state when either V_{DD} or V_{BAT} is powered.

REGISTER 10-11: PIR0: PERIPHERAL INTERRUPT STATUS REGISTER 0

U-0	U-0	R/W/HS-0/0	R-0	U-0	U-0	U-0	R/W/HS-0/0
—	—	TMR0IF	IOCIF	—	—	—	INTF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS= Hardware Set

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
- 1 = Timer0 register has overflowed (must be cleared in software)
- 0 = Timer0 register did not overflow

bit 4 **IOCIF:** Interrupt-on-Change Interrupt Flag bit (read-only)(2)
- 1 = One or more of the IOCAF-IOCEF register bits are currently set, indicating an enabled edge was detected by the IOC module.
- 0 = None of the IOCAF-IOCEF register bits are currently set

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **INTF:** INT External Interrupt Flag bit(1)
- 1 = The INT external interrupt occurred (must be cleared in software)
- 0 = The INT external interrupt did not occur

Note 1: The External Interrupt GPIO pin is selected by INTPPS (Register 15-1).

2: The IOCIF bit is the logical OR of all the IOCAF-IOCEF flags. Therefore, to clear the IOCIF flag, application firmware must clear all of the lower level IOCAF-IOCEF register bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-13: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	R/W/HS-0/0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	ZCDIF	—	—	—	—	C2IF	C1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **Unimplemented**: Read as '0'

bit 6 **ZCDIF:** Zero-Cross Detect (ZCD1) Interrupt Flag bit
1 = An enabled rising and/or falling ZCD1 event has been detected (must be cleared in software)
0 = No ZCD1 event has occurred

bit 5-2 **Unimplemented**: Read as '0'

bit 1 **C2IF**: Comparator C2 Interrupt Flag bit
1 = Comparator 2 interrupt asserted (must be cleared in software)
0 = Comparator 2 interrupt not asserted

bit 0 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Comparator 1 interrupt asserted (must be cleared in software)
0 = Comparator 1 interrupt not asserted

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 14-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	222
TRISA	TRISA7	TRISA6	—(1)	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	222
LATA	LATA7	LATA6	—	LATA4	LATA3	LATA2	LATA1	LATA0	223
ANSELA	ANSA7	ANSA6	—	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	223
WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	224
ODCONA	ODCA7	ODCA6	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	224
SLRCONA	SLRA7	SLRA6	—	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0	225
INLVLA	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	225

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: Unimplemented, read as '1'.

REGISTER 14-11: LATB: PORTB DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **LATB<7:0>**: RB<7:0> Output Latch Value bits(1)

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

REGISTER 14-12: ANSELB: PORTB ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ANSB<7:0>**: Analog Select between Analog or Digital Function on pins RB<7:0>, respectively
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 14-39: SLRCONE: PORTE SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1
SLRE7	SLRE6	SLRE5	SLRE4	SLRE3	—	SLRE1	SLRE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **SLRE<7:3>:** PORTE Slew Rate Enable bits
For RE<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **SLRE<1:0>:** PORTE Slew Rate Enable bits
For RE<1:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 14-40: INLVLE: PORTE INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1
INLVLE7	INLVLE6	INLVLE5	INLVLE4	INLVLE3	—	INLVLE1	INLVLE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **INLVLE<7:3>:** PORTE Input Level Select bits
For RE<7:3> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **INLVLE<1:0>:** PORTE Input Level Select bits
For RE<1:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

REGISTER 19-20: ADRESH: ADC RESULT REGISTER HIGH, FM = 1

U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	ADRES<11:8>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **ADRES<11:8>**: ADC Sample Result bits. Upper four bits of 12-bit conversion result.

REGISTER 19-21: ADRESL: ADC RESULT REGISTER LOW, FM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADRES<7:0>**: ADC Result Register bits. Lower eight bits of 12-bit conversion result.

REGISTER 24-8: MINUTES(1): MINUTE VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINH<2:0>			MINL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINH<2:0>:** Binary Coded Decimal value of minutes '10' digit; valid values from 0 to 5

bit 3-0 **MINL<3:0>:** Binary Coded Decimal value of minutes '1' digit; valid values from 0 to 9

Note 1: Writes to the MINUTE registers are only allowed when RTCWREN = 1.

REGISTER 24-9: SECONDS(1): SECOND VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECH<2:0>			SECL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECH<2:0>:** Binary Coded Decimal value of seconds '10' digit; valid values from 0 to 5

bit 3-0 **SECL<3:0>:** Binary Coded Decimal value of seconds '1' digit; valid values from 0 to 9

Note 1: Writes to the SECOND registers are only allowed when RTCWREN = 1.

30.1 Standard PWM Mode

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the PWMx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- TMR2 register
- PR2 register
- PWMxCON registers
- PWMxDCH registers
- PWMxDCL registers

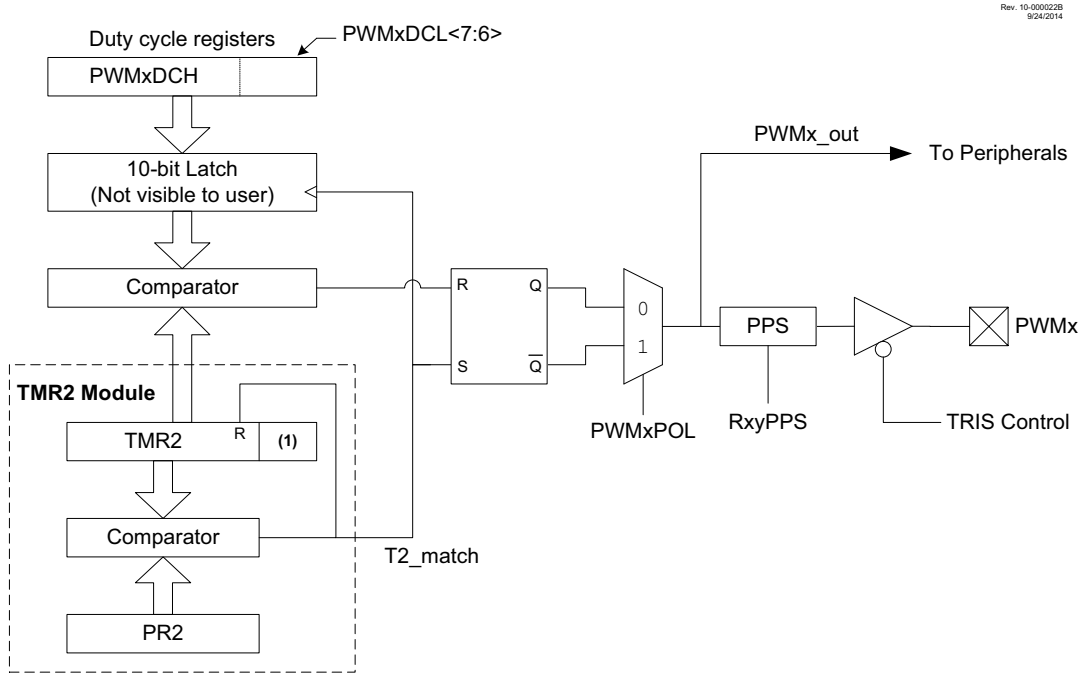
Figure 30-2 shows a simplified block diagram of PWM operation.

If PWMPOL = 0, the default state of the output is '0'. If PWMPOL = 1, the default state is '1'. If PWMEN = 0, the output will be the default state.

Note 1: The corresponding TRIS bit must be cleared to enable the PWM output on the PWMx pin.

2: Two identical Timer2 modules are implemented on this device. The timers are named Timer2 and Timer4. All references to Timer2 apply as well to Timer4. All references to T2PR apply as well to T4PR.

FIGURE 30-2: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time-base.

FIGURE 32-2: INPUT DATA SELECTION AND GATING

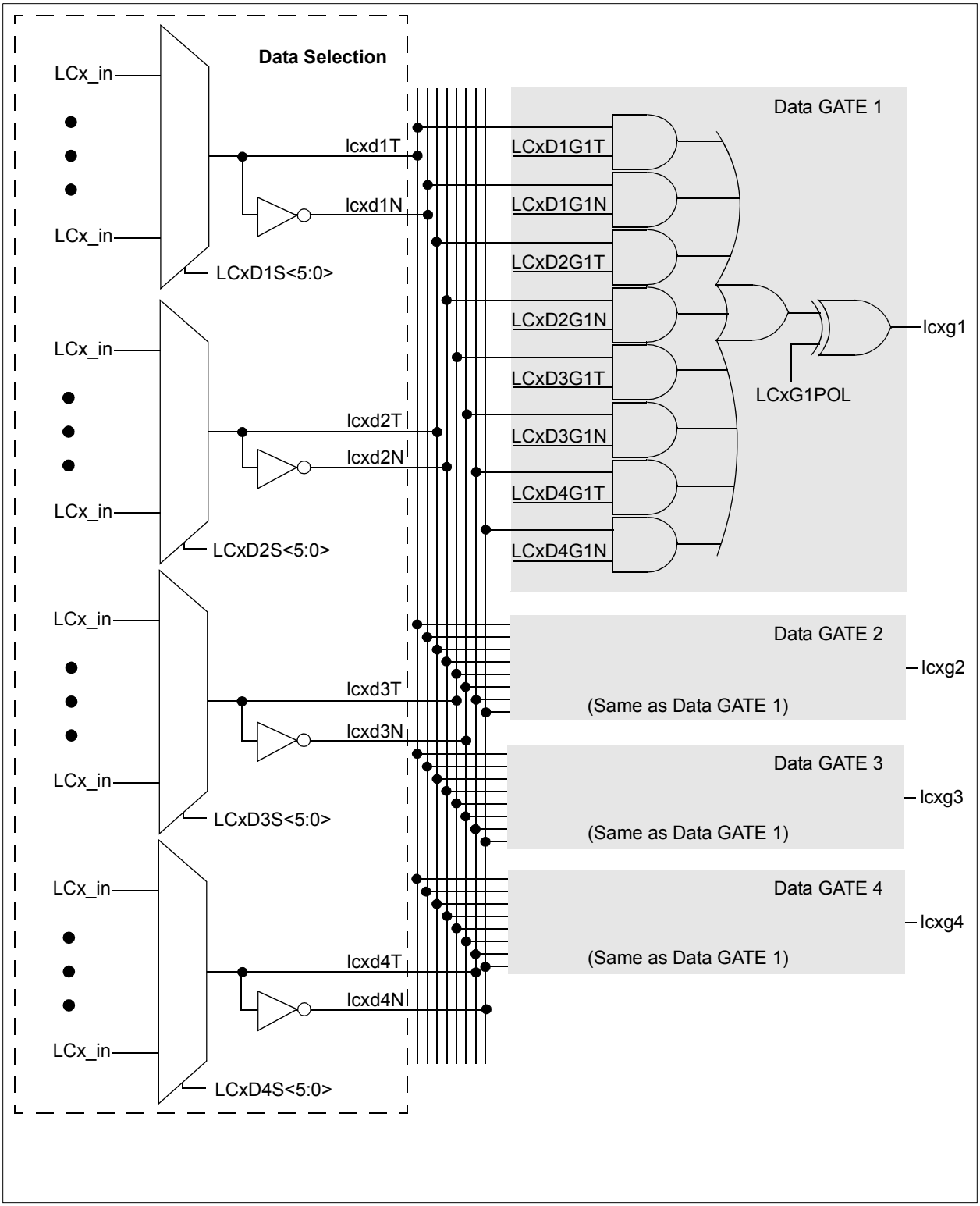


FIGURE 33-29: I^2C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)

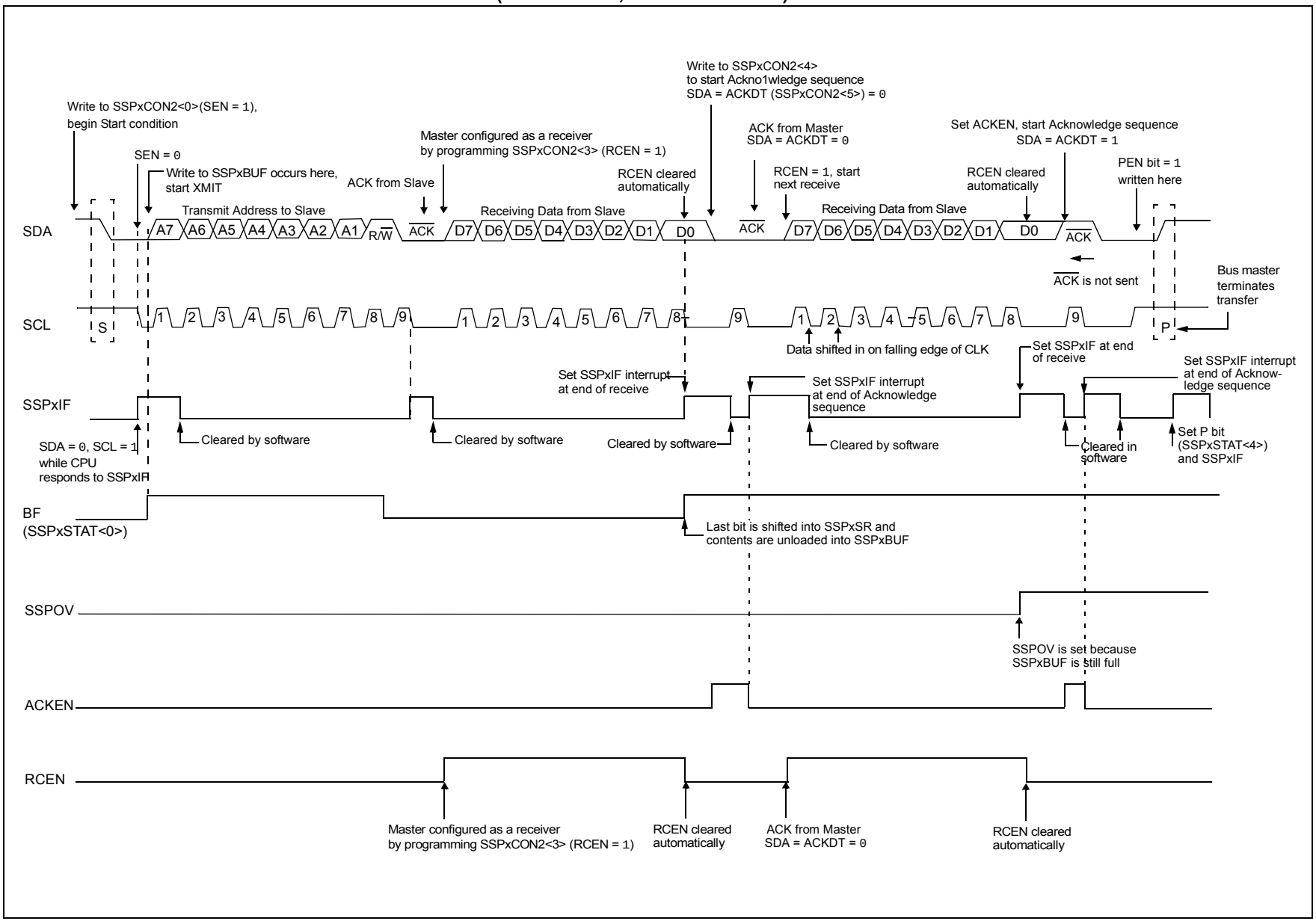


FIGURE 35-19: TYPE-B WAVEFORMS IN 1/8 MUX, 1/3 BIAS DRIVE

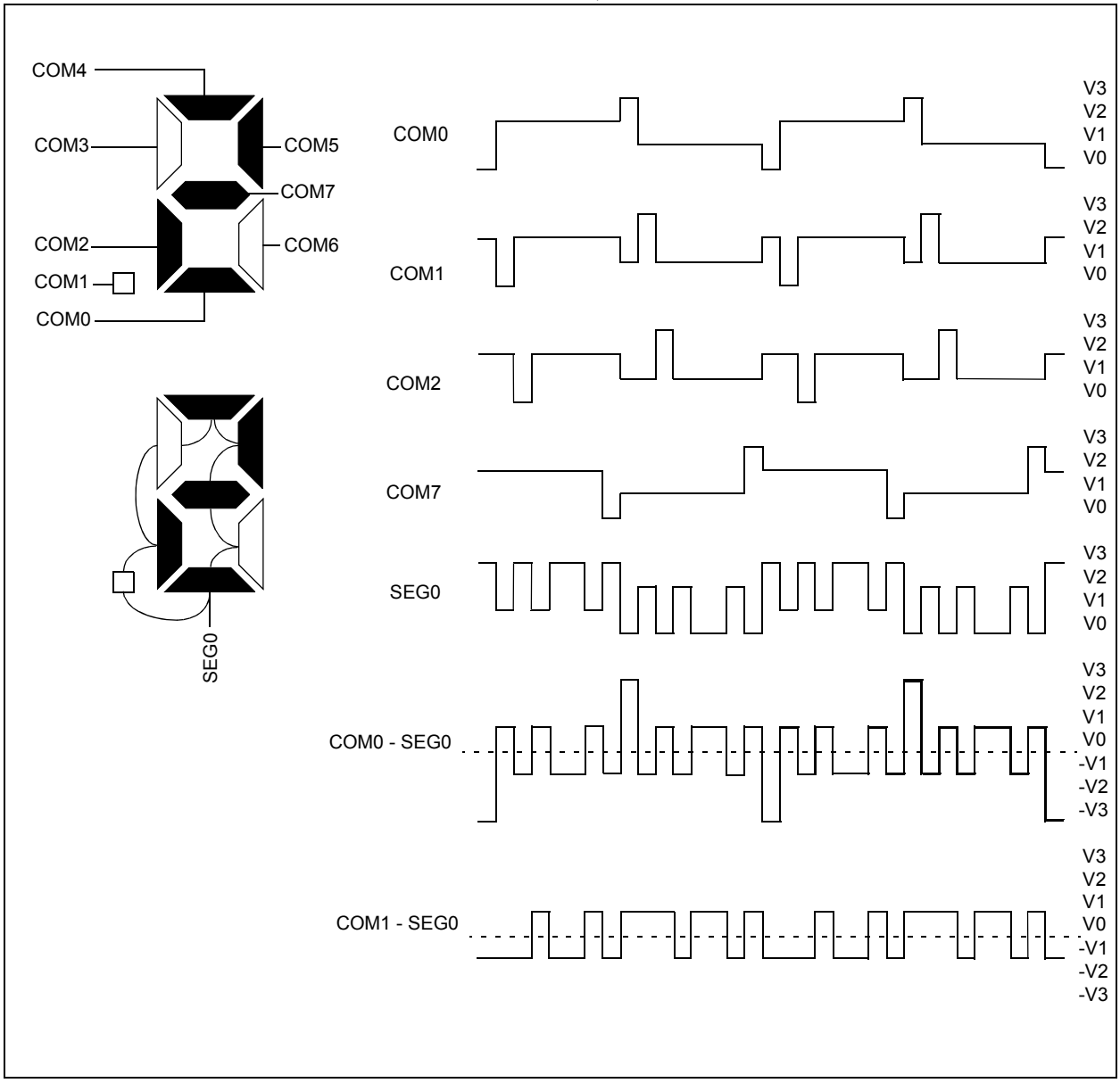


TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1E95h	—	Unimplemented								
1E96h	—	Unimplemented								
1E97h	—	Unimplemented								
1E98h	—	Unimplemented								
1E99h	—	Unimplemented								
1E9Ah	—	Unimplemented								
1E9Bh	—	Unimplemented								
1E9Ch	T2AINPPS	—	—	—	T2INPPS<4:0>					264
1E9Dh	T4AINPPS	—	—	—	T4INPPS<4:0>					264
1E9Eh	—	Unimplemented								
1E9Fh	—	Unimplemented								
1EA0h	—	Unimplemented								
1EA1h	CCP1PPS	—	—	—	CCP1PPS<4:0>					264
1EA2h	CCP2PPS	—	—	—	CCP2PPS<4:0>					264
1EA3h	—	Unimplemented								
1EA4h	—	Unimplemented								
1EA5h	—	Unimplemented								
1EA6h	—	Unimplemented								
1EA7h	—	Unimplemented								
1EA8h	—	Unimplemented								
1EA9h	SMT1WINPPS	—	—	—	SMT1WINPPS<4:0>					264
1EAAh	SMT1SIGPPS	—	—	—	SMT1SIGPPS<4:0>					264
1EABh	—	Unimplemented								
1EACh	—	Unimplemented								
1EADh	—	Unimplemented								
1EAEh	—	Unimplemented								
1EAFh	—	Unimplemented								
1EB0h	—	Unimplemented								
1EB1h	CWG1PPS	—	—	—	CWG1PPS<4:0>					264
1EB2h	—	Unimplemented								
1EB3h	—	Unimplemented								
1EB4h	—	Unimplemented								
1EB5h	—	Unimplemented								
1EB6h	—	Unimplemented								
1EB7h	—	Unimplemented								
1EB8h	—	Unimplemented								
1EB9h	—	Unimplemented								
1EBAh	—	Unimplemented								
1EBBh	CLCIN0PPS	—	—	—	CLCIN0PPS<4:0>					264
1EBCh	CLCIN1PPS	—	—	—	CLCIN1PPS<4:0>					264
1EBDh	CLCIN2PPS	—	—	—	CLCIN2PPS<4:0>					264

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1FD0h	—	Unimplemented								
1FD1h	—	Unimplemented								
1FD2h	—	Unimplemented								
1FD3h	—	Unimplemented								
1FD4h	—	Unimplemented								
1FD5h	—	Unimplemented								
1FD6h	—	Unimplemented								
1FD7h	—	Unimplemented								
1FD8h	—	Unimplemented								
1FD9h	—	Unimplemented								
1FDAh	—	Unimplemented								
1FDBh	—	Unimplemented								
1FDCh	—	Unimplemented								
1FDDh	—	Unimplemented								
1FDEh	—	Unimplemented								
1FDFh	—	Unimplemented								
1FE0h	—	Unimplemented								
1FE1h	—	Unimplemented								
1FE2h	—	Unimplemented								
1FE3h	—	Unimplemented								
1FE4h	STATUS_SHAD	—	—	—	—	—	Z_SHAD	DC_SHAD	C_SHAD	
1FE5h	WREG_SHAD	WREG_SHAD<7:0>								
1FE6h	BSR_SHAD	—	—	—	BSR_SHAD<4:0>					
1FE7h	PCLATH_SHAD	—	PCLATH_SHAD<6:0>							
1FE8h	FSR0L_SHAD	FSR0L_SHAD<7:0>								
1FE9h	FSR0H_SHAD	FSR0H_SHAD<7:0>								
1FEAh	FSR1L_SHAD	FSR1L_SHAD<7:0>								
1FEBh	FSR1H_SHAD	FSR1H_SHAD<7:0>								
1FECh	—	Unimplemented								
1FEDh	STKPTR	—	—	—	STKPTR<4:0>					
1FEEh	TOSL	TOSL<7:0>								
1FEFh	TOSH	—	TOSH<6:0>							

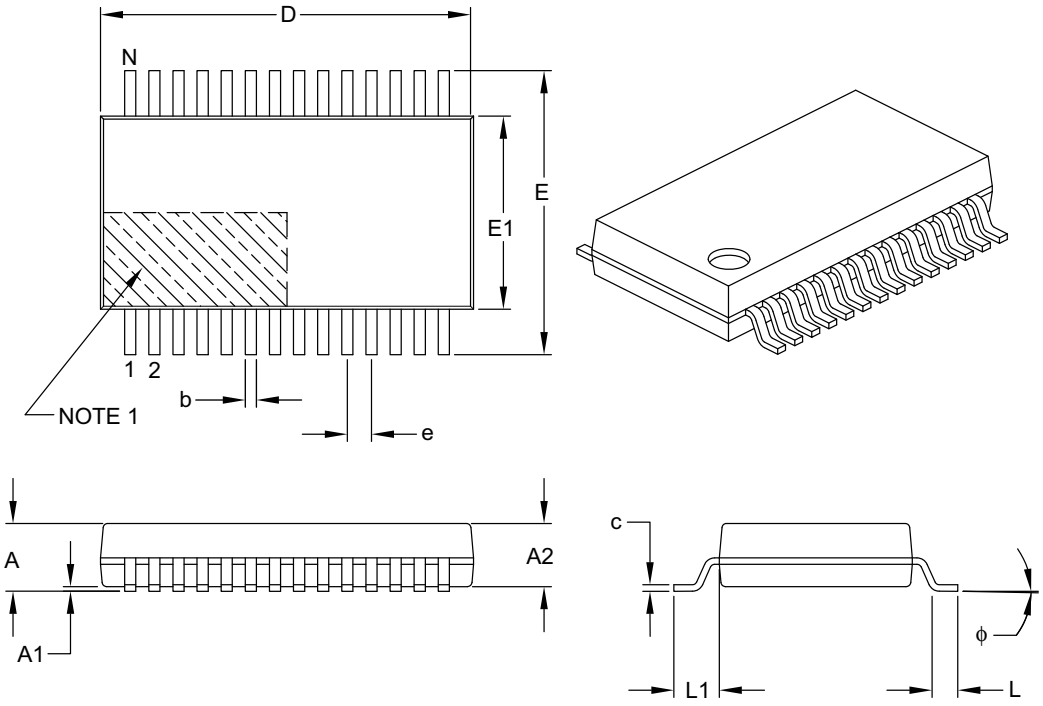
Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

The following sections give the technical details of the packages.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

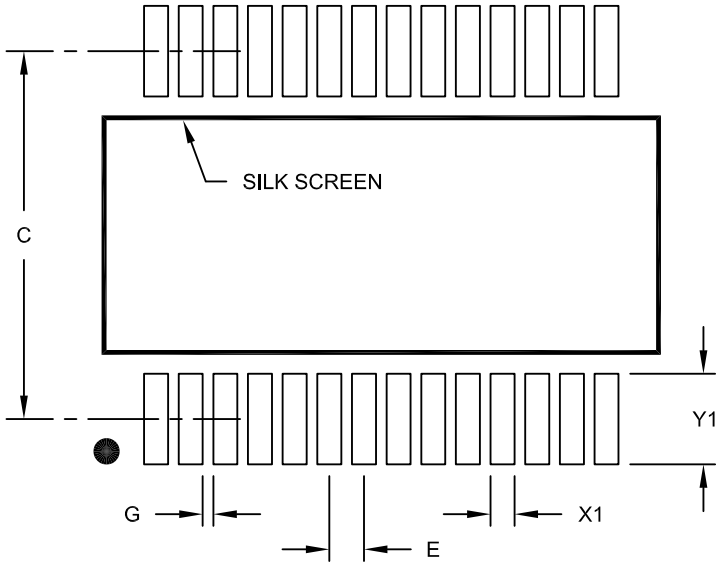
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

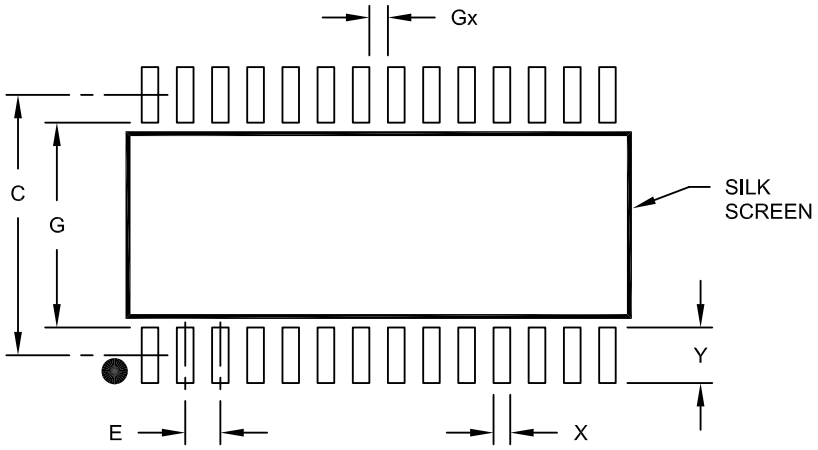
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A