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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19156-e-ss

1.0 DEVICE OVERVIEW

The PIC16(L)F19155/56/75/76/85/86 are described within this data sheet. The PIC16(L)F19155/56/75/76/85/86 devices are available in 48-pin TQFP and UQFN, 44-pin TQFP and UQFN, 40-pin PDIP and 28-pin SPDIP, SOIC, SSOP and UQFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F19155/56/75/76/85/86 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F19155/56/75/76/85/86
Analog-to-Digital Converter with Computation (ADC^2)		•
Digital-to-Analog Converter (DAC1)		•
Fixed Voltage Reference (FVR)		•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1 and EUSART2)		•
Temperature Indicator Module (TIM)		•
Zero-Cross Detect (ZCD1)		•
Real-Time Calendar and Clock (RTCC)		•
Liquid Crystal Display (LCD)		•
Capture/Compare/PWM Modules (CCP)		
	CCP1	•
	CCP2	•
Comparator Module (Cx)		
	C1	•
	C2	•
Configurable Logic Cell (CLC)		
	CLC1	•
	CLC2	•
	CLC3	•
	CLC4	•
Complementary Waveform Generator (CWG)		
	CWG1	•
Master Synchronous Serial Ports (MSSP)		
	MSSP1	•
Pulse-Width Modulator (PWM)		
	PWM3	•
	PWM4	•
Signal Measure Timer (SMT)		
	SMT1	•
Timers		
	Timer0	•
	Timer1	•
	Timer2	•
	Timer4	•

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides three specific device functions:

- Device Reset (when MCLRE = 1)
- Digital input pin (when MCLRE = 0)
- Device Programming and Debugging

If programming and debugging are not required in the end application then either set the MCLRE Configuration bit to '1' and use the pin as a digital input or clear the MCLRE Configuration bit and leave the pin open to use the internal weak pull-up. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, the programmer $\overline{MCLR}/V_{PP}$ output should be connected directly to the pin so that R1 isolates the capacitor, C1 from the $\overline{MCLR}$ pin during programming and debugging operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be isolated from the programmer by resistors between the application and the device pins or removed from the circuit during programming. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/ emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 41.0 "Development Support"**.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 3											
CPU CORE REGISTERS; see Table 4-3 for specifics											
18Ch	SSP1BUF	SSPxBUF								xxxx xxxx	xxxx xxxx
18Dh	SSP1ADD	SSPxADD								0000 0000	0000 0000
18Eh	SSP1MSK	SSPxMSK								1111 1111	1111 1111
18Fh	SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
190h	SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
191h	SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
192h	SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000	0000 0000
193h	—	Unimplemented								---- ----	---- ----
194h	—	Unimplemented								---- ----	---- ----
195h	—	Unimplemented								---- ----	---- ----
196h	—	Unimplemented								---- ----	---- ----
197h	—	Unimplemented								---- ----	---- ----
198h	—	Unimplemented								---- ----	---- ----
199h	—	Unimplemented								---- ----	---- ----
19Ah	—	Unimplemented								---- ----	---- ----
19Bh	—	Unimplemented								---- ----	---- ----
19Ch	—	Unimplemented								---- ----	---- ----
19Dh	—	Unimplemented								---- ----	---- ----
19Eh	—	Unimplemented								---- ----	---- ----
19Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

REGISTER 8-3: PCON1: POWER CONTROL REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HC-1/u	R/W/HC-q/u
—	—	—	—	—	—	$\overline{\text{MEMV}}$	$\overline{\text{VBATBOR}}$
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-m/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-2 **Unimplemented:** Read as '0'.

bit 1 **MEMV:** Memory Violation Flag bit
1 = No Memory Violation Reset occurred or set to '1' by firmware
0 = A Memory Violation Reset occurred (set '0' in hardware when a Memory Violation occurs)

bit 0 **VBATBOR:** VBAT Brown-Out Reset Status Bit
1 = No VBAT Brown-out Reset occurred.
0 = A VBAT Brown-out Reset occurred.

8.17 VBAT System

The VBAT subsystem allows the RTCC and SOSC to run from a battery connected to the VBAT pin in the event of a VDD failure. Typically, the battery is a 3V coin cell, however the system is designed to operate over the entire VDD voltage range. If VDD is greater than VBAT, the RTCC and SOSC will be powered by VDD. If VDD is less than VBAT, the RTCC and SOSC will switch over to VBAT. See Table 4-5 and Table 4-8 for more information on the VBAT registers.

Note: It should be noted that in this second scenario, VDD may still be in the valid operating range, but anytime the VDD drops below VBAT, the RTCC and SOSC will switch over to VBAT. This means that in a system with a 3V battery and a 2.8V VDD, the RTCC and SOSC will run off VBAT even when VDD is present.

8.17.1 VBAT GPR SEMAPHORE REGISTERS

The VBAT voltage domain offers the user four registers: VB0GPR, VB1GPR, VB3GPR and VB4GPR. These registers can be used by firmware to write any information that needs to survive a VDD failure. As long as either VDD or VBAT is valid, these registers will hold the last value written.

TABLE 9-1: NOSC/COSC BIT SETTINGS

NOSC<2:0>/ COSC<2:0>	Clock Source
111	EXTOSC(1)
110	HFINTOSC(2)
101	LFINTOSC
100	SOSC
011	Reserved (operates like NOSC = 110)
010	EXTOSC with 4x PLL(1)
001	HFINTOSC with 2x PLL(1)
000	HFINTOSC with OSCFRQ = 32 MHz and CDIV = 1:1

Note 1: EXTOSC configured by the FEXTOSC bits of Configuration Word 1 (Register 5-1).

2: HFINTOSC settings are configured with the HFFRQ bits of the OSCFRQ register (Register 9-6).

TABLE 9-2: NDIV/CDIV BIT SETTINGS

NDIV<3:0>/ CDIV<3:0>	Clock divider
1111-1010	Reserved
1001	512
1000	256
0111	128
0110	64
0101	32
0100	16
0011	8
0010	4
0001	2
0000	1

TABLE 11-2: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	50
VREGCON	—	—	—	—	—	—	VREGPM	—	189
CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE<2:0>			190
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	196

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in Power-Down mode.

13.0 NONVOLATILE MEMORY (NVM) CONTROL

NVM is separated into two types:

- Program Flash Memory (PFM)
- Data EEPROM Memory

NVM is accessible by using both the FSR and the INDF registers, or through the NVMREG register interface. The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device. NVM can be protected in two ways: by either code protection or write protection. Code protection (CP and CPD bits in Configuration Word 5) disables access, reading and writing, to both the PFM and EEPROM via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be Reset by a device programmer performing a Bulk Erase to the device, clearing all nonvolatile memory, Configuration bits, and User IDs. Write protection prohibits self-write and erase to a portion or all of the PFM, as defined by the WRT<1:0> bits of Configuration Word 4. Write protection does not affect a device programmer's ability to read, write, or erase the device.

13.1 Program Flash Memory (PFM)

PFM consists of an array of 14-bit words as user memory, with additional words for User ID information, Configuration Words, and interrupt vectors. PFM provides storage locations for:

- User program instructions
- User defined data

PFM data can be read and/or written to through:

- CPU instruction fetch (read-only)
- FSR/INDF indirect access (read-only) (**Section 13.3 "FSR and INDF Access"**)
- NVMREG access (**Section 13.4 "NVMREG Access"**
- In-Circuit Serial Programming™ (ICSP™)

Read operations return a single word of memory. When write and erase operations are done on a row basis, the row size is defined in Table 13-1. PFM will erase to a logic '1' and program to a logic '0'.

TABLE 13-1: FLASH MEMORY ORGANIZATION BY DEVICE

Device	Row Erase (words)	Write Latches (words)	Total Program Flash
PIC16(L)F19155	32	32	8k
PIC16(L)F19175	32	32	8k
PIC16(L)F19185	32	32	8k
PIC16(L)F19156	32	32	16k
PIC16(L)F19176	32	32	16k
PIC16(L)F19186	32	32	16k

It is important to understand the PFM memory structure for erase and programming operations. PFM is arranged in rows. A row consists of 32 14-bit program memory words. A row is the minimum size that can be erased by user software.

All or a portion of this row can be programmed. Data to be written into the program memory row is written to 14-bit wide data write latches. These latches are not directly accessible, but may be loaded via sequential writes to the NVMDATH:NVMDATL register pair.

Note:	To modify only a portion of a previously programmed row, the contents of the entire row must be read. Then, the new data and retained data can be written into the write latches to reprogram the row of PFM. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations

13.1.1 PROGRAM MEMORY VOLTAGES

The PFM is readable and writable during normal operation over the full VDD range.

13.1.1.1 Programming Externally

The program memory cell and control logic support write and Bulk Erase operations down to the minimum device operating voltage.

13.1.1.2 Self-programming

The program memory cell and control logic will support write and row erase operations at high VDD. Bulk Erase is not available when self-programming.

19.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 19-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 19-4. **The maximum recommended impedance for analog sources is 1 kΩ.** If the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be completed before the conversion can be started. To calculate the minimum acquisition time, Equation 19-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified accuracy.

EQUATION 19-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $1k\Omega$ *5.0V* V_{DD}

$$T_{ACQ} = Amplifier\ Settling\ Time + Hold\ Capacitor\ Charging\ Time + Temperature\ Coefficient$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} \quad ;[1]\ V_{CHOLD}\ charged\ to\ within\ 1/2\ lsb$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad ;[2]\ V_{CHOLD}\ charge\ response\ to\ V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \quad ;combining\ [1]\ and\ [2]$$

Note: Where n = number of bits of the ADC.

Solving for T_C*:*

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/8191)$$
$$= -28\ pF(1k\Omega + 7k\Omega + 1k\Omega)\ ln(0.0001221)$$
$$= 2.27\mu s$$

Therefore:

$$T_{ACQ} = 2\ \mu s + 4.54\ \mu s + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 5.52\mu s$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 1kΩ. This is required to meet the pin leakage specification.

21.4 Operation During Sleep

The DAC continues to function during Sleep. When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DAC1CON0 register are not affected.

21.5 Effects of a Reset

A device Reset affects the following:

- DAC is disabled.
- DAC output voltage is removed from the DAC1OUT1/2 pins.
- The DAC1R<4:0> range select bits are cleared.

REGISTER 26-4: T1GATE TIMER1 GATE SELECT REGISTER

U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	GSS<4:0>				
bit 7							bit 0

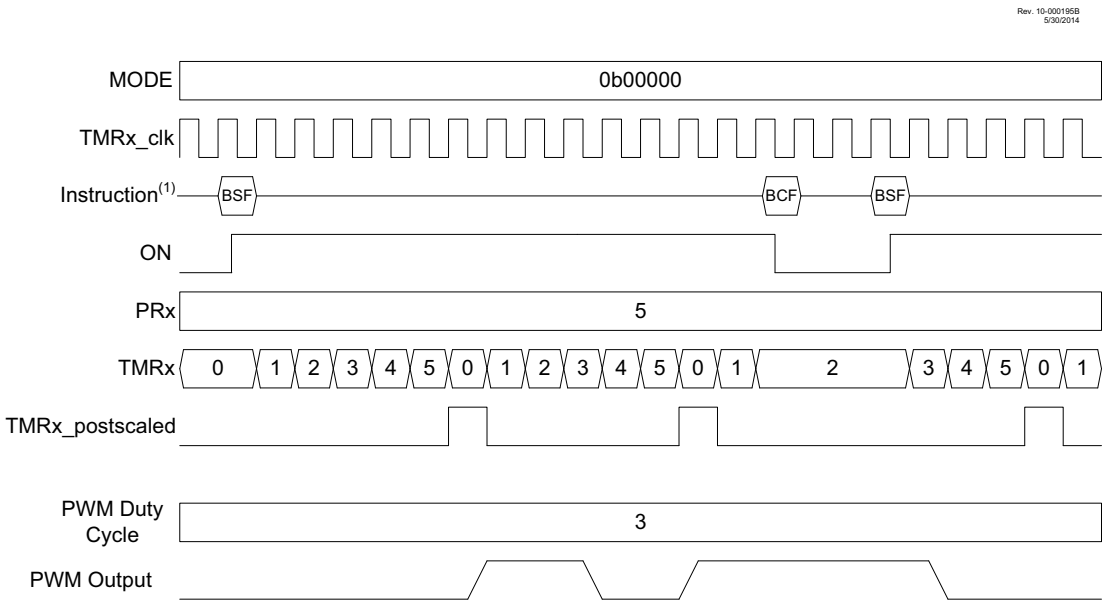
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **GSS<4:0>:** Timer1 Gate Select bits

11111-10001 = Reserved
10000 = RTCC second output
01111 = ZCD1 output
01110 = C2OUT output
01101 = C1OUT output
01100 = LC4 out
01011 = LC3 out
01010 = LC2 out
01001 = LC1 out
01000 = PWM4 out
00111 = PWM3 out
00110 = CCP2 out
00101 = CCP1 out
00100 = SMT1 overflow output
00011 = TMR4 postscaled
00010 = TMR2 postscaled
00001 = Timer0 overflow output
00000 = T1GPPS

FIGURE 27-4: SOFTWARE GATE MODE TIMING DIAGRAM (MODE = 00000)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

28.2 SMT Operation

The core of the module is the 24-bit counter, SMTxTMR combined with a complex data acquisition front-end. Depending on the mode of operation selected, the SMT can perform a variety of measurements summarized in Table .

28.2.1 CLOCK SOURCES

Clock sources available to the SMT include:

- FOSC
- FOSC/4
- HFINTOSC
- MFINTOSC (500 kHz and 31.25 kHz)
- LFINTOSC
- SOSC

The SMT clock source is selected by configuring the CSEL<2:0> bits in the SMTxCLK register. The clock source can also be prescaled using the PS<1:0> bits of the SMTxCON0 register. The prescaled clock source is used to clock both the counter and any synchronization logic used by the module.

28.2.2 PERIOD MATCH INTERRUPT

Similar to other timers, the SMT triggers an interrupt when SMTxTMR rolls over to '0'. This happens when SMTxTMR = SMTxPR, regardless of mode. Hence, in any mode that relies on an external signal or a window to reset the timer, proper operation requires that SMTxPR be set to a period larger than that of the expected signal or window.

28.3 Basic Timer Function Registers

The SMTxTMR time base and the SMTxCPW/SMTxPR/SMTxCPR buffer registers serve several functions and can be manually updated using software.

28.3.1 TIME BASE

The SMTxTMR is the 24-bit counter that is the center of the SMT. It is used as the basic counter/timer for measurement in each of the modes of the SMT. It can be reset to a value of 24'h00_0000 by setting the RST bit of the SMTxSTAT register. It can be written to and read from software, but it is not guarded for atomic access, therefore reads and writes to the SMTxTMR should only be made when the GO = 0, or the software should have other measures to ensure integrity of SMTxTMR reads/writes.

28.3.2 PULSE-WIDTH LATCH REGISTERS

The SMTxCPW registers are the 24-bit SMT pulse width latch. They are used to latch in the value of the SMTxTMR when triggered by various signals, which are determined by the mode the SMT is currently in.

The SMTxCPW registers can also be updated with the current value of the SMTxTMR value by setting the CPWUP bit of the SMTxSTAT register.

28.3.3 PERIOD LATCH REGISTERS

The SMTxCPR registers are the 24-bit SMT period latch. They are used to latch in values of the SMTxTMR when triggered by various other signals, which are determined by the mode the SMT is currently in.

The SMTxCPR registers can also be updated with the current value of the SMTxTMR value by setting the CPRUP bit in the SMTxSTAT register.

28.4 Halt Operation

The counter can be prevented from rolling-over using the STP bit in the SMTxCON0 register. When halting is enabled, the period match interrupt persists until the SMTxTMR is reset (either by a manual Reset, **Section 28.3.1 "Time Base"**) or by clearing the SMTxGO bit of the SMTxCON1 register and writing the SMTxTMR values in software.

28.5 Polarity Control

The three input signals for the SMT have polarity control to determine whether or not they are active high/positive edge or active low/negative edge signals.

The following bits apply to Polarity Control:

- WSEL bit (Window Polarity)
- SSEL bit (Signal Polarity)
- CSEL bit (Clock Polarity)

These bits are located in the SMTxCON0 register.

28.6 Status Information

The SMT provides input status information for the user without requiring the need to deal with the polarity of the incoming signals.

28.6.1 WINDOW STATUS

Window status is determined by the WS bit of the SMTxSTAT register. This bit is only used in Windowed Measure, Gated Counter and Gated Window Measure modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

28.6.2 SIGNAL STATUS

Signal status is determined by the AS bit of the SMTxSTAT register. This bit is used in all modes except Window Measure, Time of Flight and Capture modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

29.3.4 TIMER2 TIMER RESOURCE

This device has a newer version of the Timer2 module that has many new modes, which allow for greater customization and control of the PWM signals than on older parts. Refer to **Section 27.5 "Operation Examples"** for examples of PWM signal generation using the different modes of Timer2. The CCP operation requires that the timer used as the PWM time base has the FOSC/4 clock source selected

29.3.5 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 29-1.

EQUATION 29-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

Note 1: TOSC = 1/FOSC

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is transferred from the CCPRxL/H register pair into a 10-bit buffer.

Note:	The Timer postscaler (see **Section 27.4 "Timer2/4 Interrupt"**) is not used in the determination of the PWM frequency.

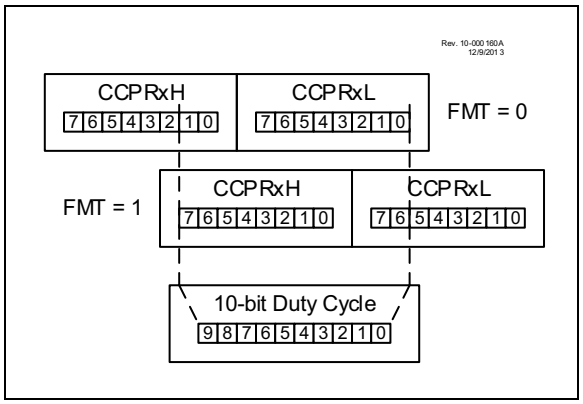
29.3.6 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the CCPRxH:CCPRxL register pair. The alignment of the 10-bit value is determined by the CCPRxFMT bit of the CCPxCON register (see Figure 29-5). The CCPRxH:CCPRxL register pair can be written to at any time; however the duty cycle value is not latched into the 10-bit buffer until after a match between PR2 and TMR2.

Equation 29-2 is used to calculate the PWM pulse width.

Equation 29-3 is used to calculate the PWM duty cycle ratio.

FIGURE 29-5: PWM 10-BIT ALIGNMENT



EQUATION 29-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxH{:}CCPRxL\ register\ pair) \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

EQUATION 29-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxH{:}CCPRxL\ register\ pair)}{4(PR2 + 1)}$$

CCPRxH:CCPRxL register pair are used to double buffer the PWM duty cycle. This double buffering provides for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH:CCPRxL register pair, then the CCPx pin is cleared (see Figure 29-4).

29.3.7 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 29-4.

EQUATION 29-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)}\ bits$$

Note:	If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

30.0 PULSE-WIDTH MODULATION (PWM)

The PWMx modules generate Pulse-Width Modulated (PWM) signals of varying frequency and duty cycle.

In addition to the CCP modules, the PIC16(L)F19155/56/75/76/85/86 devices contain two PWM modules (PWM3 and PWM4). The PWM modules reproduce the PWM capability of the CCP modules.

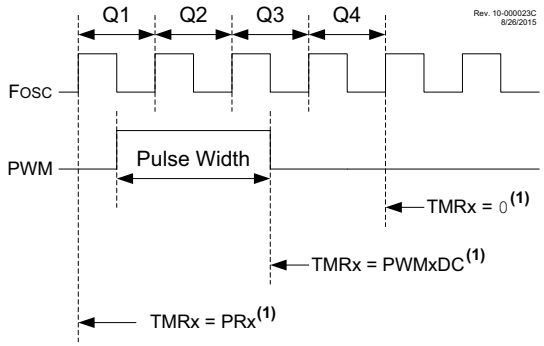
Note:	The PWM3/4 modules are two instances of the same PWM module design. Throughout this section, the lower case 'x' in register and bit names is a generic reference to the PWM module number (which should be substituted with 3, or 4 during code development). For example, the control register is generically described in this chapter as PWMxCON, but the actual device registers are PWM3CON and PWM4CON. Similarly, the PWMxEN bit represents the PWM3EN and PWM4EN bits.

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully ON and fully OFF states. The PWM signal resembles a square wave where the high portion of the signal is considered the 'ON' state (pulse width), and the low portion of the signal is considered the 'OFF' state. The term duty cycle describes the proportion of the 'on' time to the 'off' time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and, in turn, the power that is applied to the load.

Figure 30-1 shows a typical waveform of the PWM signal.

FIGURE 30-1: PWM OUTPUT



Note 1: Timer dependent on PWMTMRS register settings.

31.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces half-bridge, full-bridge, and steering of PWM waveforms. It is backwards compatible with previous ECCP functions.

The CWG has the following features:

- Six Operating modes:
  - Synchronous Steering mode
  - Asynchronous Steering mode
  - Full-Bridge mode, Forward
  - Full-Bridge mode, Reverse
  - Half-Bridge mode
  - Push-Pull mode
- Output Polarity Control
- Output Steering:
  - Synchronized to rising event
  - Immediate effect
- Independent 6-Bit Rising and Falling Event Dead-Band Timers:
  - Clocked dead band
  - Independent rising and falling dead-band enables
- Auto-Shutdown Control with:
  - Selectable shutdown sources
  - Auto-restart enable
  - Auto-shutdown pin override control

The CWG modules available are shown in Table 31-1.

TABLE 31-1: AVAILABLE CWG MODULES

Device	CWG1
PIC16(L)F19155/56/75/76/85/86	●

31.1 Fundamental Operation

The CWG module can operate in six different modes, as specified by MODE of the CWG1CON0 register:

- Half-Bridge mode (Figure 31-9)
- Push-Pull mode (Figure 31-2)
  - Full-Bridge mode, Forward (Figure 31-3)
  - Full-Bridge mode, Reverse (Figure 31-3)
- Steering mode (Figure 31-10)
- Synchronous Steering mode (Figure 31-11)

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. Thus, all output modes support auto-shutdown, which is covered in **Section 31.10 “Auto-Shutdown”**.

31.1.1 HALF-BRIDGE MODE

In Half-Bridge mode, two output signals are generated as true and inverted versions of the input as illustrated in Figure 31-9. A non-overlap (dead-band) time is inserted between the two outputs as described in **Section 31.5 “Dead-Band Control”**.

The unused outputs CWG1C and CWG1D drive similar signals, with polarity independently controlled by the POLC and POLD bits of the CWG1CON1 register, respectively.

REGISTER 31-2: CWG1CON1: CWG1 CONTROL REGISTER 1

U-0	U-0	R-x	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IN	—	POLD	POLC	POLB	POLA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IN:** CWG Input Value bit

bit 4 **Unimplemented:** Read as '0'

bit 3 **POLD:** CWG1D Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 2 **POLC:** CWG1C Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 1 **POLB:** CWG1B Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 0 **POLA:** CWG1A Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

REGISTER 32-7: CLCxGLS0: GATE 0 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG1D4T	LCxG1D4N	LCxG1D3T	LCxG1D3N	LCxG1D2T	LCxG1D2N	LCxG1D1T	LCxG1D1N
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **LCxG1D4T:** Gate 0 Data 4 True (non-inverted) bit
1 = CLCIN3 (true) is gated into CLCx Gate 0
0 = CLCIN3 (true) is not gated into CLCx Gate 0

bit 6 **LCxG1D4N:** Gate 0 Data 4 Negated (inverted) bit
1 = CLCIN3 (inverted) is gated into CLCx Gate 0
0 = CLCIN3 (inverted) is not gated into CLCx Gate 0

bit 5 **LCxG1D3T:** Gate 0 Data 3 True (non-inverted) bit
1 = CLCIN2 (true) is gated into CLCx Gate 0
0 = CLCIN2 (true) is not gated into CLCx Gate 0

bit 4 **LCxG1D3N:** Gate 0 Data 3 Negated (inverted) bit
1 = CLCIN2 (inverted) is gated into CLCx Gate 0
0 = CLCIN2 (inverted) is not gated into CLCx Gate 0

bit 3 **LCxG1D2T:** Gate 0 Data 2 True (non-inverted) bit
1 = CLCIN1 (true) is gated into CLCx Gate 0
0 = CLCIN1 (true) is not gated into l CLCx Gate 0

bit 2 **LCxG1D2N:** Gate 0 Data 2 Negated (inverted) bit
1 = CLCIN1 (inverted) is gated into CLCx Gate 0
0 = CLCIN1 (inverted) is not gated into CLCx Gate 0

bit 1 **LCxG1D1T:** Gate 0 Data 1 True (non-inverted) bit
1 = CLCIN0 (true) is gated into CLCx Gate 0
0 = CLCIN0 (true) is not gated into CLCx Gate 0

bit 0 **LCxG1D1N:** Gate 0 Data 1 Negated (inverted) bit
1 = CLCIN0 (inverted) is gated into CLCx Gate 0
0 = CLCIN0 (inverted) is not gated into CLCx Gate 0

The I^2C interface supports the following modes and features:

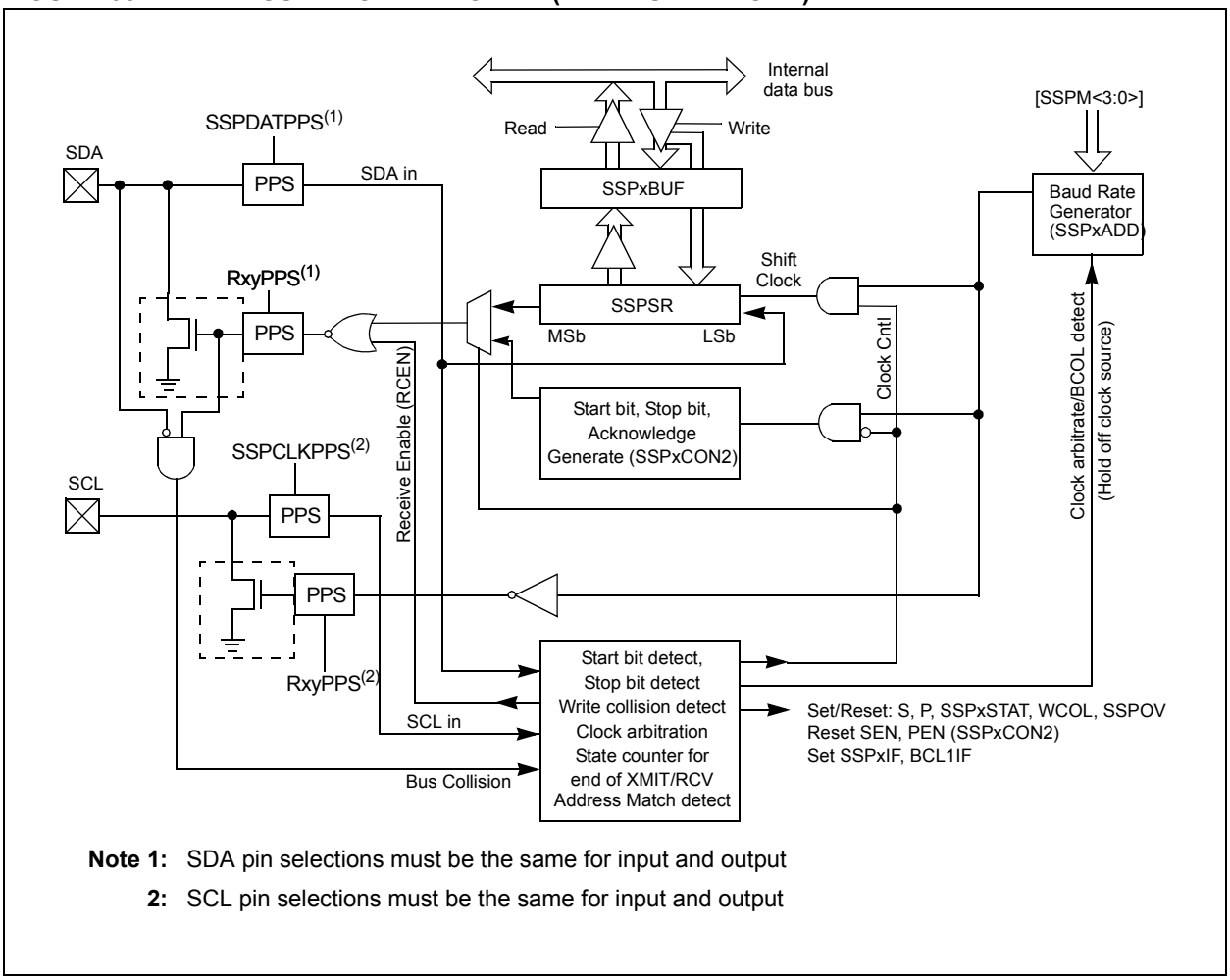
- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- Limited multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- Bus collision detection
- General call address matching
- Address masking
- Selectable SDA hold times

Figure 33-2 is a block diagram of the I^2C interface module in Master mode. Figure 33-3 is a diagram of the I^2C interface module in Slave mode.

Note 1: In devices with more than one MSSP module, it is very important to pay close attention to SSPxCONx register names. SSPxCON1 and SSPxCON2 registers control different operational aspects of the same module, while SSPxCON1 and SSP2CON1 control the same features for two different modules.

2: Throughout this section, generic references to an MSSPx module in any of its operating modes may be interpreted as being equally applicable to MSSPx or MSSP2. Register names, module I/O signals, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module when required.

FIGURE 33-2: MSSP BLOCK DIAGRAM (I^2C MASTER MODE)



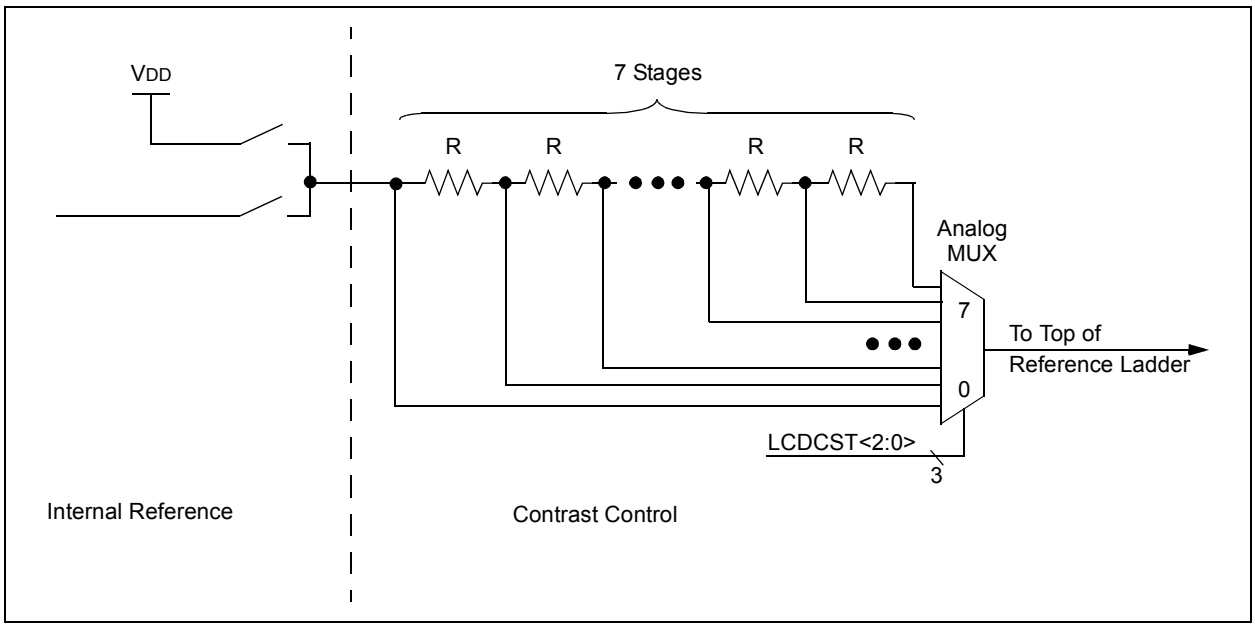
Note 1: SDA pin selections must be the same for input and output

2: SCL pin selections must be the same for input and output

35.5.3 CONTRAST CONTROL

The LCD contrast control circuit consists of a 7-tap resistor ladder, controlled by the LCDCSTx bits (see Figure 35-4).

FIGURE 35-4: INTERNAL REFERENCE AND CONTRAST CONTROL BLOCK DIAGRAM



35.6 Bias Generation

35.6.1 INTERNAL REFERENCE

An internal reference for the LCD bias voltage can be enabled under firmware control. When enabled, the source of this voltage can be VDD, LCD charge pump or 3x FVR.

When no internal reference is selected, the LCD contrast control circuit is disabled and LCD bias must be provided externally. Whenever the LCD module is inactive (LCDA = 0), the internal reference will be turned off.

35.6.2 VLCDx PINS AND EXTERNAL BIAS

The VLCD3, VLCD2 and VLCD1 pins provide the ability for an external LCD bias network to be used instead of the internal ladder. Use of the VLCDx pins does not prevent use of the internal ladder.

35.6.3 LCD BIAS GENERATION

The LCD driver module is capable of generating the required bias voltages for LCD operation with a minimum of external components. This includes the ability to generate the different voltage levels required by the different bias types that are required by the LCD. The driver module can also provide bias voltages, both above and below microcontroller VDD, through the use of an on-chip LCD charge pump.

35.6.4 LCD CHARGE PUMP

The purpose of the LCD charge pump is to provide proper bias voltage and good contrast for the LCD, regardless of VDD levels. This module contains a charge pump and internal voltage reference. The charge pump can be configured by using external components to boost bias voltage above VDD. It can also operate a display at a constant voltage below VDD. The charge pump can also be selectively disabled to allow bias voltages to be generated by an external resistor network.

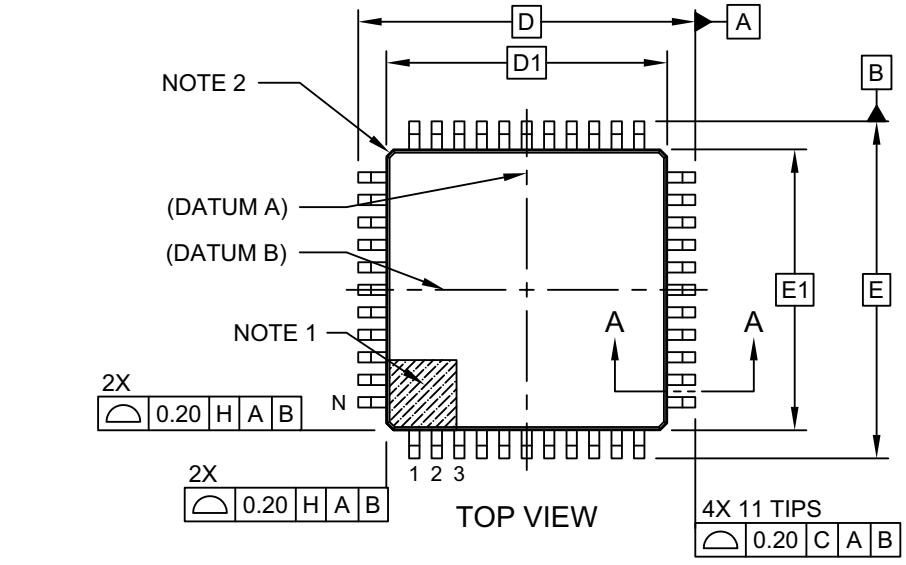
The LCD charge pump is controlled through the LCDVCONx registers.

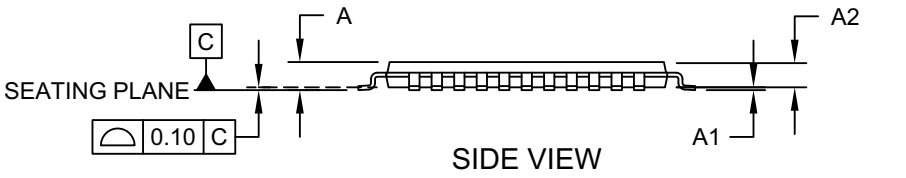
35.6.5 VLCD3 MONITORING

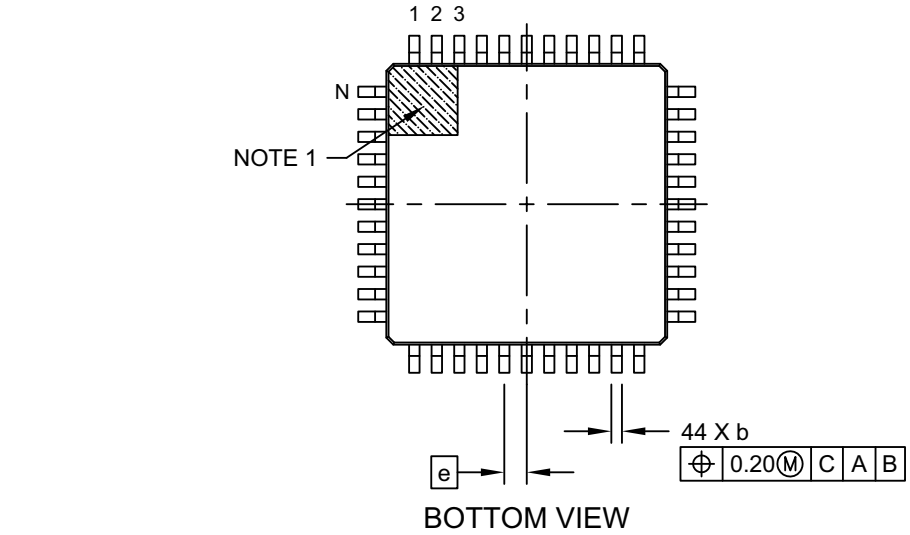
The ADC can be used to measure the VLCD3 voltage via a VLCD3 divided by 4 channel on the ADC. This feature is useful when active adjustment of the LCDCST<2:0> or BIAS<2:0> bits need to be made to account of contrast changes due to extreme temperatures and/or a high number of large active pixels. See **Section 19.0 "Analog-to-Digital Converter with Computation (ADC2) Module"** for additional details.

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







Microchip Technology Drawing C04-076C Sheet 1 of 2