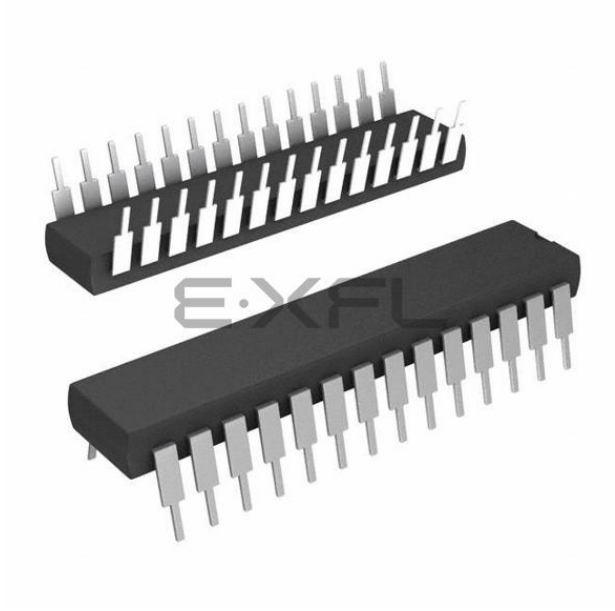

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19156-i-sp

TABLE 1-2: PIC16(L)F19155/56 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/C1IN2-/C2IN2-/IOCB3/ANB3/SEG11/COM6/ SEGCFLY2	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
	ANB3	AN	—	ADC Channel input.
	SEG11	—	AN	LCD Analog output.
	COM6	—	AN	LCD Driver Common Outputs.
	SEGCFLY2	AN	—	LCD Drive Charge Pump Capacitor Inputs
RB4/ADCACT(1)/IOCB4/ANB4/COM0	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ADCACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input
	IOCB4	TTL/ST	—	Interrupt-on-change input.
	ANB4	AN	—	ADC Channel input.
	COM0	—	AN	LCD Driver Common Outputs.
RB5/T1G(1)/IOCB5/ANB5/SEG13/COM1	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	T1G(1)	—	—	Timer1 Gate input.
	IOCB5	TTL/ST	—	Interrupt-on-change input.
	ANB5	AN	—	ADC Channel input.
	SEG13	—	AN	LCD Analog output.
	COM1	—	AN	LCD Driver Common Outputs.
RB6/CK2(3)/TX2(1)/CLCIN2(1)/IOCB6/ANB6/SEG14/ ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	CK2(3)	—	—	EUSART synchronous clock out
	TX2(1)	—	—	EUSART asynchronous TX data out
	CLCIN2(1)	—	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	ANB6	AN	—	ADC Channel input.
	SEG14	—	AN	LCD Analog output.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
RB7/DK2(3)/RX2(1)/CLCIN3(1)/IOCB7/ANB7/SEG15/ DAC1OUT2/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	DK2(3)	—	—	EUSART synchronous data output
	RX2(1)	—	—	EUSART receive input.
	CLCIN3(1)	—	—	Configurable Logic Cell source input.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	ANB7	AN	—	ADC Channel input.
	SEG15	—	AN	LCD Analog output.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	TTL/ST	TTL/ST	In-Circuit Serial Programming™ and debugging data input/output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input‘; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

4.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Program Flash Memory
  - Device Information Area (DIA)
  - Device Configuration Information (DCI)
  - Revision ID
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM (GPR)
  - Common RAM
- Data EEPROM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing
- NVMREG access

4.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing 32K x 14 program memory space. Table 4-1 shows the memory sizes implemented. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 4-1).

TABLE 4-1: DEVICE SIZES AND ADDRESSES

Device	Program Flash Memory Size (Words)	Last Program Memory Address
PIC16(L)F19155	8k	1FFFh
PIC16(L)F19175	8k	1FFFh
PIC16(L)F19185	8k	1FFFh
PIC16(L)F19156	16k	3FFFh
PIC16(L)F19176	16k	3FFFh
PIC16(L)F19186	16k	3FFFh

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 13											
CPU CORE REGISTERS; see Table 4-3 for specifics											
68Ch	—	Unimplemented								---- ----	---- ----
68Dh	—	Unimplemented								---- ----	---- ----
68Eh	—	Unimplemented								---- ----	---- ----
68Fh	—	Unimplemented								---- ----	---- ----
690h	—	Unimplemented								---- ----	---- ----
691h	—	Unimplemented								---- ----	---- ----
692h	—	Unimplemented								---- ----	---- ----
693h	—	Unimplemented								---- ----	---- ----
694h	—	Unimplemented								---- ----	---- ----
695h	—	Unimplemented								---- ----	---- ----
696h	—	Unimplemented								---- ----	---- ----
697h	—	Unimplemented								---- ----	---- ----
698h	—	Unimplemented								---- ----	---- ----
699h	—	Unimplemented								---- ----	---- ----
69Ah	—	Unimplemented								---- ----	---- ----
69Bh	—	Unimplemented								---- ----	---- ----
69Ch	—	Unimplemented								---- ----	---- ----
69Dh	—	Unimplemented								---- ----	---- ----
69Eh	—	Unimplemented								---- ----	---- ----
69Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 16											
CPU CORE REGISTERS; see Table 4-3 for specifics											
80Ch	WDTCON0	—	—	WDTPS<4:0>					SWDTEN	--qq qqq0	--qq qqq0
80Dh	WDTCON1	—	WDTCS<2:0>			—	WINDOW<2:0>			-qqq -qqq	-qqq -qqq
80Eh	WDTPSL	PSCNT								0000 0000	0000 0000
80Fh	WDTPSH	PSCNT								0000 0000	0000 0000
810h	WDTTMR	—	WDTTMR<3:0>				STATE	PSCNT17	PSCNT16	-xxx x000	-xxx x000
811h	BORCON	SBOREN	—	—	—	—	—	—	BORRDY	1--- ---q	u--- ---u
812h	VREGCON	—	—	—	—	—	—	VREGPM	—	---- --x-	---- --x-
813h	PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	0011 110q	qqqq qquu
814h	PCON1	—	—	—	—	—	—	$\overline{\text{MEMV}}$	$\overline{\text{VBATBOR}}$	---- --1x	---- --qu
815h	—	Unimplemented								---- ----	---- ----
816h	—	Unimplemented								---- ----	---- ----
817h	—	Unimplemented								---- ----	---- ----
818h	—	Unimplemented								---- ----	---- ----
819h	—	Unimplemented								---- ----	---- ----
81Ah	NVMADRL	NVMADR7	NVMADR6	NVMADR5	NVMADR4	NVMADR3	NVMADR2	NVMADR1	NVMADR0	xxxx xxxx	uuuu uuuu
81Bh	NVMADRH	—	NVMADR14	NVMADR13	NVMADR12	NVMADR11	NVMADR10	NVMADR9	NVMADR8	1xxx xxxx	1uuu uuuu
81Ch	NVMDATL	NVMDAT7	NVMDAT6	NVMDAT5	NVMDAT4	NVMDAT3	NVMDAT2	NVMDAT1	NVMDAT0	0000 0000	0000 0000
81Dh	NVMDATH	—	—	NVMDAT13	NVMDAT12	NVMDAT11	NVMDAT10	NVMDAT9	NVMDAT8	0000 0000	0000 0000
81Eh	NVMCON1	—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 0000	0000 0000
81Fh	NVMCON2	NVMCON2<7:0>								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Banks 30-57											
CPU CORE REGISTERS; see Table 4-3 for specifics											
F0Ch — 1C9Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 59											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1D8Ch — 1D9Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

REGISTER 10-19: PIR8: PERIPHERAL INTERRUPT REQUEST REGISTER 8

R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **LCDIF:** LCD Interrupt Flag bit
1 = A LCDIF interrupt condition has occurred (must be cleared in software)
0 = No LCDIF interrupt event has occurred

bit 6 **RTCCIF:** LCD Interrupt Flag bit
1 = A RTCCIF interrupt condition has occurred (must be cleared in software)
0 = No RTCCIF interrupt event has occurred

bit 5-3 **Unimplemented:** Read as '0'

bit 2 **SMT1PWAIF:** SMT1 Pulse-Width Acquisition Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **SMT1PRAIF:** SMT1 Period Acquisition Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **SMT1IF:** SMT1 Overflow Interrupt Flag bit
1 = An SMT overflow event has occurred (must be cleared in software)
0 = No overflow event detected

EXAMPLE 13-5: DEVICE ID ACCESS

```
; This write routine assumes the following:
; 1. A full row of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
; stored in little endian format
; 3. A valid starting address (the least significant bits = 00000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
; 5. NVM interrupts are not taken into account
BANKSEL NVMADRH
MOVF ADDRH,W
MOVWF NVMADRH               ; Load initial address
MOVF ADDRL,W
MOVWF NVMADRL
MOVLW LOW DATA_ADDR           ; Load initial data address
MOVWF FSR0L
MOVLW HIGH DATA_ADDR
MOVWF FSR0H
BCF NVMCON1,NVMREGS           ; Set PFM as write location
BSF NVMCON1,WREN              ; Enable writes
BSF NVMCON1,LWLO             ; Load only write latches
LOOP
MOVIW FSR0++
MOVWF NVMDATL             ; Load first data byte
MOVIW FSR0++
MOVWF NVMDATH               ; Load second data byte
CALL UNLOCK_SEQ             ; If not, go load latch
INCF NVMADRL,F              ; Increment address
MOVF NVMADRL,W
XORLW 0x1F                  ; Check if lower bits of address are 00000
ANDLW 0x1F                  ; and if on last of 32 addresses
BTFSC STATUS,Z             ; Last of 32 words?
GOTO START_WRITE            ; If so, go write latches into memory
GOTO LOOP
START_WRITE
BCF NVMCON1,LWLO            ; Latch writes complete, now write memory
CALL UNLOCK_SEQ             ; Perform required unlock sequence
BCF NVMCON1,LWLO            ; Disable writes
UNLOCK_SEQ
MOVLW 55h
BCF INTCON,GIE               ; Disable interrupts
MOVWF NVMCON2                ; Begin unlock sequence
MOVLW AAh
MOVWF NVMCON2
BSF NVMCON1,WR
BSF INTCON,GIE               ; Unlock sequence complete, re-enable interrupts
```

REGISTER 14-29: WPUD: WEAK PULL-UP PORTD REGISTER(2)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUD<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.
2: **Not** available on the PIC16(L)F19155/56 family of devices.

REGISTER 14-30: ODCOND: PORTD OPEN-DRAIN CONTROL REGISTER(1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODCD<7:0>:** PORTD Open-Drain Enable bits
For RD<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

Note 1: **Not** available on the PIC16(L)F19155/56 family of devices.

REGISTER 14-39: SLRCONE: PORTE SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1
SLRE7	SLRE6	SLRE5	SLRE4	SLRE3	—	SLRE1	SLRE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **SLRE<7:3>:** PORTE Slew Rate Enable bits
For RE<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **SLRE<1:0>:** PORTE Slew Rate Enable bits
For RE<1:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 14-40: INLVLE: PORTE INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1
INLVLE7	INLVLE6	INLVLE5	INLVLE4	INLVLE3	—	INLVLE1	INLVLE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **INLVLE<7:3>:** PORTE Input Level Select bits
For RE<7:3> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **INLVLE<1:0>:** PORTE Input Level Select bits
For RE<1:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

REGISTER 17-9: IOCCF: INTERRUPT-ON-CHANGE PORTC FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCCF7	IOCCF6	—	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6 **IOCCF<7:6>:** Interrupt-on-Change PORTC Flag bits
1 = An enabled change was detected on the associated pin
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.
0 = No change was detected, or the user cleared the detected change

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **IOCCF<4:0>:** Interrupt-on-Change PORTC Flag bits
1 = An enabled change was detected on the associated pin
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.
0 = No change was detected, or the user cleared the detected change

REGISTER 17-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3(1)	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEP3:** Interrupt-on-Change PORTE Positive Edge Enable bit
1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCEFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

bit 2-0 **Unimplemented:** Read as '0'

Note 1: If MCLRE = 1 or LVP = 1, RC port functionality is disabled and IOC is not available on RE3.

REGISTER 22-3: CMxNSEL: COMPARATOR Cx NEGATIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	NCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 **Unimplemented:** Read as '0'

bit 2-0 **NCH<2:0>:** Comparator Negative Input Channel Select bits

111 = CxVN connects to AVSS
110 = CxVN connects to FVR Buffer 2
101 = CxVN unconnected
100 = CxVN connects to CxIN4- pin
011 = CxVN connects to CxIN3- pin
010 = CxVN connects to CxIN2- pin
001 = CxVN connects to CxIN1- pin
000 = CxVN connects to CxIN0- pin

REGISTER 22-4: CMxPSEL: COMPARATOR Cx POSITIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	PCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 **Unimplemented:** Read as '0'

bit 5-3 **PCH<2:0>:** Comparator Positive Input Channel Select bits

111 = CxVP connects to AVSS
110 = CxVP connects to FVR Buffer 2
101 = CxVP connects to DAC output
100 = CxVP LCD VREF(1)
011 = CxVP unconnected
010 = CxVP unconnected
001 = CxVP connects to CxIN1+ pin
000 = CxVP connects to CxIN0+ pin

Note 1: Applies to C2 comparator only.

FIGURE 26-4: TIMER1 GATE TOGGLE MODE

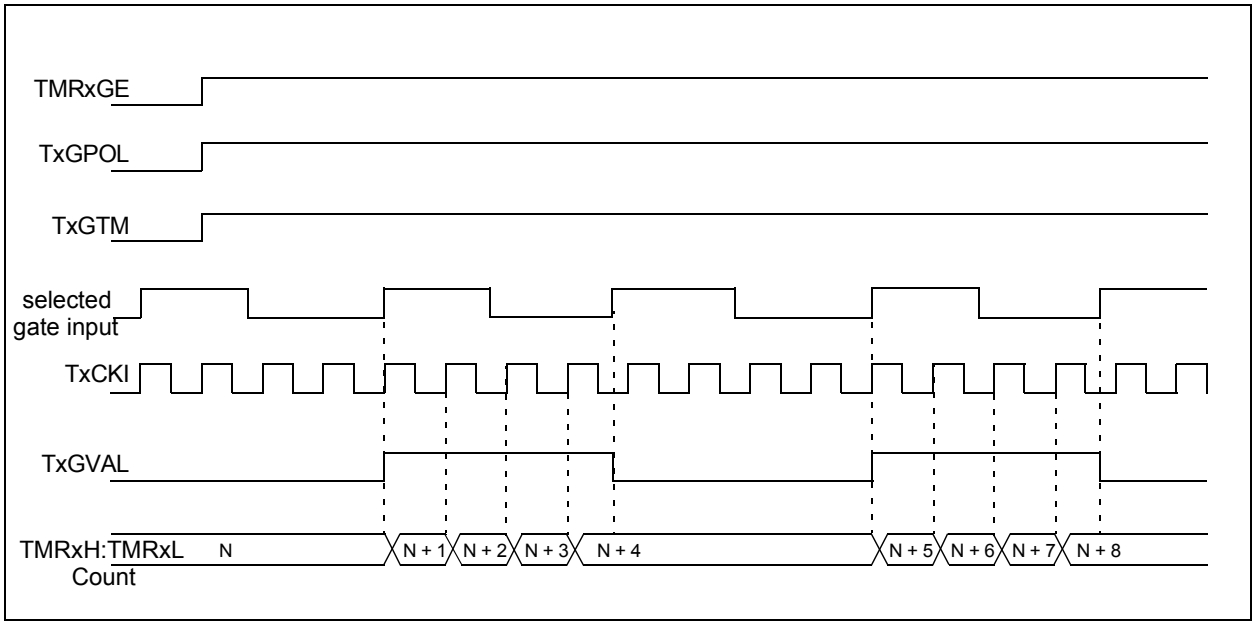


FIGURE 26-5: TIMER1 GATE SINGLE-PULSE MODE

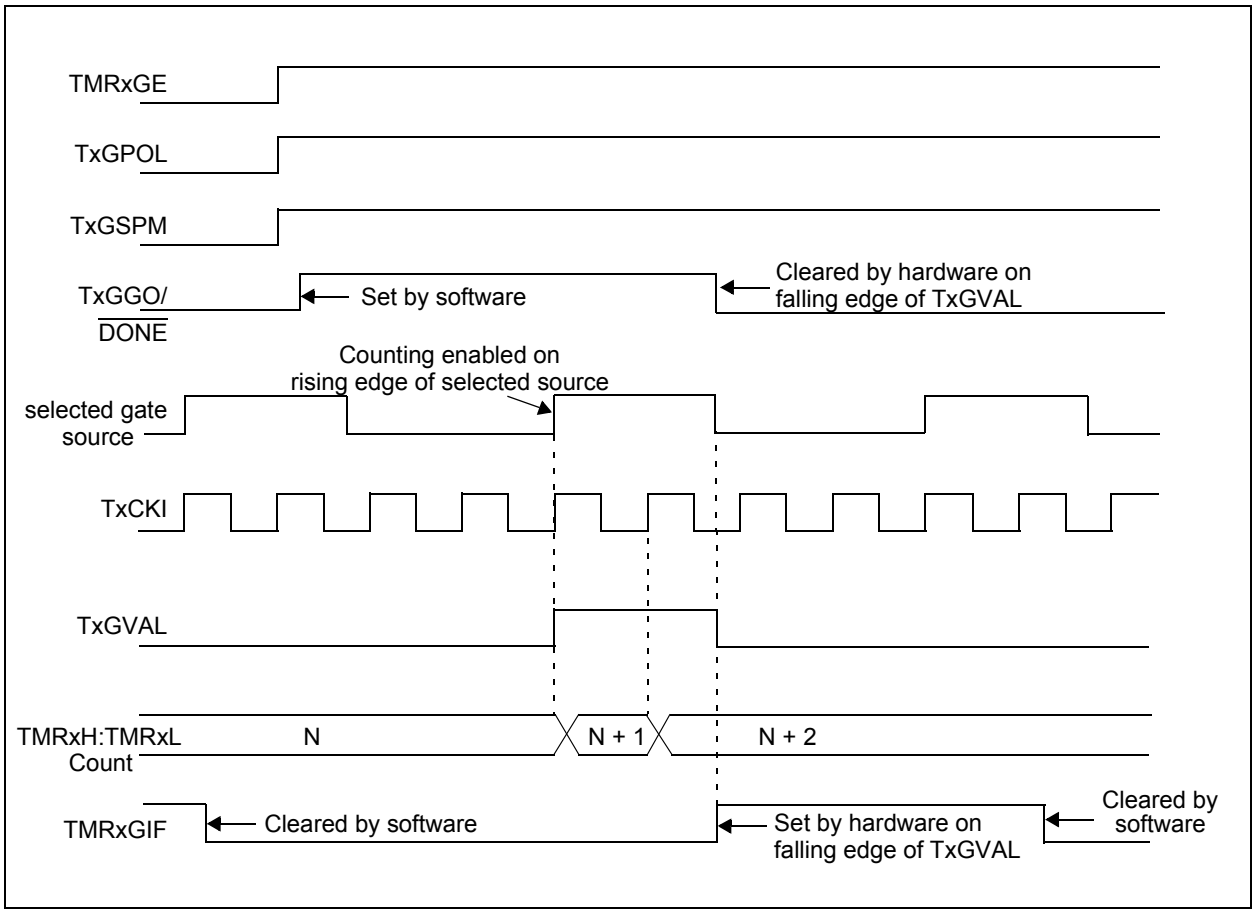


FIGURE 33-7: SPI DAISY-CHAIN CONNECTION

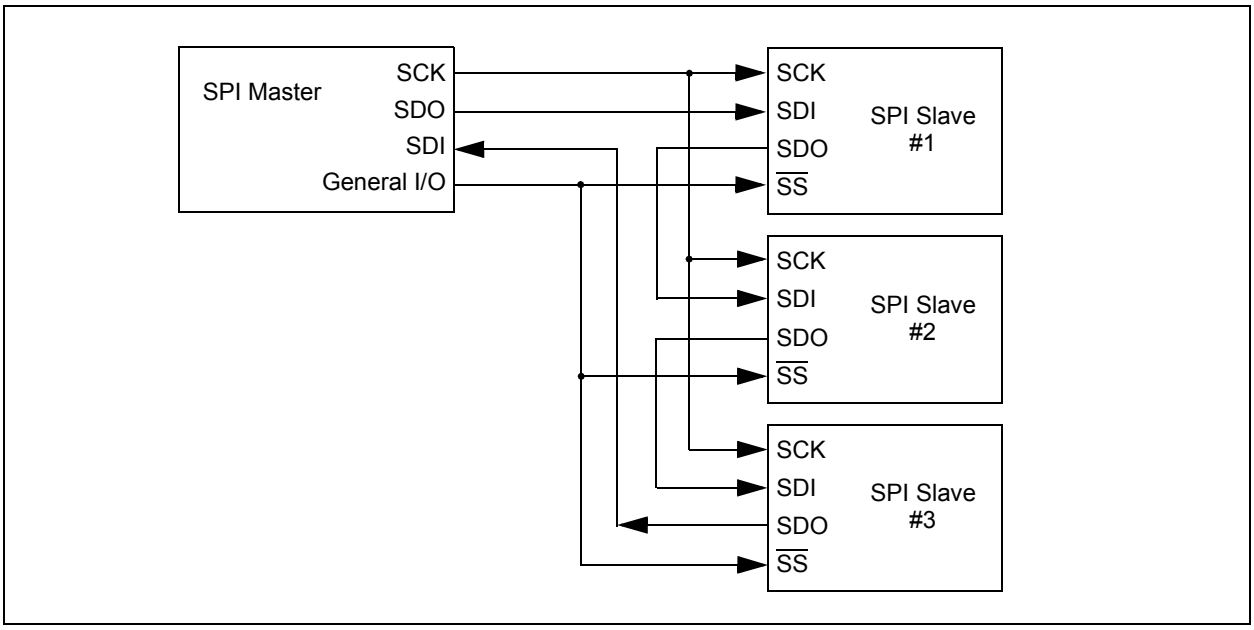


FIGURE 33-8: SLAVE SELECT SYNCHRONOUS WAVEFORM

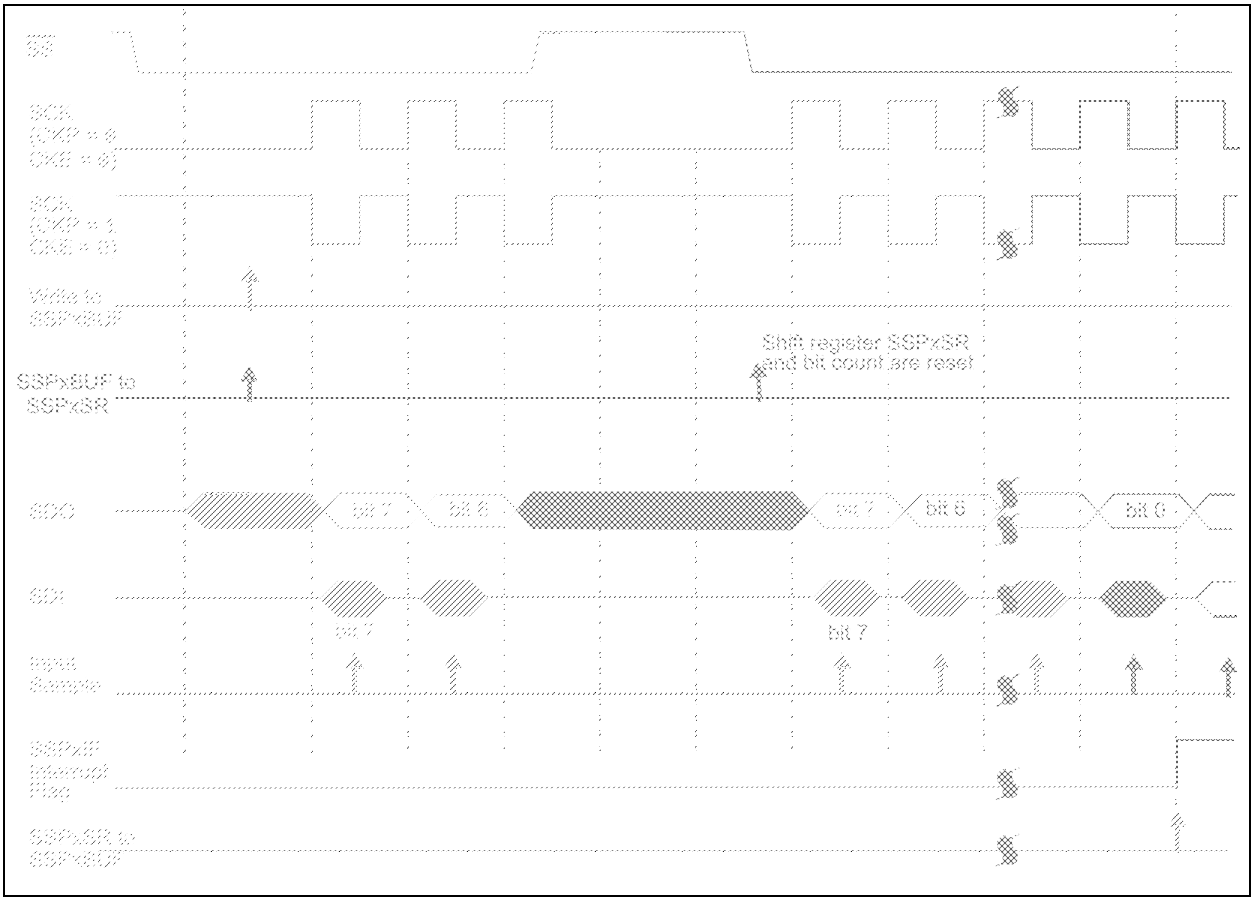
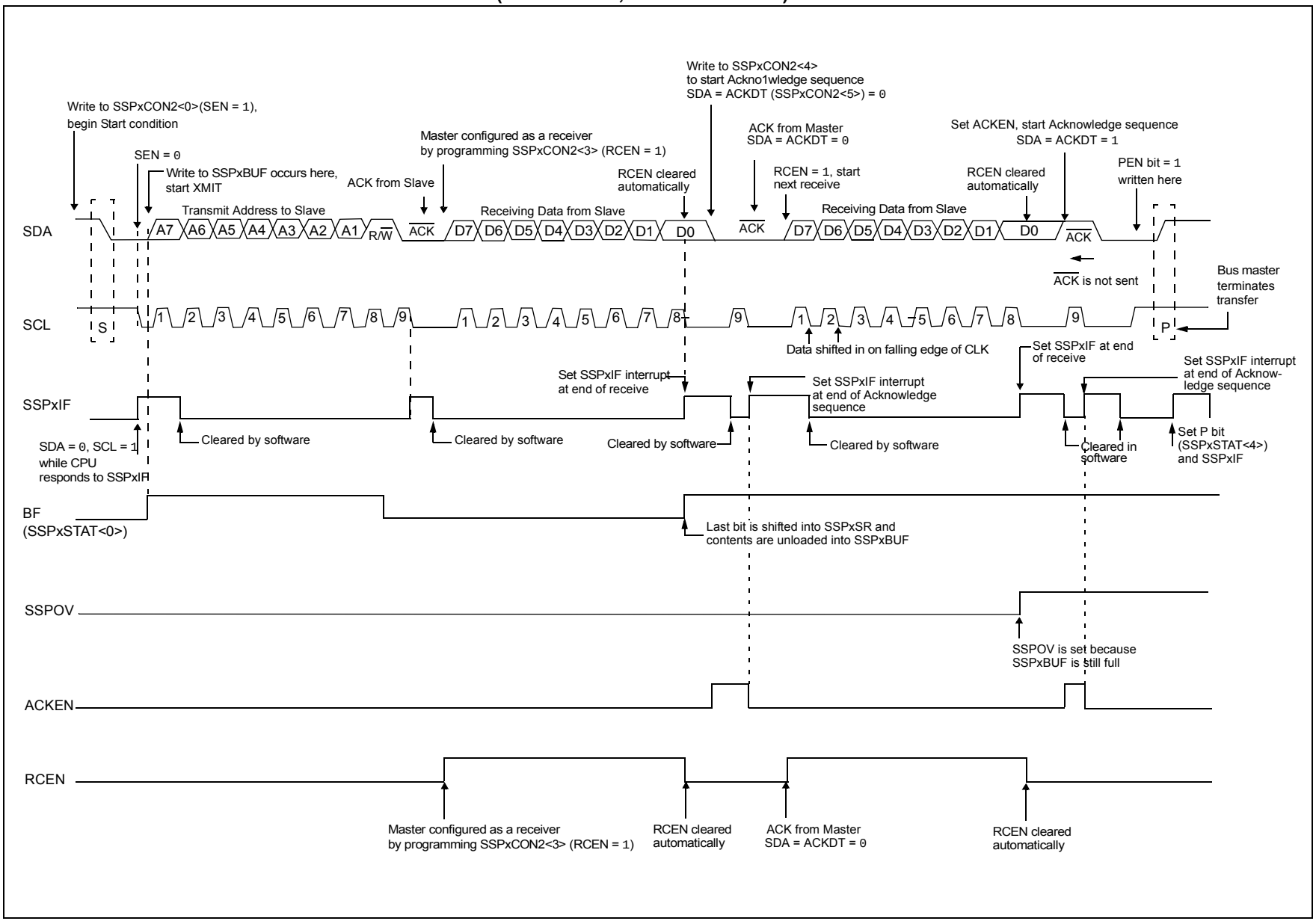


FIGURE 33-29: I^2C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



.

TABLE 35-3: LCDDATAX REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS (28-PIN)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDDATA0	SEG7 COM0	SEG6 COM0	—	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	—	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0
LCDDATA2	SEG23 COM0	SEG22 COM0	—	SEG20 COM0	SEG19 COM0	SEG18 COM0	—	—
LCDDATA3	—	—	—	—	—	—	—	—
LCDDATA4	—	—	—	—	—	—	—	—
LCDDATA5	—	—	—	—	—	—	—	—
LCDDATA6	SEG7 COM1	SEG6 COM1	—	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1
LCDDATA7	SEG15 COM1	SEG14 COM1	SEG13 COM1	—	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1
LCDDATA8	SEG23 COM1	SEG22 COM1	—	SEG20 COM1	SEG19 COM1	SEG18 COM1	—	—
LCDDATA9	—	—	—	—	—	—	—	—
LCDDATA10	—	—	—	—	—	—	—	—
LCDDATA11	—	—	—	—	—	—	—	—
LCDDATA12	SEG7 COM2	SEG6 COM2	—	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2
LCDDATA13	SEG15 COM2	SEG14 COM2	SEG13 COM2	—	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2
LCDDATA14	SEG23 COM2	SEG22 COM2	—	SEG20 COM2	SEG19 COM2	SEG18 COM2	—	—
LCDDATA15	—	—	—	—	—	—	—	—
LCDDATA16	—	—	—	—	—	—	—	—
LCDDATA17	—	—	—	—	—	—	—	—
LCDDATA18	SEG7 COM3	SEG6 COM3	—	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3
LCDDATA19	SEG15 COM3	SEG14 COM3	SEG13 COM3	—	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3
LCDDATA20	SEG23 COM3	SEG22 COM3	—	SEG20 COM3	SEG19 COM3	SEG18 COM3	—	—
LCDDATA21	—	—	—	—	—	—	—	—
LCDDATA22	—	—	—	—	—	—	—	—
LCDDATA23	—	—	—	—	—	—	—	—
LCDDATA24	SEG7 COM4	SEG6 COM4	—	SEG4 COM4	SEG3 COM4	SEG2 COM4	SEG1 COM4	SEG0 COM4
LCDDATA25	SEG15 COM4	SEG14 COM4	SEG13 COM4	—	SEG11 COM4	SEG10 COM4	SEG9 COM4	SEG8 COM4
LCDDATA26	SEG23 COM4	SEG22 COM4	—	SEG20 COM4	SEG19 COM4	SEG18 COM4	—	—
LCDDATA27	—	—	—	—	—	—	—	—
LCDDATA28	—	—	—	—	—	—	—	—
LCDDATA29	—	—	—	—	—	—	—	—
LCDDATA30	SEG7 COM5	SEG6 COM5	—	SEG4 COM5	SEG3 COM5	SEG2 COM5	SEG1 COM5	SEG0 COM5
LCDDATA31	SEG15 COM5	SEG14 COM5	SEG13 COM5	—	SEG11 COM5	SEG10 COM5	SEG9 COM5	SEG8 COM5
LCDDATA32	SEG23 COM5	SEG22 COM5	—	SEG20 COM5	SEG19 COM5	SEG18 COM5	—	—
LCDDATA33	—	—	—	—	—	—	—	—
LCDDATA34	—	—	—	—	—	—	—	—
LCDDATA35	—	—	—	—	—	—	—	—
LCDDATA36	SEG7 COM6	SEG6 COM6	—	SEG4 COM6	SEG3 COM6	SEG2 COM6	SEG1 COM6	SEG0 COM6
LCDDATA37	SEG15 COM6	SEG14 COM6	SEG13 COM6	—	SEG11 COM6	SEG10 COM6	SEG9 COM6	SEG8 COM6
LCDDATA38	SEG23 COM6	SEG22 COM6	—	SEG20 COM6	SEG19 COM6	SEG18 COM6	—	—
LCDDATA39	—	—	—	—	—	—	—	—
LCDDATA40	—	—	—	—	—	—	—	—
LCDDATA41	—	—	—	—	—	—	—	—
LCDDATA42	SEG7 COM7	SEG6 COM7	—	SEG4 COM7	SEG3 COM7	SEG2 COM7	SEG1 COM7	SEG0 COM7
LCDDATA43	SEG15 COM7	SEG14 COM7	SEG13 COM7	—	SEG11 COM7	SEG10 COM7	SEG9 COM7	SEG8 COM7
LCDDATA44	SEG23 COM7	SEG22 COM7	—	SEG20 COM7	SEG19 COM7	SEG18 COM7	—	—
LCDDATA45	—	—	—	—	—	—	—	—
LCDDATA46	—	—	—	—	—	—	—	—
LCDDATA47	—	—	—	—	—	—	—	—

FIGURE 35-12: TYPE-B WAVEFORMS IN 1/2 MUX, 1/3 BIAS DRIVE

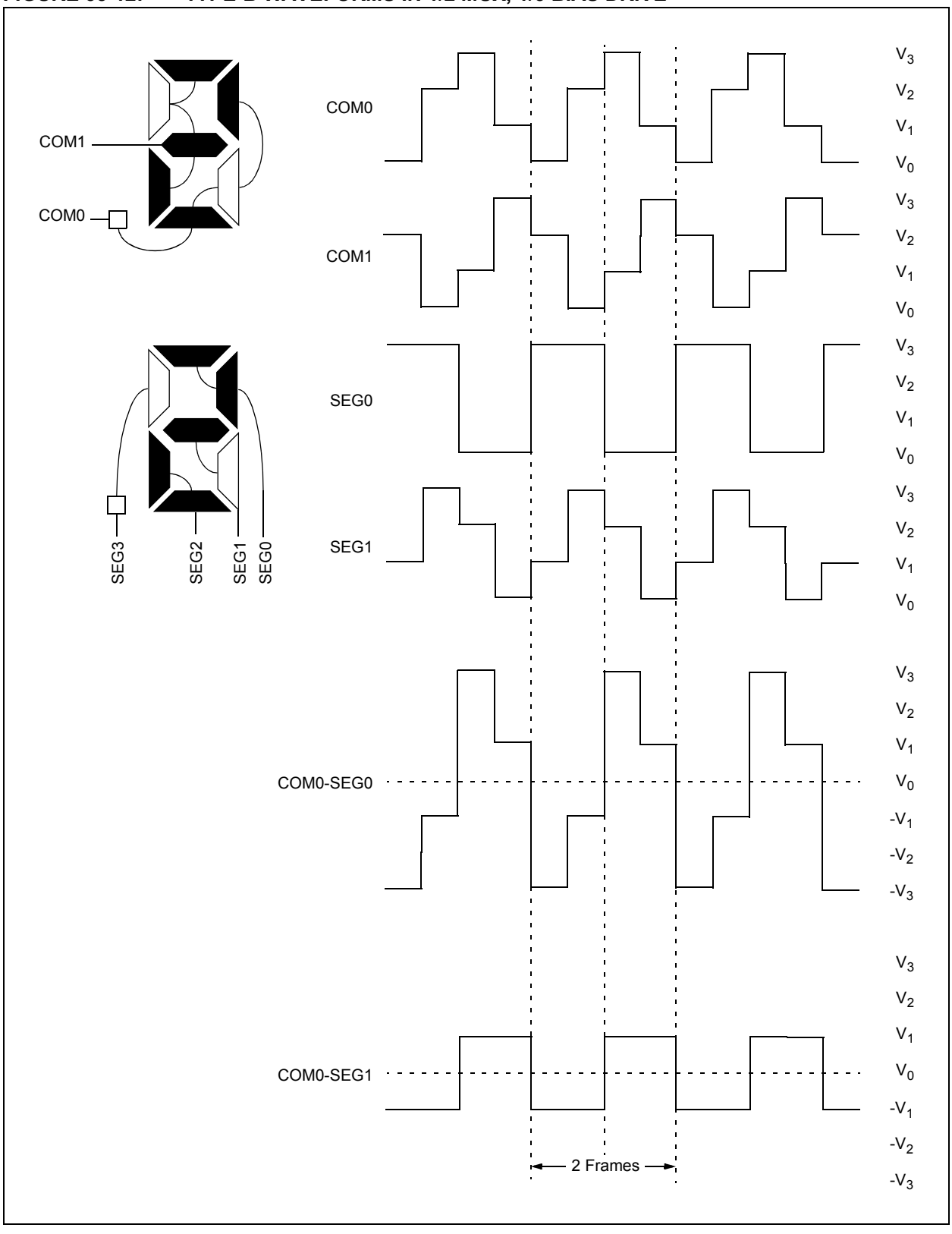


FIGURE 35-15: TYPE-A WAVEFORMS IN 1/3 MUX, 1/3 BIAS DRIVE

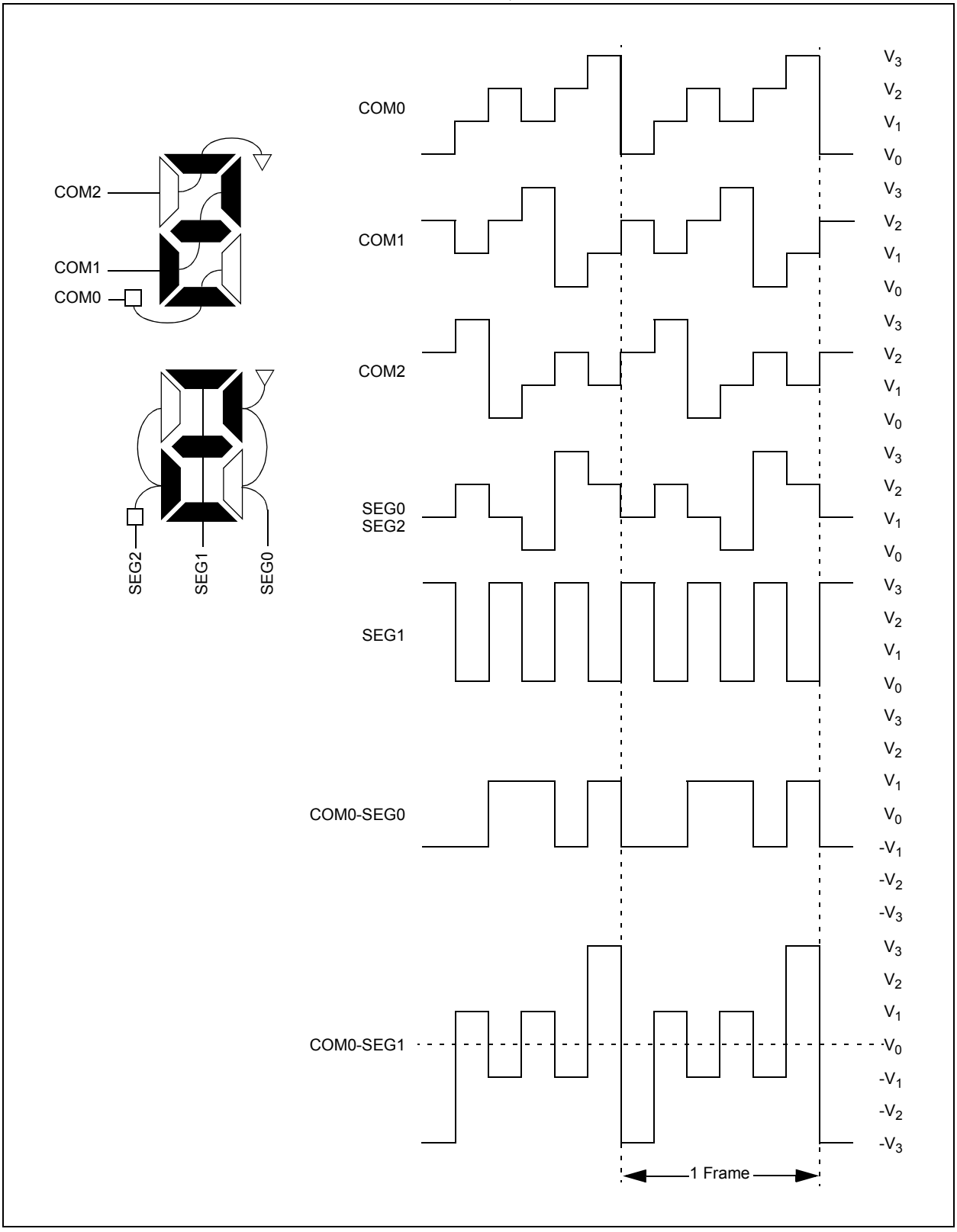


TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1D8Ch — 1D9Fh	—	Unimplemented								
1E0Ch	—	Unimplemented								
1E0Dh	—	Unimplemented								
1E0Eh	—	Unimplemented								
1E0Fh	CLCDATA	—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT	509
1E10h	CLC1CON	LC1EN	—	LC1OUT	LC1INTP	LC1INTN	LC1MODE<2:0>			501
1E11h	CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	502
1E12h	CLC1SEL0	—	—	LC1D1S<5:0>						503
1E13h	CLC1SEL1	—	—	LC1D2S<5:0>						503
1E14h	CLC1SEL2	—	—	LC1D3S<5:0>						503
1E15h	CLC1SEL3	—	—	LC1D4S<5:0>						503
1E16h	CLC1GLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	505
1E17h	CLC1GLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	503
1E18h	CLC1GLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	507
1E19h	CLC1GLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	508
1E1Ah	CLC2CON	LC2EN	—	LC2OUT	LC2INTP	LC2INTN	LC2MODE<2:0>			501
1E1Bh	CLC2POL	LC2POL	—	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	502
1E1Ch	CLC2SEL0	—	—	LC2D1S<5:0>						503
1E1Dh	CLC2SEL1	—	—	LC2D2S<5:0>						503
1E1Eh	CLC2SEL2	—	—	LC2D3S<5:0>						503
1E1Fh	CLC2SEL3	—	—	LC2D4S<5:0>						504
1E20h	CLC2GLS0	LC2G1D4T	LC1G1D4N	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	505
1E21h	CLC2GLS1	LC2G2D4T	LC1G2D4N	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	506
1E22h	CLC2GLS2	LC2G3D4T	LC1G3D4N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	507
1E23h	CLC2GLS3	LC2G4D4T	LC1G4D4N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	508
1E24h	CLC3CON	LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE<2:0>			501
1E25h	CLC3POL	LC3POL	—	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	502
1E26h	CLC3SEL0	—	—	LC3D1S						503
1E27h	CLC3SEL1	—	—	LC3D2S						503
1E28h	CLC3SEL2	—	—	LC3D3S						503
1E29h	CLC3SEL3	—	—	LC3D4S						503
1E2Ah	CLC3GLS0	LC3G1D4T	LC3G1D4N	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	505
1E2Bh	CLC3GLS1	LC3G2D4T	LC3G2D4N	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	506
1E2Ch	CLC3GLS2	LC3G3D4T	LC3G3D4N	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	507
1E2Dh	CLC3GLS3	LC3G4D4T	LC3G4D4N	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	508
1E2Eh	CLC4CON	LC4EN	—	LC4OUT	LC4INTP	LC4INTN	LC4MODE<2:0>			501
1E2Fh	CLC4POL	LC4POL	—	—	—	LC4G4POL	LC4G3POL	LC4G2POL	LC4G1POL	502
1E30h	CLC4SEL0	—	—	LC4D1S<5:0>						503
1E31h	CLC4SEL1	—	—	LC4D2S<5:0>						503
1E32h	CLC4SEL2	—	—	LC4D3S<5:0>						503
1E33h	CLC4SEL3	—	—	LC4D4S<5:0>						503
1E34h	CLC4GLS0	LC4G1D4T	LC4G1D4N	LC4G1D3T	LC4G1D3N	LC4G1D2T	LC4G1D2N	LC4G1D1T	LC4G1D1N	505
1E35h	CLC4GLS1	LC4G2D4T	LC4G2D4N	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	506

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1F33h	—	Unimplemented								
1F34h	—	Unimplemented								
1F35h	—	Unimplemented								
1F36h	—	Unimplemented								
1F37h	—	Unimplemented								
1F38h	ANSELA	ANSA7	ANSA6	—	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	223
1F39h	WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	224
1F3Ah	ODCONA	ODCA7	ODCA6	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	224
1F3Bh	SLRCONA	SLRA7	SLRA6	—	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0	225
1F3Ch	INLVLA	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	225
1F3Dh	IOCAP	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	
1F3Eh	IOCAN	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	
1F3Fh	IOCAF	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	
1F40h	—	Unimplemented								
1F41h	—	Unimplemented								
1F42h	—	Unimplemented								
1F43h	ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	230
1F44h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	231
1F45h	ODCONB	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	231
1F46h	SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	232
1F47h	INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	232
1F48h	IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	277
1F49h	IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	277
1F4Ah	IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	277
1F4Bh	—	Unimplemented								
1F4Ch	—	Unimplemented								
1F4Dh	—	Unimplemented								
1F4Eh	—	Unimplemented								
1F4Fh	WPUC	WPUC7	WPUC6	—	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	236
1F50h	ODCONC	ODCC7	ODCC6	—	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	237
1F51h	SLRCONC	SLRC7	SLRC6	—	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	237
1F52h	INLVLC	INLVLC7	INLVLC6	—	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	238
1F53h	IOCCP	IOCCP7	IOCCP6	—	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	278
1F54h	IOCCN	IOCCN7	IOCCN6	—	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	278
1F55h	IOCCF	IOCCF7	IOCCF6	—	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	278
1F56h	—	Unimplemented								
1F57h	—	Unimplemented								
1F58h	—	Unimplemented								
1F59h	ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	242
1F5Ah	WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	243
1F5Bh	ODCOND	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	243
1F5Ch	SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	244
1F5Dh	INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	244

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.