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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19156t-i-ss

TABLE 1: PIC16(L)F191XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (kW/KB)	DataEE (bytes)	Data SRAM (bytes)	I/O Pins	12-bit ADC (ch)	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer (WWDT)	CCP/10-bit PWM	CWG	CLC	Zero-Cross Detect	Temperature Indicator	Memory Access Partition	Device Information Area	EUSART/ I^2C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug(1)	LCD Segments (Max)	LCD Charge Pump/ Bias Generator
PIC16(L)F19155	**(A)**	8/14	256	1024	24	20	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	96	Y/Y
PIC16(L)F19156	**(A)**	16/28	256	2048	24	20	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	96	Y/Y
PIC16(L)F19175	**(A)**	8/14	256	1024	35	31	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	184	Y/Y
PIC16(L)F19176	**(A)**	16/28	256	2048	35	31	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	184	Y/Y
PIC16(L)F19185	**(A)**	8/14	256	1024	43	39	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	248	Y/Y
PIC16(L)F19186	**(A)**	16/28	256	2048	43	39	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	248	Y/Y
PIC16(L)F19195	**(B)**	8/14	256	1024	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y
PIC16(L)F19196	**(B)**	16/28	256	2048	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y
PIC16(L)F19197	**(B)**	32/56	256	4096	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y

Note 1: I – Debugging integrated on chip.

Data Sheet Index (Unshaded devices are described in this document):

A. Future Release PIC16(L)F19155/56/75/76/85/86 Data Sheet, 28/40/44/48-Pin

B. DS40001873 PIC16(L)F19195/6/7 Data Sheet, Full-Featured 64-Pin Microcontrollers

Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

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TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RC0	15	30	32	34	—	—	—	—	—	T1CKI(1) SMTWIN1(1)	—	—	—	—	—	—	—	—	IOCC0	—	Y	SOSCO
RC1	16	31	35	35	—	—	—	—	—	SMTSIG1(1) T4IN(1)	CCP2(1)	—	—	—	—	—	—	—	IOCC1	—	Y	SOSCI
RC2	17	32	36	36	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM2 SEG18	IOCC2	—	Y	—
RC3	18	33	37	37	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG19	IOCC3	—	Y	—
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG20	IOCC4	—	Y	—
RC6	25	40	44	44	ANC6	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	SEG22 VLCD2	IOCC6	—	Y	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1)	—	—	SEG23 VLCD1	IOCC7	—	Y	—
RD0	19	34	38	38	AND0	—	—	—	—	—	—	—	—	—	—	—	—	SEG24	—	—	Y	—
RD1	20	35	39	39	AND1	—	—	—	—	—	—	—	—	—	—	—	—	SEG25	—	—	Y	—
RD2	21	36	40	40	AND2	—	—	—	—	—	—	—	—	—	—	—	—	COM5 SEG26	—	—	Y	—
RD3	22	37	41	41	AND3	—	—	—	—	—	—	—	—	—	—	—	—	COM4 SEG27	—	—	Y	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	SEG28	—	—	Y	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	SEG29	—	—	Y	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	SEG30	—	—	Y	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	SEG31	—	—	Y	—
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	SEG32	—	—	Y	—
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	COM6 SEG33	—	—	Y	—
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	COM7 SEG34	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	—	Y	$\overline{MCLR}$

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

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2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides three specific device functions:

- Device Reset (when MCLRE = 1)
- Digital input pin (when MCLRE = 0)
- Device Programming and Debugging

If programming and debugging are not required in the end application then either set the MCLRE Configuration bit to '1' and use the pin as a digital input or clear the MCLRE Configuration bit and leave the pin open to use the internal weak pull-up. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, the programmer $\overline{MCLR}/V_{PP}$ output should be connected directly to the pin so that R1 isolates the capacitor, C1 from the $\overline{MCLR}$ pin during programming and debugging operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be isolated from the programmer by resistors between the application and the device pins or removed from the circuit during programming. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/ emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 41.0 "Development Support"**.

1D3Bh	LCDDATA35	1DBBh	—	1E3Bh	RF3PPS(3)	1EBBh	CLCIN0PPS	1F3Bh	SLRCONA	1FBBh	—
1D3Ch	LCDDATA36	1DBCh	—	1E3Ch	RF4PPS(3)	1EBCh	CLCIN1PPS	1F3Ch	INLVLA	1FBCh	—
1D3Dh	LCDDATA37	1DBDh	—	1E3Dh	RF5PPS(3)	1EBDh	CLCIN2PPS	1F3Dh	IOCAP	1FBDh	—
1D3Eh	LCDDATA38	1DBEh	—	1E3Eh	RF6PPS(3)	1EBEh	CLCIN3PPS	1F3Eh	IOCAN	1FBEh	—
1D3Fh	LCDDATA39	1DBFh	—	1E3Fh	RF7PPS(3)	1EBFh	—	1F3Fh	IOCAF	1FBFh	—
1D40h	LCDDATA40	1DC0h	—	1E40h	—	1EC0h	—	1F40h	—	1FC0h	—
1D41h	LCDDATA41	1DC1h	—	1E41h	—	1EC1h	—	1F41h	—	1FC1h	—
1D42h	LCDDATA42	1DC2h	—	1E42h	—	1EC2h	—	1F42h	—	1FC2h	—
1D43h	LCDDATA43	1DC3h	—	1E43h	—	1EC3h	ADCACTPPS	1F43h	ANSELB	1FC3h	—
1D44h	LCDDATA44	1DC4h	—	1E44h	—	1EC4h	—	1F44h	WPUB	1FC4h	—
1D45h	LCDDATA45	1DC5h	—	1E45h	—	1EC5h	SSP1CLKPPS	1F45h	ODCONB	1FC5h	—
1D46h	LCDDATA46	1DC6h	—	1E46h	—	1EC6h	SSP1DATPPS	1F46h	SLRCONB	1FC6h	—
1D47h	LCDDATA47	1DC7h	—	1E47h	—	1EC7h	SSP1SSPPS	1F47h	INLVLB	1FC7h	—
1D48h	—	1DC8h	—	1E48h	—	1EC8h	—	1F48h	IOCBP	1FC8h	—
1D49h	—	1DC9h	—	1E49h	—	1EC9h	—	1F49h	IOCBN	1FC9h	—
1D4Ah	—	1DCAh	—	1E4Ah	—	1ECAh	—	1F4Ah	IOCBF	1FCAh	—
1D4Bh	—	1DCBh	—	1E4Bh	—	1ECBh	RX1PPS	1F4Bh	—	1FCBh	—
1D4Ch	—	1DCCh	—	1E4Ch	—	1ECCh	TX1PPS	1F4Ch	—	1FCCh	—
1D4Dh	—	1DCDh	—	1E4Dh	—	1ECDh	RX2PPS	1F4Dh	—	1FCDh	—
1D4Eh	—	1DCEh	—	1E4Eh	—	1ECEh	TX2PPS	1F4Eh	ANSELC	1FCEh	—
1D4Fh	—	1DCFh	—	1E4Fh	—	1ECFh	—	1F4Fh	WPUC	1FCFh	—
1D50h	—	1DD0h	—	1E50h	ANSELF(3)	1ED0h	—	1F50h	ODCONC	1FD0h	—
1D51h	—	1DD1h	—	1E51h	WPUF(3)	1ED1h	—	1F51h	SLRCONC	1FD1h	—
1D52h	—	1DD2h	—	1E52h	ODCONF(3)	1ED2h	—	1F52h	INLVLC	1FD2h	—
1D53h	—	1DD3h	—	1E53h	SLRCONF(3)	1ED3h	—	1F53h	IOCCP	1FD3h	—
1D54h	—	1DD4h	—	1E54h	INLVLF(3)	1ED4h	—	1F54h	IOCCN	1FD4h	—
1D55h	—	1DD5h	—	1E55h	—	1ED5h	—	1F55h	IOCCF	1FD5h	—
1D56h	—	1DD6h	—	1E56h	—	1ED6h	—	1F56h	—	1FD6h	—
1D57h	—	1DD7h	—	1E57h	—	1ED7h	—	1F57h	—	1FD7h	—
1D58h	—	1DD8h	—	1E58h	—	1ED8h	—	1F58h	—	1FD8h	—
1D59h	—	1DD9h	—	1E59h	—	1ED9h	—	1F59h	ANSELD	1FD9h	—
1D5Ah	—	1DDAh	—	1E5Ah	—	1EDAh	—	1F5Ah	WPUD	1FDAh	—
1D5Bh	—	1DDBh	—	1E5Bh	—	1EDBh	—	1F5Bh	ODCOND	1FDBh	—
1D5Ch	—	1DDCh	—	1E5Ch	—	1EDCh	—	1F5Ch	SLRCOND	1FDCh	—
1D5Dh	—	1DDDh	—	1E5Dh	—	1EDDh	—	1F5Dh	INLVLD	1FDDh	—
1D5Eh	—	1DDEh	—	1E5Eh	—	1EDEh	—	1F5Eh	—	1FDEh	—
1D5Fh	—	1DDFh	—	1E5Fh	—	1EDFh	—	1F5Fh	—	1FDFh	—
1D60h	—	1DE0h	—	1E60h	—	1EE0h	—	1F60h	—	1FE0h	—
1D61h	—	1DE1h	—	1E61h	—	1EE1h	—	1F61h	—	1FE1h	—
1D62h	—	1DE2h	—	1E62h	—	1EE2h	—	1F62h	—	1FE2h	—
1D63h	—	1DE3h	—	1E63h	—	1EE3h	—	1F63h	—	1FE3h	—
1D64h	—	1DE4h	—	1E64h	—	1EE4h	—	1F64h	ANSELE	1FE4h	STATUS_SHAD
1D65h	—	1DE5h	—	1E65h	—	1EE5h	—	1F65h	WPUE	1FE5h	WREG_SHAD
1D66h	—	1DE6h	—	1E66h	—	1EE6h	—	1F66h	ODCONE	1FE6h	BSR_SHAD
1D67h	—	1DE7h	—	1E67h	—	1EE7h	—	1F67h	SLRCONE	1FE7h	PCLATH_SHAD
1D68h	—	1DE8h	—	1E68h	—	1EE8h	—	1F68h	INLVLE	1FE8h	FSR0L_SHAD
1D69h	—	1DE9h	—	1E69h	—	1EE9h	—	1F69h	IOCEP	1FE9h	FSR0H_SHAD
1D6Ah	—	1DEAh	—	1E6Ah	—	1EEAh	—	1F6Ah	IOCEN	1FEAh	FSR1L_SHAD
1D6Bh	—	1DEBh	—	1E6Bh	—	1EEBh	—	1F6Bh	IOCEF	1FEBh	FSR1H_SHAD
1D6Ch	—	1DECh	—	1E6Ch	—	1EECh	—	1F6Ch	—	1FECh	—
1D6Dh	—	1DEDh	—	1E6Dh	—	1EEDh	—	1F6Dh	—	1FEDh	STKPTR

Note 1: Unimplemented locations read as '0'.
2: Present only on PIC16(L)F19156/76/86.
3: Present only on PIC16(L)F19185/86.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 20											
CPU CORE REGISTERS; see Table 4-3 for specifics											
A0Ch	—	Unimplemented								---- ----	---- ----
A0Dh	—	Unimplemented								---- ----	---- ----
A0Eh	—	Unimplemented								---- ----	---- ----
A0Fh	—	Unimplemented								---- ----	---- ----
A10h	—	Unimplemented								---- ----	---- ----
A11h	—	Unimplemented								---- ----	---- ----
A12h	—	Unimplemented								---- ----	---- ----
A13h	—	Unimplemented								---- ----	---- ----
A14h	—	Unimplemented								---- ----	---- ----
A15h	—	Unimplemented								---- ----	---- ----
A16h	—	Unimplemented								---- ----	---- ----
A17h	—	Unimplemented								---- ----	---- ----
A18h	—	Unimplemented								---- ----	---- ----
A19h	RC2REG	RC2REG								0000 0000	0000 0000
A1Ah	TX2REG	TX2REG								0000 0000	0000 0000
A1Bh	SP2BRGL	SP2BRGL								0000 0000	0000 0000
A1Ch	SP2BRGH	SP2BRGH								0000 0000	0000 0000
A1Dh	RC2STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
A1Eh	TX2STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
A1Fh	BAUD2CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

Preliminary

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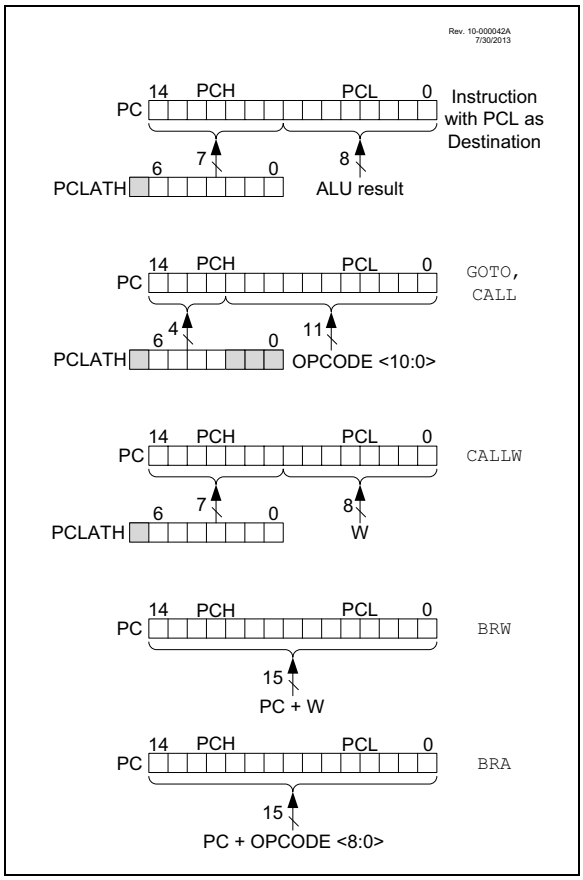
4.4 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 4-3 shows the five situations for the loading of the PC.

FIGURE 4-3: LOADING OF PC IN DIFFERENT SITUATIONS



4.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

4.4.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

4.4.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

4.4.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 + the signed value of the operand of the BRA instruction.

9.6 Register Definitions: Oscillator Control

REGISTER 9-1: OSCCON1: OSCILLATOR CONTROL REGISTER1

U-0	R/W-f/f(1)	R/W-f/f(1)	R/W-f/f(1)	R/W-q/q	R/W-q/q	R/W-q/q	R/W-q/q
—	NOSC<2:0>(2,3)			NDIV<3:0>(2,3,4)			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	f = determined by fuse setting

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **NOSC<2:0>:** New Oscillator Source Request bits
The setting requests a source oscillator and PLL combination per Table 9-1.
POR value = RSTOSC (Register 5-1).

bit 3-0 **NDIV<3:0>:** New Divider Selection Request bits
The setting determines the new postscaler division ratio per Table 9-1.

Note 1: The default value (f/f) is set equal to the RSTOSC Configuration bits.
2: If NOSC is written with a reserved value (Table 9-1), the operation is ignored and neither NOSC nor NDIV is written.
3: When CSWEN = 0, this register is read-only and cannot be changed from the POR value.
4: When NOSC = 110 (HFINTOSC 4 MHz), the NDIV bits will default to '0010' upon Reset; for all other NOSC settings the NDIV bits will default to '0000' upon Reset.

REGISTER 9-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2(1)

U-0	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)
—	COSC<2:0>			CDIV<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **COSC<2:0>:** Current Oscillator Source Select bits (read-only)
Indicates the current source oscillator and PLL combination per Table 9-1.

bit 3-0 **CDIV<3:0>:** Current Divider Select bits (read-only)
Indicates the current postscaler division ratio per Table 9-1.

Note 1: The POR value is the value present when user code execution begins.
2: The Reset value (n/n) is the same as the NOSC/NDIV bits.

REGISTER 11-2: CPUDOZE: DOZE AND IDLE REGISTER

R/W-0/0	R/W/HC/HS-0/0	R/W-0/0	R/W/HC/HS-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
IDLEN	DOZEN(1,2)	ROI	DOE	—	DOZE<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Hardware clear-able HS = Hardware set-able

bit 7 **IDLEN:** Idle Enable bit
1 = A SLEEP instruction places device into Idle mode
0 = A SLEEP instruction places the device into full Sleep mode

bit 6 **DOZEN:** Doze Enable bit(1)
1 = Places the CPU into DOZE mode
0 = Places the CPU into normal mode of operation

bit 5 **ROI:** Recover-on-Interrupt bit(1)
1 = Entering the Interrupt Service Routine (ISR) makes DOZEN = 0
0 = Entering ISR does not change DOZEN

bit 4 **DOE:** Doze on Exit bit(1)
1 = Exiting ISR makes DOZEN = 1
0 = Exiting ISR does not change DOZEN

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DOZE<2:0>:** Ratio of CPU Instruction Cycles to Peripheral Instruction Cycles
111 =1:256
110 =1:128
101 =1:64
100 =1:32
011 =1:16
010 =1:8
001 =1:4
000 =1:2

Note 1: Refer to Table 11-1 for more information.

REGISTER 19-3: ADCON2: ADC CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0	R/W-0/0	R/W-0/0	R/W-0/0
PSIS	CRS<2:0>			ACLR	MD<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **PSIS:** ADC Previous Sample Input Select bits
1 = PREV is the FLTR value at start-of-conversion
0 = PREV is the RES value at start-of-conversion

bit 6-4 **CRS<2:0>:** ADC Accumulated Calculation Right Shift Select bits
If ADMD = 100:
Low-pass filter time constant is 2^{ADCRS}, filter gain is 1:1
If ADMD = 001, 010 or 011:
The accumulated value is right-shifted by CRS (divided by 2^{ADCRS})**(1,2)**
Otherwise:
Bits are ignored

bit 3 **ACLR:** A/D Accumulator Clear Command bit**(3)**
1 = ACC, AOV and CNT registers are cleared
0 = Clearing action is complete (or not started)

bit 2-0 **MD<2:0>:** ADC Operating Mode Selection bits**(4)**
111-101 = Reserved
100 = Low-pass Filter mode
011 = Burst Average mode
010 = Average mode
001 = Accumulate mode
000 = Basic mode

Note 1: To correctly calculate an average, the number of samples (set in RPT) must be 2^{ADCRS}.
2: ADCRS = 3'b111 is a reserved option.
3: This bit is cleared by hardware when the accumulator operation is complete; depending on oscillator selections, the delay may be many instructions.
4: See Table 19-2 for Full mode descriptions.

22.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Programmable input selection
- Selectable voltage reference
- Programmable output polarity
- Rising/falling output edge interrupts
- Programmable Speed/Power optimization
- CWG1 Auto-shutdown source

22.1 Comparator Overview

A single comparator is shown in Figure 22-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available are shown in Table 22-1.

TABLE 22-1: AVAILABLE COMPARATORS

Device	C1	C2
PIC16(L)F19155/56/75/76/85/86	•	•

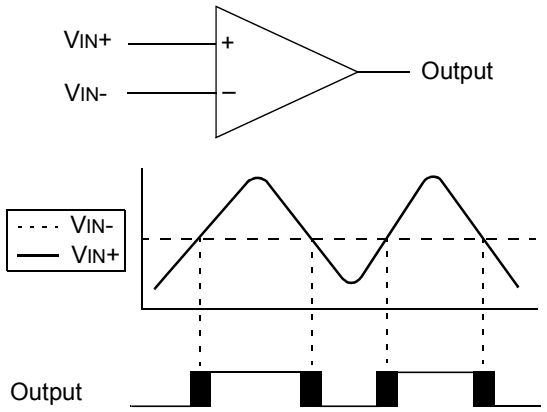
22.2 C2 Low-Power Clocked Comparator

C2 is a low-power LFINTOSC clocked comparator. On each rising edge of LFINTOSC the output state of the comparator is updated based on the states of the comparator inputs.

22.2.1 LOW POWER REFERENCE

C2 has access to a low power reference source (3.072V) used by the LCD module. If the lowest power operation is desired and a highest variation of tolerance is acceptable, the user can choose the C2 Low-Power Clocked Comparator with the LCD VREF as a positive channel input (see Comparator Positive Input Channel Select bits PCH<2:0>). See **Section 18.0 "Fixed Voltage Reference (FVR)"** for additional details.

FIGURE 22-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

24.1.3 CLOCK SOURCES

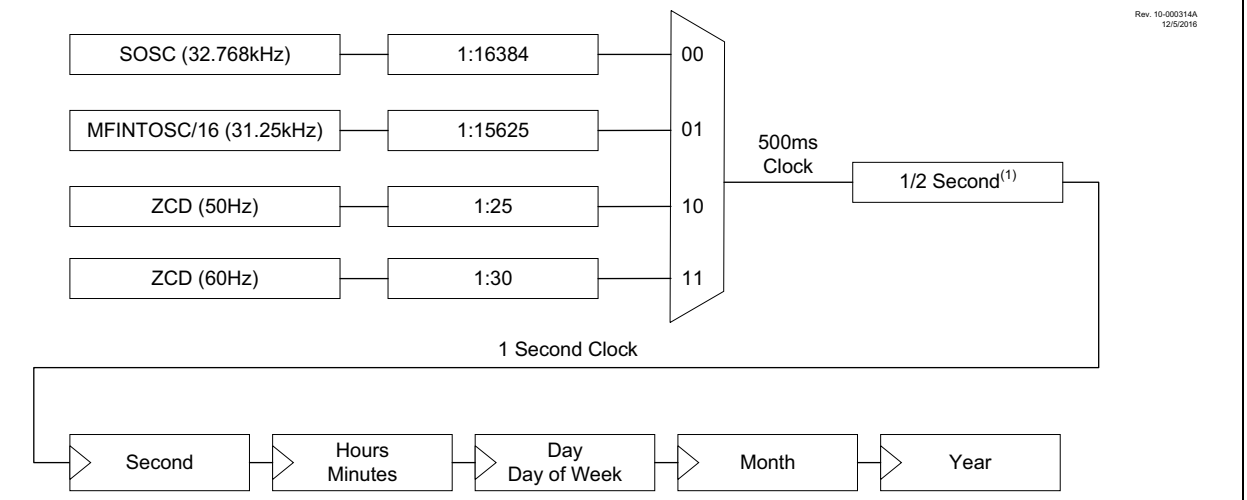
The RTCC module can be clocked by either an external Real-Time Clock crystal oscillating at 32.768 kHz, MFINTOSC/16 (31.25 kHz) or via the ZCD at 50 Hz or 60 Hz. Each clock selection has a fixed prescaler in order to generate the required half-second clock needed by the RTCC. They are as following:

- SOSC (32.768 kHz) = 1:16384
- MFINTOSC/16 (31.25 kHz) = 1:15625
- ZCD (50 Hz) = 1:25
- ZCD (60 Hz) = 1:30

Note:	The accuracy of the oscillator is not the same as a crystal. Refer to Figure 39-6 for more details.

Calibration of the RTCC can be performed to yield an error of three seconds or less per month (see **Section 24.1.7 "Calibration"** for further details).

FIGURE 24-4: CLOCK SOURCE MULTIPLEXING



Note 1: Writing to the SECONDS register resets all counters, allowing for fraction of a second synchronization.

24.1.4 DIGIT CARRY RULES

This section explains which timer values are affected when there is a rollover.

- Time of Day: From 23:59:59 to 00:00:00 with a carry to the Day and Weekday field
- Month: From 12/31 to 01/01 with a carry to the Year field
- Day of Week: From 6 to 0 with no carry (see Table 24-1)
- Year Carry: From 99 to 00; this also surpasses the use of the RTCC

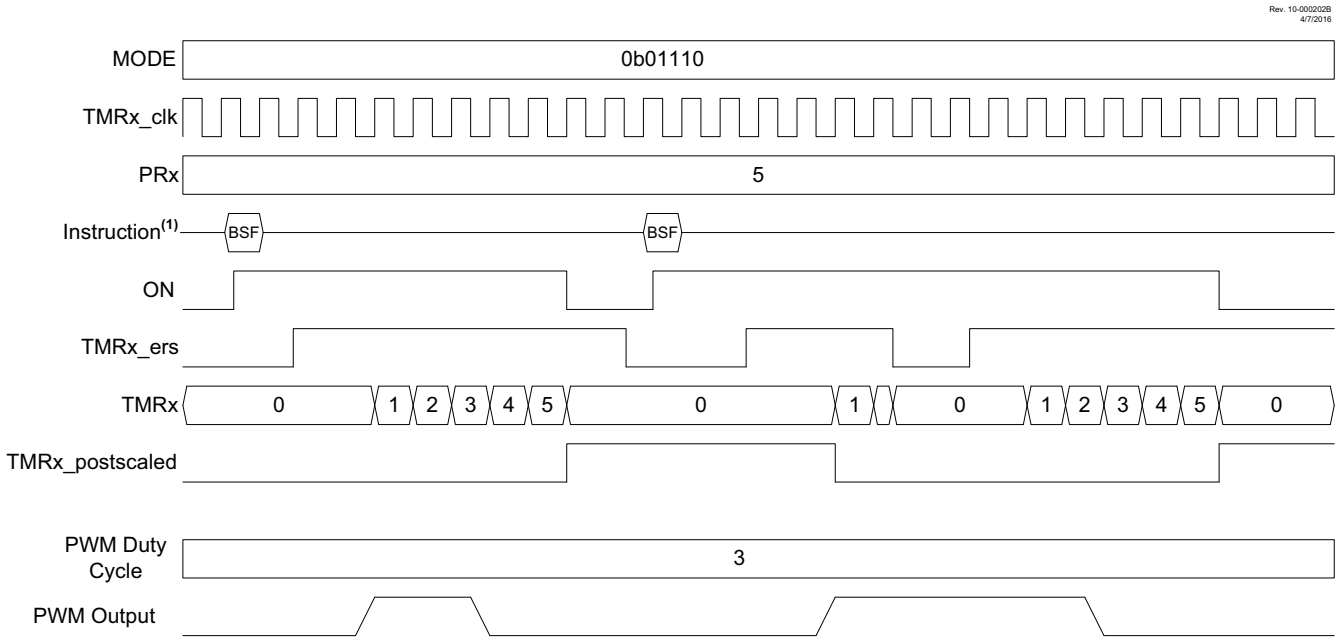
For the day to month rollover schedule, see Table 24-2.

Because the values are in BCD format, the carry to the upper BCD digit will occur at a count of 10 and not at 16 (SECONDS, MINUTES, HOURS, WEEKDAY, DAYS and MONTHS).

TABLE 24-1: DAY OF WEEK SCHEDULE

Day of Week	
Sunday	0
Monday	1
Tuesday	2
Wednesday	3
Thursday	4
Friday	5
Saturday	6

FIGURE 27-11: LOW LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01110)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

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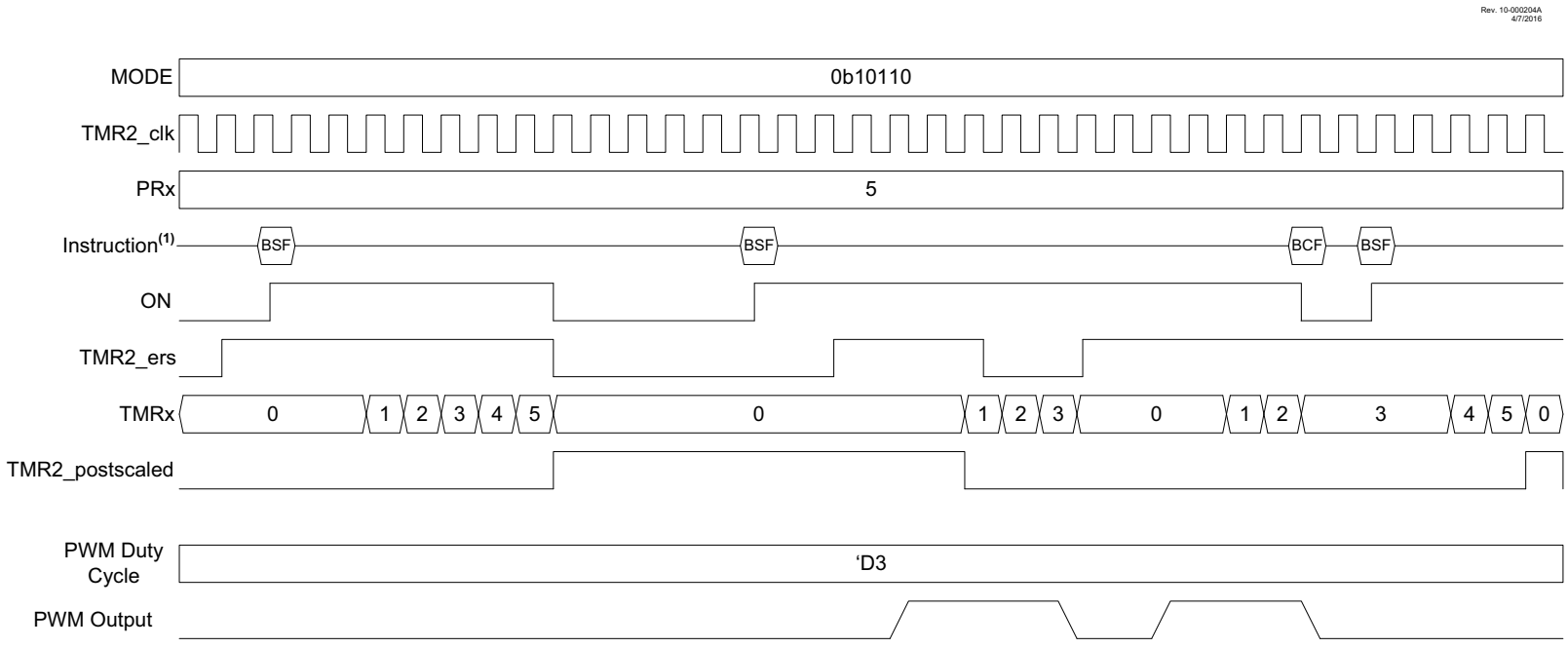
FIGURE 27-13: LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 10110)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

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REGISTER 28-3: SMTxSTAT: SMT STATUS REGISTER

R/W/HC-0/0	R/W/HC-0/0	R/W/HC-0/0	U-0	U-0	R-0/0	R-0/0	R-0/0
CPRUP	CPWUP	RST	—	—	TS	WS	AS
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **CPRUP:** SMT Manual Period Buffer Update bit
1 = Request update to SMTxCPRx registers
0 = SMTxCPRx registers update is complete

bit 6 **CPWUP:** SMT Manual Pulse Width Buffer Update bit
1 = Request update to SMTxCPW registers
0 = SMTxCPW registers update is complete

bit 5 **RST:** SMT Manual Timer Reset bit
1 = Request Reset to SMTxTMR registers
0 = SMTxTMR registers update is complete

bit 4-3 **Unimplemented**: Read as ‘0’

bit 2 **TS:** SMT GO Value Status bit
1 = SMT timer is incrementing
0 = SMT timer is not incrementing

bit 1 **WS:** SMTxWIN Value Status bit
1 = SMT window is open
0 = SMT window is closed

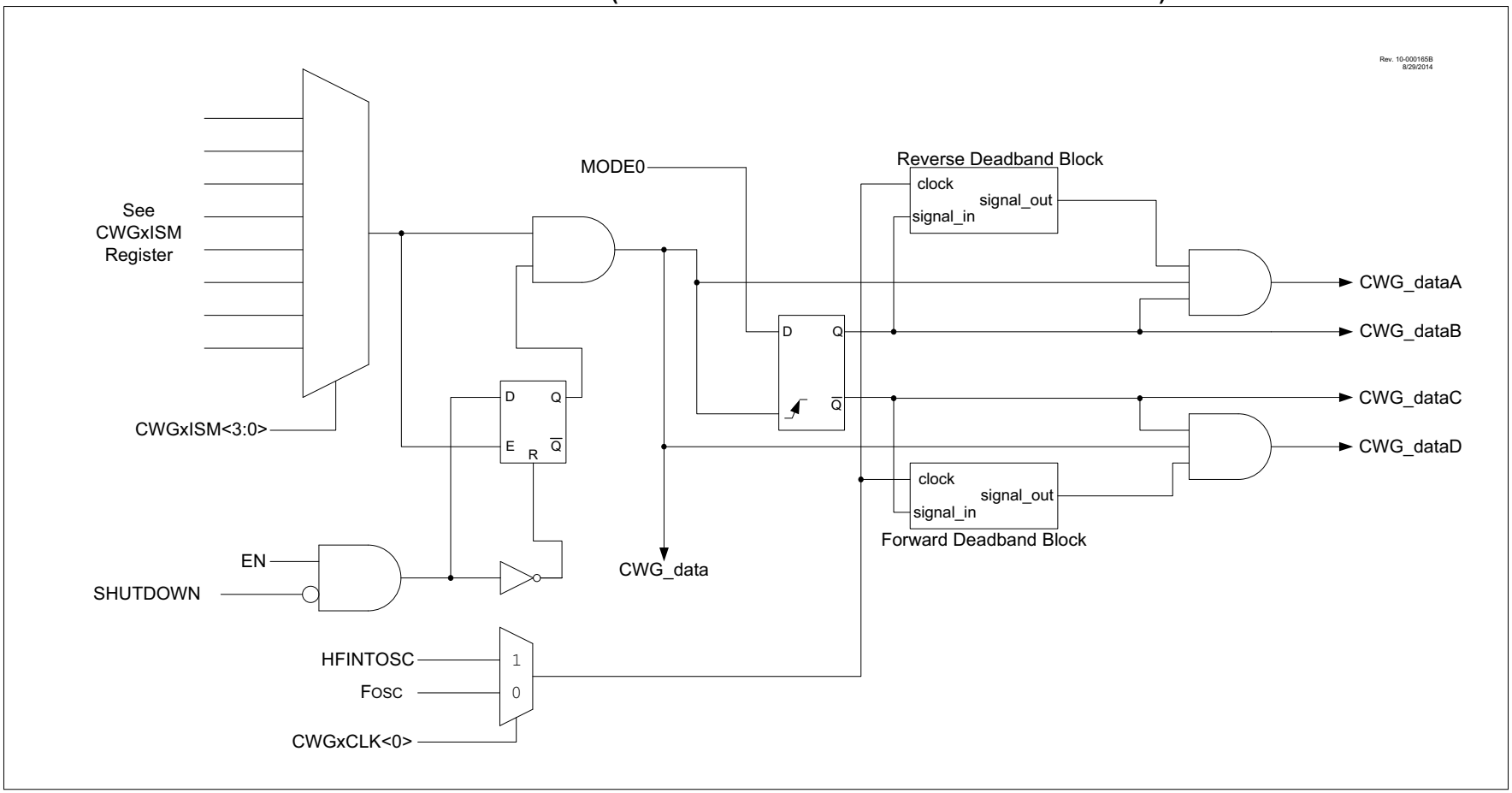
bit 0 **AS:** SMT_signal Value Status bit
1 = SMT acquisition is in progress
0 = SMT acquisition is not in progress

TABLE 29-5: SUMMARY OF REGISTERS ASSOCIATED WITH CCPx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIR4	—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF	178
PIE4	—	—	—	—	TMR4IE	—	TMR2IE	TMR1IE	169
CCP1CON	EN	—	OUT	FMT	MODE<3:0>				458
CCP1CAP	—	—	—	—	—	CTS<2:0>			460
CCPR1L	Capture/Compare/PWM Register 1 (LSB)								460
CCPR1H	Capture/Compare/PWM Register 1 (MSB)								461
CCP2CON	EN	—	OUT	FMT	MODE<3:0>				458
CCP2CAP	—	—	—	—	—	CTS<2:0>			460
CCPR2L	Capture/Compare/PWM Register 1 (LSB)								460
CCPR2H	Capture/Compare/PWM Register 1 (MSB)								460
CCPTMRS0	P4TSEL<1:0>		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		461
CCP1PPS	—	—	—	CCP1PPS<4:0>					264
CCP2PPS	—	—	—	CCP2PPS<4:0>					264
RxyPPS	—	—	—	RxyPPS<4:0>					265
ADACT	—	—	—	ACT<4:0>					323
CLCxSELy	—	—	—	LCxDyS<4:0>					503
CWG1ISM	—	—	—	—	IS<3:0>				492

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the CCPx module.

FIGURE 31-3: SIMPLIFIED CWG BLOCK DIAGRAM (FORWARD AND REVERSE FULL-BRIDGE MODES)



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31.12 Configuring the CWG

The following steps illustrate how to properly configure the CWG.

1. Ensure that the TRIS control bits corresponding to the desired CWG pins for your application are set so that the pins are configured as inputs.
2. Clear the EN bit, if not already cleared.
3. Set desired mode of operation with the MODE bits.
4. Set desired dead-band times, if applicable to mode, with the CWG1DBR and CWG1DBF registers.
5. Setup the following controls in the CWG1AS0 and CWG1AS1 registers.
   a. Select the desired shutdown source.
   b. Select both output overrides to the desired levels (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
   c. Set which pins will be affected by auto-shutdown with the CWG1AS1 register.
   d. Set the SHUTDOWN bit and clear the REN bit.
6. Select the desired input source using the CWG1ISM register.
7. Configure the following controls.
   a. Select desired clock source using the CWG1CLKCON register.
   b. Select the desired output polarities using the CWG1CON1 register.
   c. Set the output enables for the desired outputs.
8. Set the EN bit.
9. Clear TRIS control bits corresponding to the desired output pins to configure these pins as outputs.
10. If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit to start the CWG.

31.12.1 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown input is true, are controlled by the LSBD and LSAC bits of the CWG1AS0 register. LSBD<1:0> controls the CWG1B and D override levels and LSAC<1:0> controls the CWG1A and C override levels. The control bit logic level corresponds to the output logic drive level while in the shutdown state. The polarity control does not affect the override level.

31.12.2 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the REN bit of the CWG1CON2 register. Waveforms of software controlled and automatic restarts are shown in Figure 31-13 and Figure 31-14.

31.12.2.1 Software Controlled Restart

When the REN bit of the CWG1AS0 register is cleared, the CWG must be restarted after an auto-shutdown event by software. Clearing the shutdown state requires all selected shutdown inputs to be low, otherwise the SHUTDOWN bit will remain set. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

31.12.2.2 Auto-Restart

When the REN bit of the CWG1CON2 register is set, the CWG will restart from the auto-shutdown state automatically. The SHUTDOWN bit will clear automatically when all shutdown sources go low. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

TABLE 35-4: LCDDATAX REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS (40/44-PIN)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDDATA0	SEG7 COM0	SEG6 COM0	—	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	—	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0
LCDDATA2	SEG23 COM0	SEG22 COM0	—	SEG20 COM0	SEG19 COM0	SEG18 COM0	—	—
LCDDATA3	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
LCDDATA4	—	—	—	—	—	SEG34 COM0	SEG33 COM0	SEG32 COM0
LCDDATA5	—	—	—	—	—	—	—	—
LCDDATA6	SEG7 COM1	SEG6 COM1	—	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1
LCDDATA7	SEG15 COM1	SEG14 COM1	SEG13 COM1	—	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1
LCDDATA8	SEG23 COM1	SEG22 COM1	—	SEG20 COM1	SEG19 COM1	SEG18 COM1	—	—
LCDDATA9	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
LCDDATA10	—	—	—	—	—	SEG34 COM1	SEG33 COM1	SEG32 COM1
LCDDATA11	—	—	—	—	—	—	—	—
LCDDATA12	SEG7 COM2	SEG6 COM2	—	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2
LCDDATA13	SEG15 COM2	SEG14 COM2	SEG13 COM2	—	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2
LCDDATA14	SEG23 COM2	SEG22 COM2	—	SEG20 COM2	SEG19 COM2	SEG18 COM2	—	—
LCDDATA15	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
LCDDATA16	—	—	—	—	—	SEG34 COM2	SEG33 COM2	SEG32 COM2
LCDDATA17	—	—	—	—	—	—	—	—
LCDDATA18	SEG7 COM3	SEG6 COM3	—	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3
LCDDATA19	SEG15 COM3	SEG14 COM3	SEG13 COM3	—	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3
LCDDATA20	SEG23 COM3	SEG22 COM3	—	SEG20 COM3	SEG19 COM3	SEG18 COM3	—	—
LCDDATA21	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3
LCDDATA22	—	—	—	—	—	SEG34 COM3	SEG33 COM3	SEG32 COM3
LCDDATA23	—	—	—	—	—	—	—	—
LCDDATA24	SEG7 COM4	SEG6 COM4	—	SEG4 COM4	SEG3 COM4	SEG2 COM4	SEG1 COM4	SEG0 COM4
LCDDATA25	SEG15 COM4	SEG14 COM4	SEG13 COM4	—	SEG11 COM4	SEG10 COM4	SEG9 COM4	SEG8 COM4
LCDDATA26	SEG23 COM4	SEG22 COM4	—	SEG20 COM4	SEG19 COM4	SEG18 COM4	—	—
LCDDATA27	SEG31 COM4	SEG30 COM4	SEG29 COM4	SEG28 COM4	SEG27 COM4	SEG26 COM4	SEG25 COM4	SEG24 COM4
LCDDATA28	—	—	—	—	—	SEG34 COM4	SEG33 COM4	SEG32 COM4
LCDDATA29	—	—	—	—	—	—	—	—
LCDDATA30	SEG7 COM5	SEG6 COM5	—	SEG4 COM5	SEG3 COM5	SEG2 COM5	SEG1 COM5	SEG0 COM5
LCDDATA31	SEG15 COM5	SEG14 COM5	SEG13 COM5	—	SEG11 COM5	SEG10 COM5	SEG9 COM5	SEG8 COM5
LCDDATA32	SEG23 COM5	SEG22 COM5	—	SEG20 COM5	SEG19 COM5	SEG18 COM5	—	—
LCDDATA33	SEG31 COM5	SEG30 COM5	SEG29 COM5	SEG28 COM5	SEG27 COM5	SEG26 COM5	SEG25 COM5	SEG24 COM5
LCDDATA34	—	—	—	—	—	SEG34 COM5	SEG33 COM5	SEG32 COM5
LCDDATA35	—	—	—	—	—	—	—	—
LCDDATA36	SEG7 COM6	SEG6 COM6	—	SEG4 COM6	SEG3 COM6	SEG2 COM6	SEG1 COM6	SEG0 COM6
LCDDATA37	SEG15 COM6	SEG14 COM6	SEG13 COM6	—	SEG11 COM6	SEG10 COM6	SEG9 COM6	SEG8 COM6
LCDDATA38	SEG23 COM6	SEG22 COM6	—	SEG20 COM6	SEG19 COM6	SEG18 COM6	—	—
LCDDATA39	SEG31 COM6	SEG30 COM6	SEG29 COM6	SEG28 COM6	SEG27 COM6	SEG26 COM6	SEG25 COM6	SEG24 COM6
LCDDATA40	—	—	—	—	—	SEG34 COM6	SEG33 COM6	SEG32 COM6
LCDDATA41	—	—	—	—	—	—	—	—
LCDDATA42	SEG7 COM7	SEG6 COM7	—	SEG4 COM7	SEG3 COM7	SEG2 COM7	SEG1 COM7	SEG0 COM7
LCDDATA43	SEG15 COM7	SEG14 COM7	SEG13 COM7	—	SEG11 COM7	SEG10 COM7	SEG9 COM7	SEG8 COM7
LCDDATA44	SEG23 COM7	SEG22 COM7	—	SEG20 COM7	SEG19 COM7	SEG18 COM7	—	—
LCDDATA45	SEG31 COM7	SEG30 COM7	SEG29 COM7	SEG28 COM7	SEG27 COM7	SEG26 COM7	SEG25 COM7	SEG24 COM7
LCDDATA46	—	—	—	—	—	SEG34 COM7	SEG33 COM7	SEG32 COM7
LCDDATA47	—	—	—	—	—	—	—	—

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
C0Ch	RTCCON	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	—	RTCCLKSEL<1:0>		357
C0Dh	RTCCAL	CAL								358
C0Eh	ALRMCON	ALRMEN	CHIME	AMASK<3:0>				—	—	361
C0Fh	ALRMRPT	ARPT								361
C10h	YEAR	YEARH<3:0>				YEARL<3:0>				358
C11h	MONTH	—	—	—	MONTHH	MONTHL<3:0>				358
C12h	WEEKDAY	—	—	—	—	—	WDAY<2:0>			359
C13h	DAY	—	—	DAYH<1:0>		DAYL<3:0>				359
C14h	HOURS	—	—	HRH<1:0>		HRL<3:0>				359
C15h	MINUTES	—	MINH<2:0>			MINL<3:0>				360
C16h	SECONDS	—	SECH<2:0>			SECL<3:0>				360
C17h	ALRMMTH	—	—	—	ALRMH-MONTH	ALRMLMONTH <3:0>				362
C18h	ALRMWD	—	—	—	—	—	ALRMLWDAY<2:0>			362
C19h	ALRMDAY	—	—	ALRMHDAY<1:0>		ALRMLDAY<3:0>				362
C1Ah	ALRMHR	—	—	ALRMHHR<1:0>		ALRMLHR<3:0>				363
C1Bh	ALRMMIN	—	ALRMHMIN<2:0>			ALRMLMIN<3:0>				363
C1Ch	ALRMSEC	—	ALRMHSEC<2:0>			ALRMLSEC<3:0>				363
C1Dh	—	Unimplemented								
C1Eh	—	Unimplemented								
C1Fh	—	Unimplemented								
C8Ch	—	Unimplemented								
C8Dh	—	Unimplemented								
C8Eh	—	Unimplemented								
C8Fh	—	Unimplemented								
C90h	—	Unimplemented								
C91h	—	Unimplemented								
C92h	—	Unimplemented								
C93h	—	Unimplemented								
C94h	—	Unimplemented								
C95h	—	Unimplemented								
C96h	—	Unimplemented								
C97h	—	Unimplemented								
C98h	—	Unimplemented								
C99h	—	Unimplemented								
C9Ah	—	Unimplemented								
C9Bh	—	Unimplemented								
C9Ch	—	Unimplemented								
C9Dh	—	Unimplemented								
C9Eh	—	Unimplemented								
C9Fh	—	Unimplemented								
D0Ch — D1Fh	—	Unimplemented								
D8Ch — D9Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

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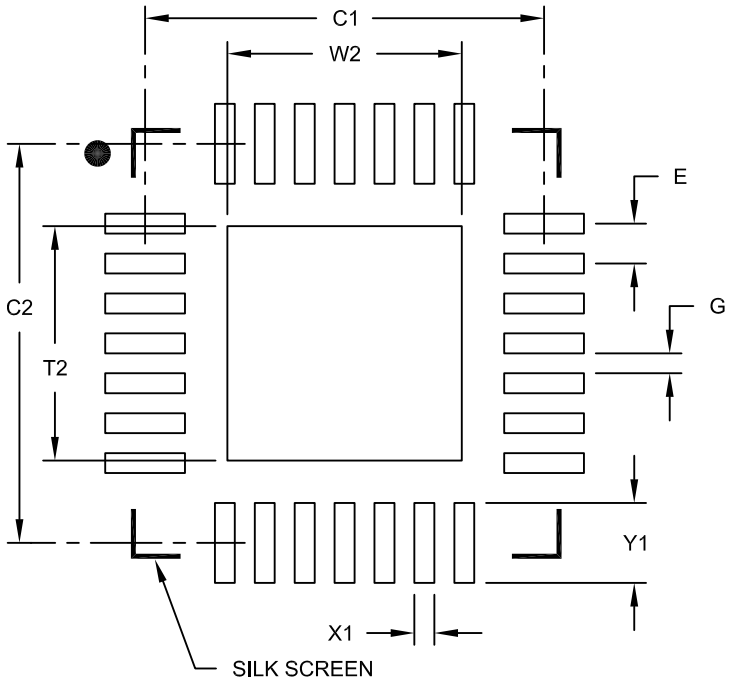
28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			2.35
Optional Center Pad Length	T2			2.35
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2152A