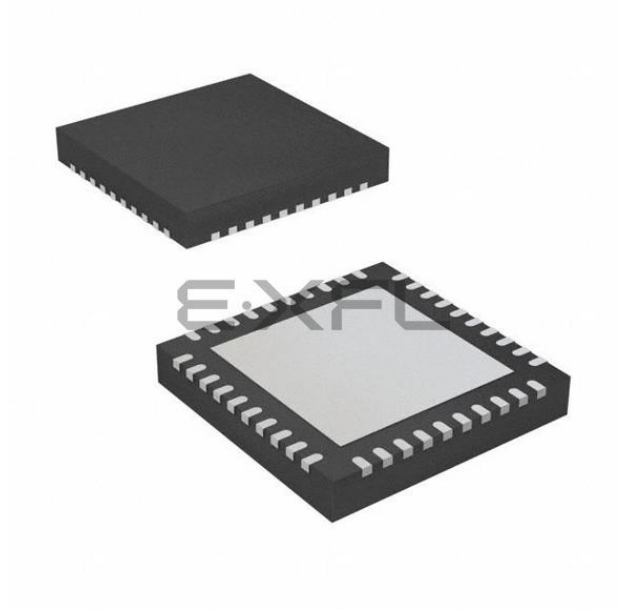

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 31x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19175-e-mv

TABLE 1-2: PIC16(L)F19155/56 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/C1IN0-/C2IN0-/ANA0/CLCIN0(1)/IOCA0/SEG0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0-	AN		Comparator negative input.
	C2IN0-	AN		Comparator negative input.
	ANA0	AN		ADC Channel input.
	CLCIN0(1)	—		Configurable Logic Cell source input.
	IOCA0	TTL/ST		Interrupt-on-change input.
	SEG0	—	AN	LCD Analog output.
RA1/C1IN1-/C2IN1-/ANA1/CLCIN1(1)/SEG1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN1-	AN		Comparator negative input.
	C2IN1-	AN		Comparator negative input.
	ANA1	AN		ADC Channel input.
	CLCIN1(1)	—		Configurable Logic Cell source input.
	IOCA1	TTL/ST		Interrupt-on-change input.
	SEG1	—	AN	LCD Analog output.
RA2/C1IN0+/C2IN0+/ANA2/DAC1OUT1/IOCA2/SEG2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN0+	AN	—	Comparator positive input.
	C2IN0+	AN	—	Comparator positive input.
	ANA2	AN	—	ADC Channel input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
	SEG2	—	AN	LCD Analog output.
RA3/C1IN1+/ANA3/SEG3/IOCA3/VREF+ (ADC)/VREF+ (DAC1)	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	C1IN1+	AN	—	Comparator positive input.
	ANA3	AN	—	ADC Channel input.
	SEG3	—	AN	LCD Analog output.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
	VREF+ (ADC)	AN	—	ADC positive reference.
	VREF+ (DAC1)	AN	—	DAC positive reference.
RA4/ANA4/T0CKI(1)/IOCA4/SEG4/COM3	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel input.
	T0CKI(1)	—	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
	SEG4	—	AN	LCD Analog output.
	COM3	—	AN	LCD Driver Common Outputs.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input' ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 1-4: PIC16(L)F19185/86 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Types	Output Types	Description
RC6/CK1(3)/TX1(1)/IOCC6/ANC6/SEG22/VLCD2	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	CK1(3)	—	—	EUSART synchronous clock out
	TX1(1)	—	—	EUSART asynchronous TX data out
	IOCC6	TTL/ST	—	Interrupt-on-change input.
	ANC6	AN	—	ADC Channel input.
	SEG22	—	AN	LCD Analog output.
	VLCD2	AN	—	LCD analog input
RC7/DT1(3)/RX1(1)/IOCC7/ANC7/SEG23/VLCD1	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	DT1(3)	—	—	EUSART synchronous data output
	RX1(1)	—	—	EUSART receive input.
	IOCC7	TTL/ST	—	Interrupt-on-change input.
	ANC7	AN	—	ADC Channel input.
	SEG23	—	AN	LCD Analog output.
	VLCD1	AN	—	LCD analog input
RD0/AND0/SEG24	RD0	TTL/ST	CMOS/OD	General purpose I/O.
	AND0	AN	—	ADC Channel input.
	SEG24	AN	—	LCD Analog output.
RD1/AND1/SEG25	RD1	TTL/ST	CMOS/OD	General purpose I/O.
	AND1	AN	—	ADC Channel input.
	SEG25	—	AN	LCD Analog output.
RD2/AND2/COM5	RD2	TTL/ST	CMOS/OD	General purpose I/O.
	AND2	AN	—	ADC Channel input.
	SEG26	—	AN	LCD Analog output.
	COM5	—	AN	LCD Driver Common Outputs.
RD3/AND3/SEG27/COM4	RD3	TTL/ST	CMOS/OD	General purpose I/O.
	AND3	AN	—	ADC Channel input.
	SEG27	—	AN	LCD Analog output.
	COM4	—	AN	LCD Driver Common Outputs.
RD4/AND4/SEG28	RD4	TTL/ST	CMOS/OD	General purpose I/O.
	AND4	AN	—	ADC Channel input.
	SEG28	—	AN	LCD Analog output.
RD5/AND5/SEG29	RD5	TTL/ST	CMOS/OD	General purpose I/O.
	AND5	AN	—	ADC Channel input.
	SEG29	AN	—	LCD Analog output.
RD6/AND6/SEG30	RD6	TTL/ST	CMOS/OD	General purpose I/O.
	AND6	AN	—	ADC Channel input.
	SEG30	—	AN	LCD Analog output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input'; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 19											
CPU CORE REGISTERS; see Table 4-3 for specifics											
98Ch	—	Unimplemented								---- ----	---- ----
98Dh	—	Unimplemented								---- ----	---- ----
98Eh	—	Unimplemented								---- ----	---- ----
98Fh	CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	0000 0000	0000 0000
990h	CM1CON0	ON	OUT	—	POL	—	—	HYS	SYNC	00-0 --00	00-0 --00
991h	CM1CON1	—	—	—	—	—	—	INTP	INTN	0000 0000	0000 0000
992h	CM1NSEL	—	—	—	—	—	NCH<2:0>			0000 0000	0000 0000
992h		—	—	—	—	—	NCH2	NCH1	NCH0	0000 0000	0000 0000
993h	CM1PSEL	—	—	—	—	PCH<3:0>				0000 0000	0000 0000
993h		—	—	—	—	—	PCH2	PCH1	PCH0	0000 0000	0000 0000
994h	CM2CON0	ON	OUT	—	POL	—	—	HYS	SYNC	00-0 --00	00-0 --00
995h	CM2CON1	—	—	—	—	—	—	INTP	INTN	0000 0000	0000 0000
996h	CM2NSEL	—	—	—	—	—	NCH<2:0>			0000 0000	0000 0000
996h		—	—	—	—	—	NCH2	NCH1	NCH0	0000 0000	0000 0000
997h	CM2PSEL	—	—	—	—	—	PCH<2:0>			0000 0000	0000 0000
997h		—	—	—	—	—	PCH2	PCH1	PCH0	0000 0000	0000 0000
998h	—	Unimplemented								---- ----	---- ----
999h	—	Unimplemented								---- ----	---- ----
99Ah	—	Unimplemented								---- ----	---- ----
99Bh	—	Unimplemented								---- ----	---- ----
99Ch	—	Unimplemented								---- ----	---- ----
99Dh	—	Unimplemented								---- ----	---- ----
99Eh	—	Unimplemented								---- ----	---- ----
99Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

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8.5 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) is an essential part of the Rest subsystem. Refer to Figure 8-1 to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external VDD pin. when too low of a voltage is detected, the device is held in Reset. When this occurs, a register bit ($\overline{BOR}$) is changed to indicate that a BOR Reset has occurred. The same bit is set for both the BOR and the LPBOR. Refer to Register 8-2.

8.5.1 ENABLING LPBOR

The LPBOR is controlled by the $\overline{LPBOR}$ bit of the Configuration Word (Register 5-1). When the device is erased, the LPBOR module defaults to disabled.

8.5.2 LPBOR MODULE OUTPUT

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. This signal is OR'd together with the Reset signal of the BOR module to provide the generic $\overline{BOR}$ signal, which goes to the PCON register and to the power control block.

8.6 $\overline{MCLR}$

The $\overline{MCLR}$ is an optional external input that can reset the device. The $\overline{MCLR}$ function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 8-2).

TABLE 8-2: $\overline{MCLR}$ CONFIGURATION

MCLRE	LVP	$\overline{MCLR}$
0	0	Disabled
1	0	Enabled
x	1	Enabled

8.6.1 $\overline{MCLR}$ ENABLED

When $\overline{MCLR}$ is enabled and the pin is held low, the device is held in Reset. The $\overline{MCLR}$ pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

Note:	A Reset does not drive the $\overline{MCLR}$ pin low.

8.6.2 $\overline{MCLR}$ DISABLED

When $\overline{MCLR}$ is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See **Section 14.1 "I/O Priorities"** for more information.

8.7 Windowed Watchdog Timer (WWDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period and the window is open. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register and the $\overline{WDT}$ bit in PCON are changed to indicate a WDT Reset caused by the timer overflowing, and WDTWV bit in the PCON register is changed to indicate a WDT Reset caused by a window violation. See **Section 12.0 "Windowed Watchdog Timer (WWDT)"** for more information.

8.8 RESET Instruction

A RESET instruction will cause a device Reset. The $\overline{RI}$ bit in the PCON register will be set to '0'. See Table 8-4 for default conditions after a RESET instruction has occurred.

8.9 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See **Section 4.5.2 "Overflow/Underflow Reset"** for more information.

8.10 Programming Mode Exit

Upon exit of In-Circuit Serial Programming™ (ICSP™) mode, the device will behave as if a POR had just occurred (the device does not reset upon run time self-programming/erase operations).

8.11 Power-up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the $\overline{PWRTE}$ bit of the Configuration Words.

The Power-up Timer provides a nominal 64 ms time out on POR or Brown-out Reset. The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the $\overline{PWRTE}$ bit in the Configuration Words. The Power-up Timer starts after the release of the POR and BOR. For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*" (DS00607).

9.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode).

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated Phase Lock Loop (PLL) that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce a range from 1 to 32 MHz. The Low-Frequency Internal Oscillator (LFINTOSC) generates a 31 kHz frequency. The external oscillator block can also be used with the PLL.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 9.3 "Clock Switching"** for additional information.

9.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset
- Write the NOSC<2:0> and NDIV<3:0> bits in the OSCCON1 register to switch the system clock source

See **Section 9.3 "Clock Switching"** for more information.

9.2.1.1 EC Mode

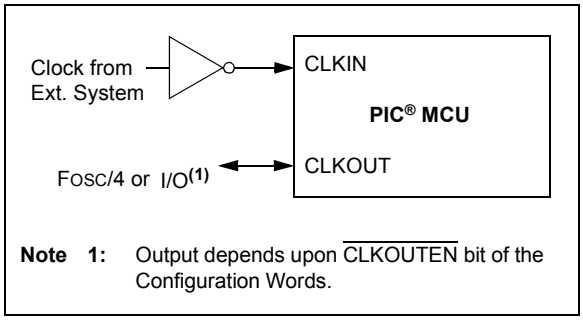
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the CLKIN input. CLKOUT is available for general purpose I/O or CLKOUT. Figure 9-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH – High power, < = 32 MHz
- ECM – Medium power, < = 8 MHz
- ECL – Low power, < = 0.5 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 9-2: EXTERNAL CLOCK (EC) MODE OPERATION

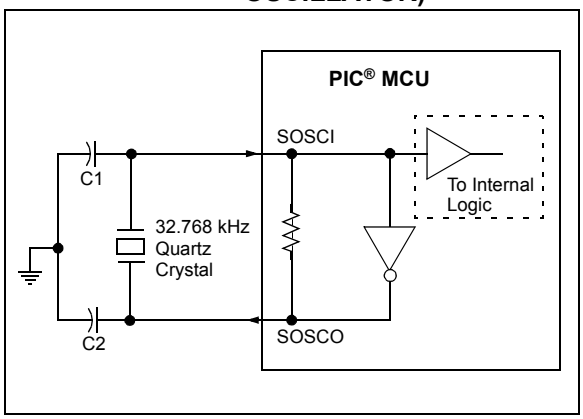


Note 1: Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words.

9.2.1.2 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCI pin. Refer to **Section 9.3 "Clock Switching"** for more information.

FIGURE 9-3: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)



9.5 Active Clock Tuning

The Active Clock Tuning module (ACT) takes the SOSC frequency of 32.768 kHz and uses that time base to adjust the frequency of the HFINTOSC over voltage and temperature. The ACT module uses the same TUN<5:0> bits as supplied to the user. When clock recovery is enabled, the TUN bits are read-only to the user, and automatically updated.

REGISTER 10-16: PIR5: PERIPHERAL INTERRUPT REQUEST REGISTER 5

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	R/W/HS-0/0
CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **CLC4IF:** CLC4 Interrupt Flag bit
1 = A CLC4OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC4 interrupt event has occurred

bit 6 **CLC3IF:** CLC3 Interrupt Flag bit
1 = A CLC3OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC3 interrupt event has occurred

bit 5 **CLC2IF:** CLC2 Interrupt Flag bit
1 = A CLC2OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC2 interrupt event has occurred

bit 4 **CLC1IF:** CLC1 Interrupt Flag bit
1 = A CLC1OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC1 interrupt event has occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = The Timer1 Gate has gone inactive (the acquisition is complete)
0 = The Timer1 Gate has not gone inactive

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 14-49: HIDRVF: PORTF HIGH DRIVE CONTROL REGISTER

R/W-0/0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
HIDF7	—	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **HIDF7:** PORTF High Drive Enable bit
For RF7 pin
1 = High current source and sink enabled
0 = Standard current source and sink

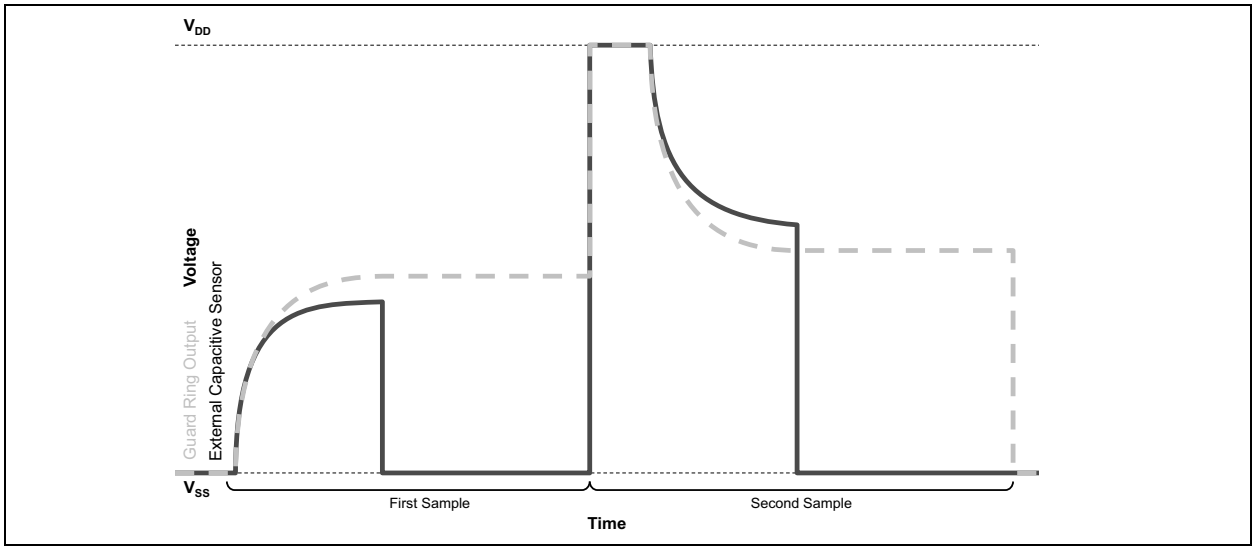
bit 6-0 **Unimplemented:** Read as '0'

TABLE 14-7: SUMMARY OF REGISTERS ASSOCIATED WITH PORTF

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	255
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	255
LATF	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	256
ANSELF	ANSF7	ANSF6	ANSF5	ANSF4	ANSF3	ANSF2	ANSF1	ANSF0	256
WPUF	WPUF7	WPUF6	WPUF5	WPUF4	WPUF3	WPUF2	WPUF1	WPUF0	256
ODCONF	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	257
SLRCONF	SLRF7	SLRF6	SLRF5	SLRF4	SLRF3	SLRF2	SLRF1	SLRF0	257
INLVLF	INLVLF7	INLVLF6	INLVLF5	INLVLF4	INLVLF3	INLVLF2	INLVLF1	INLVLF0	257
HIDRVF	HIDF7	—	—	—	—	—	—	—	258

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTF.

FIGURE 19-9: DIFFERENTIAL CVD WITH GUARD RING OUTPUT WAVEFORM



19.4.5 ADDITIONAL SAMPLE AND HOLD CAPACITANCE

Additional capacitance can be added in parallel with the internal sample and hold capacitor (CHOLD) by using the ADCAP register. This register selects a digitally programmable capacitance which is added to the ADC conversion bus, increasing the effective internal capacitance of the sample and hold capacitor in the ADC module. This is used to improve the match between internal and external capacitance for a better sensing performance. The additional capacitance does not affect analog performance of the ADC because it is not connected during conversion. See Figure 19-10.

19.5.5 BURST AVERAGE MODE

The Burst Average mode (ADMD = 011) acts the same as the Average mode in most respects. The one way it differs is that it continuously retriggers ADC sampling until the CNT value is greater than or equal to RPT, even if Continuous Sampling mode (see **Section 19.5.8 "Continuous Sampling mode"**) is not enabled. This allows for a threshold comparison on the average of a short burst of ADC samples.

19.5.6 LOW-PASS FILTER MODE

The Low-Pass Filter mode (ADMD = 100) acts similarly to the Average mode in how it handles samples (accumulates samples until CNT value is greater than or equal to RPT, then triggers threshold comparison. CNT does not reset once it is greater or equal to RPT. Thus CNT will be greater than RPT for all subsequent samples until CNT is reset by the user), but instead of a simple average, it performs a low-pass filter operation on all of the samples, reducing the effect of high-frequency noise on the average, then performs a threshold comparison on the results. (see Table 19-2 for a more detailed description of the mathematical operation). In this mode, the ADCRS bits determine the cut-off frequency of the low-pass filter (as demonstrated by Table 19-3).

19.5.7 THRESHOLD COMPARISON

At the end of each computation:

- The conversion results are latched and held stable at the end-of-conversion.
- The error is calculated based on a difference calculation which is selected by the ADCALC<2:0> bits in the ADCON3 register. The value can be one of the following calculations (see Register 19-4 for more details):
  - The first derivative of single measurements
  - The CVD result in CVD mode
  - The current result vs. a setpoint
  - The current result vs. the filtered/average result
  - The first derivative of the filtered/average value
  - Filtered/average value vs. a setpoint
- The result of the calculation (ERR) is compared to the upper and lower thresholds, UTH<ADUTHH:ADUTHL> and LTH<ADLTHH:ADLTHL> registers, to set the ADUTHR and ADLTHR flag bits. The threshold logic is selected by ADTMD<2:0> bits in the ADCON3 register. The threshold trigger option can be one of the following:
  - Never interrupt
  - Error is less than lower threshold
  - Error is greater than or equal to lower threshold
  - Error is between thresholds (inclusive)
  - Error is outside of thresholds
  - Error is less than or equal to upper threshold
  - Error is greater than upper threshold
  - Always interrupt regardless of threshold test results
  - If the threshold condition is met, the threshold interrupt flag ADTIF is set.

Note 1:	The threshold tests are signed operations.
2:	If OV is set, a threshold interrupt is signaled.

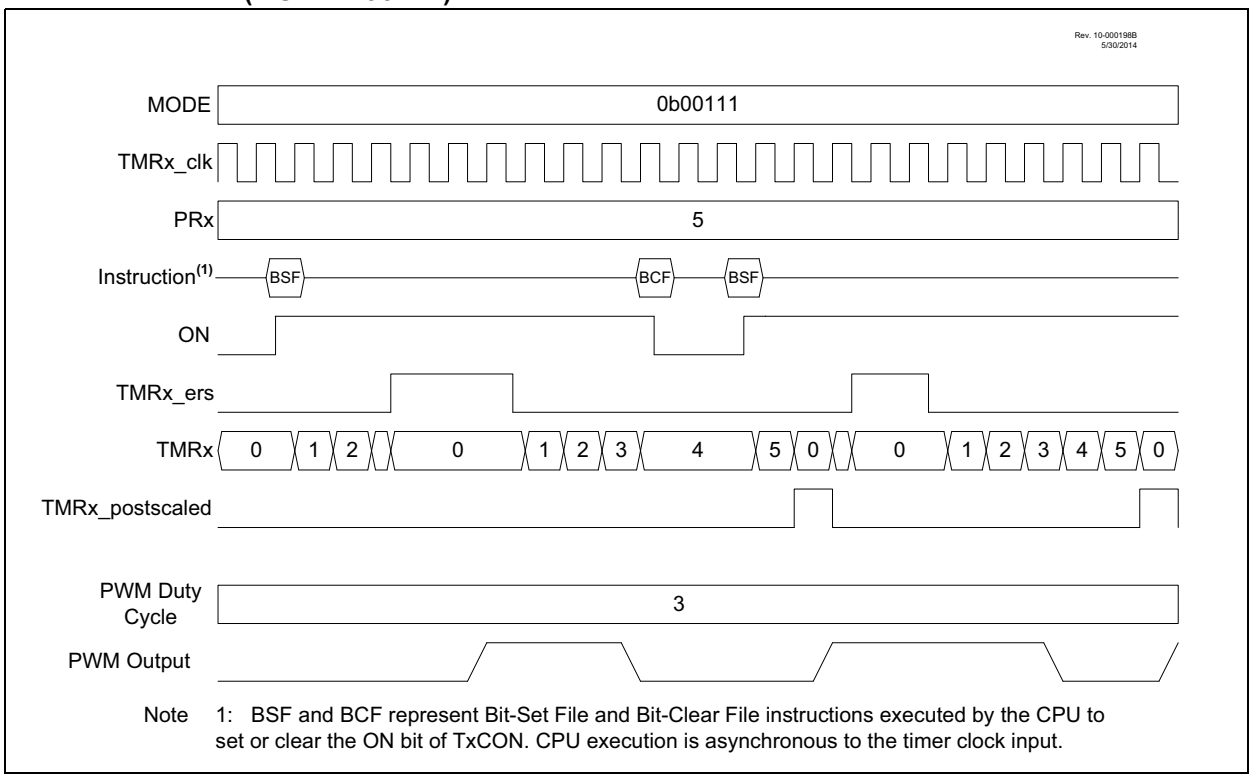
27.5.4 LEVEL-TRIGGERED HARDWARE LIMIT MODE

In the Level-Triggered Hardware Limit Timer modes the counter is reset by high or low levels of the external signal TMRx_ers, as shown in Figure 27-7. Selecting MODE<4:0> = 00110 will cause the timer to reset on a low level external signal. Selecting MODE<4:0> = 00111 will cause the timer to reset on a high level external signal. In the example, the counter is reset while TMRx_ers = 1. ON is controlled by BSF and BCF instructions. When ON = 0 the external signal is ignored.

When the CCP uses the timer as the PWM time base then the PWM output will be set high when the timer starts counting and then set low only when the timer count matches the CCPRx value. The timer is reset when either the timer count matches the PRx value or two clock periods after the external Reset signal goes true and stays true.

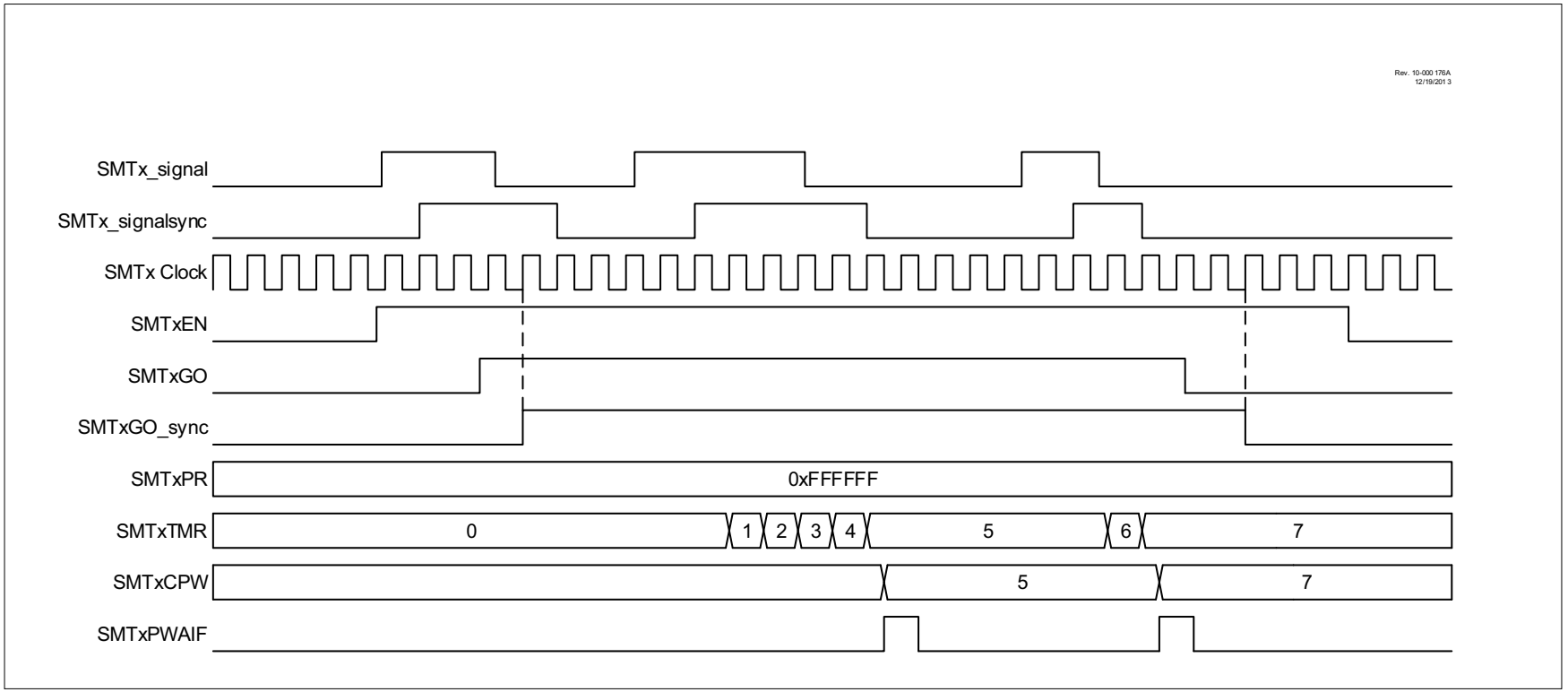
The timer starts counting, and the PWM output is set high, on either the clock following the PRx match or two clocks after the external Reset signal relinquishes the Reset. The PWM output will remain high until the timer counts up to match the CCPRx pulse width value. If the external Reset signal goes true while the PWM output is high then the PWM output will remain high until the Reset signal is released allowing the timer to count up to match the CCPRx value.

FIGURE 27-7: LEVEL-TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE = 00111)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

FIGURE 28-4: GATED TIMER MODE REPEAT ACQUISITION TIMING DIAGRAM



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28.7.4 HIGH AND LOW-MEASURE MODE

This mode measures the high and low-pulse time of the SMTSIGx relative to the SMT clock. It begins incrementing the SMTxTMR on a rising edge on the SMTSIGx input, then updates the SMTxCPW register with the value and resets the SMTxTMR on a falling edge, starting to increment again. Upon observing another rising edge, it updates the SMTxCPR register with its current value and once again resets the SMTxTMR value and begins incrementing again. See Figure 28-8 and Figure 28-9.

REGISTER 31-6: CWG1AS1: CWG1 AUTO-SHUTDOWN CONTROL REGISTER 1

U-1	U-1	U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **AS4E:** CLC2 Output bit
1 = LC2_out shut-down is enabled
0 = LC2_out shut-down is disabled

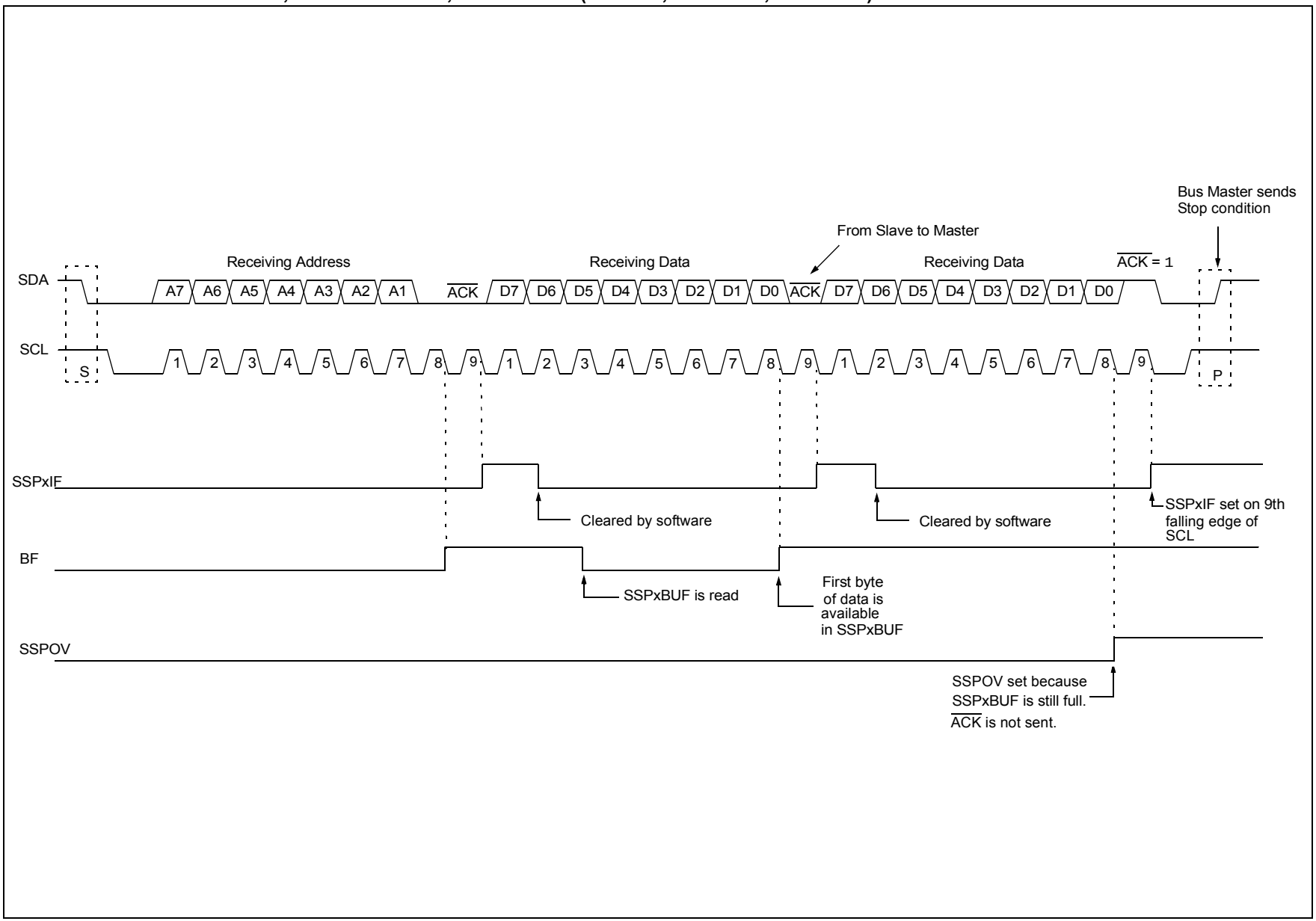
bit 3 **AS3E:** Comparator C2 Output bit
1 = C2 output shut-down is enabled
0 = C2 output shut-down is disabled

bit 2 **AS2E:** Comparator C1 Output bit
1 = C1 output shut-down is enabled
0 = C1 output shut-down is disabled

bit 2 **AS1E:** TMR2 Postscale Output bit
1 = TMR2 Postscale shut-down is enabled
0 = TMR2 Postscale shut-down is disabled

bit 0 **AS0E:** CWG1 Input Pin bit
1 = Input pin selected by CWG1PPS shut-down is enabled
0 = Input pin selected by CWG1PPS shut-down is disabled

FIGURE 33-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)



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33.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition (Figure 33-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 33-27: REPEATED START CONDITION WAVEFORM

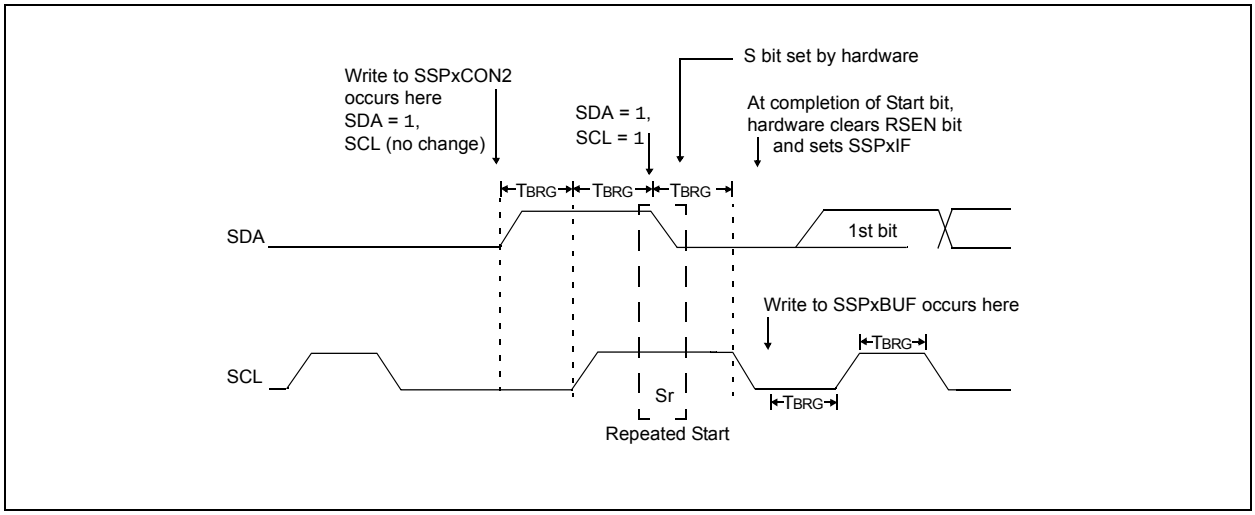

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
891h	OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	156
892h	OSCTUNE	—	—	HFTUN<5:0>						157
893h	OSCFRQ	—	—	—	—	—	HFFRQ<2:0>			157
894h	ACTCON	ACTEN	ACTUD	—	—	ACTLOCK	—	ACTORS	—	158
895h	—	Unimplemented								
896h	—	Unimplemented								
897h	—	Unimplemented								
898h	—	Unimplemented								
899h	—	Unimplemented								
89Ah	—	Unimplemented								
89Bh	—	Unimplemented								
89Ch	—	Unimplemented								
89Dh	—	Unimplemented								
89Eh	—	Unimplemented								
89Fh	—	Unimplemented								
90Ch	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		285
90Dh	—	Unimplemented								
90Eh	DAC1CON0	EN	—	OE1	OE2	DAC1PSS<1:0>		—	—	332
90Fh	DAC1CON1	—	—	—	DAC1R<4:0>					332
90Fh		—	—	—	DAC1R4	DAC1R3	DAC1R2	DAC1R1	DAC1R0	332
910h	—	Unimplemented								
911h	—	Unimplemented								
912h	—	Unimplemented								
913h	—	Unimplemented								
914h	—	Unimplemented								
915h	—	Unimplemented								
916h	—	Unimplemented								
917h	—	Unimplemented								
918h	—	Unimplemented								
919h	—	Unimplemented								
91Ah	—	Unimplemented								
91Bh	—	Unimplemented								
91Ch	—	Unimplemented								
91Dh	—	Unimplemented								
91Eh	—	Unimplemented								
91Fh	ZCDCON	ZCDSEN	—	ZCDOUT	ZCDPOL	—	—	ZCDINTP	ZCDINTN	349
98Ch	—	Unimplemented								
98Dh	—	Unimplemented								
98Eh	—	Unimplemented								
98Fh	CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	343
990h	CM1CON0	ON	OUT	—	POL	—	—	HYS	SYNC	340
991h	CM1CON1	—	—	—	—	—	—	INTP	INTN	341
992h	CM1NSEL	—	—	—	—	—	NCH<2:0>			342
992h		—	—	—	—	—	NCH2	NCH1	NCH0	342
993h	CM1PSEL	—	—	—	—	PCH<3:0>				342
993h		—	—	—	—	—	PCH2	PCH1	PCH0	342

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

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TABLE 39-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param. No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	60	°C/W	28-pin SPDIP package
			80	°C/W	28-pin SOIC package
			90	°C/W	28-pin SSOP package
			48	°C/W	28-pin UQFN 4x4 mm package
			47.2	°C/W	40-pin PDIP package
			41.0	°C/W	40-pin UQFN 5x5 package
			46.0	°C/W	44-pin TQFP package
			24.4	°C/W	44-pin QFN 8x8 mm package
			27.6	°C/W	48-pin UQFN 6x6 package
			—	°C/W	48-pin TQFP 7x7 package
TH02	θJC	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package
			24	°C/W	28-pin SOIC package
			24	°C/W	28-pin SSOP package
			12	°C/W	28-pin UQFN 4x4 mm package
			24.70	°C/W	40-pin PDIP package
			5.5	°C/W	40-pin UQFN 5x5 package
			14.5	°C/W	44-pin TQFP package
			20.0	°C/W	44-pin QFN 8x8 mm package
			6.7	°C/W	48-pin UQFN 6x6 package
			—	°C/W	48-pin TQFP 7x7 package
TH03	TJMAX	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD(1)
TH06	PI/O	I/O Power Dissipation	—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power	—	W	PDER = PDMAX (TJ - TA)/θJA(2)

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature, TJ = Junction Temperature

PRELIMINARY

TABLE 39-13: ANALOG-TO-DIGITAL CONVERTER (ADC) CONVERSION TIMING SPECIFICATIONS

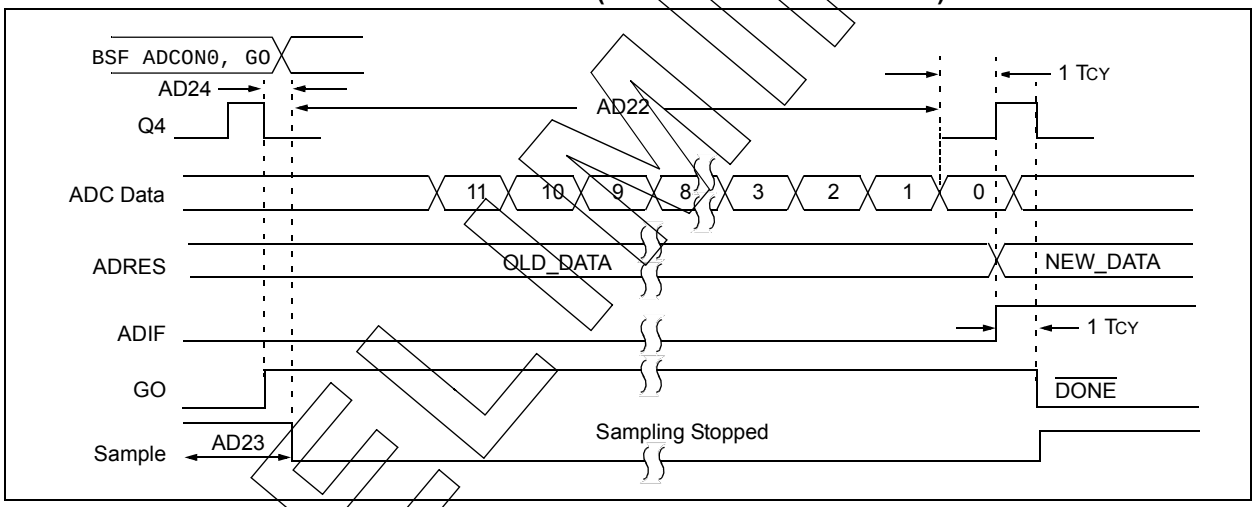
Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD20	TAD	ADC Clock Period	1	—	9	μs	Using FOSC as the ADC clock source ADCS = 1
AD21			—	2	—	μs	Using FRC as the ADC clock source ADSC = 0
AD22	TCNV	Conversion Time	—	14 TAD + 2 TCY	—	—	Using FOSC as the ADC clock source ADCS = 1
			—	16 TAD + 2 TCY	—	—	Using FRC as the ADC clock source ADSC = 0
AD24	THCD	Sample and Hold Capacitor Disconnect Time	—	2 TAD + 1 TCY	—	—	Using FOSC as the ADC clock source ADCS = 1
			—	3 TAD + 2 TCY	—	—	Using FRC as the ADC clock source ADSC = 0

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

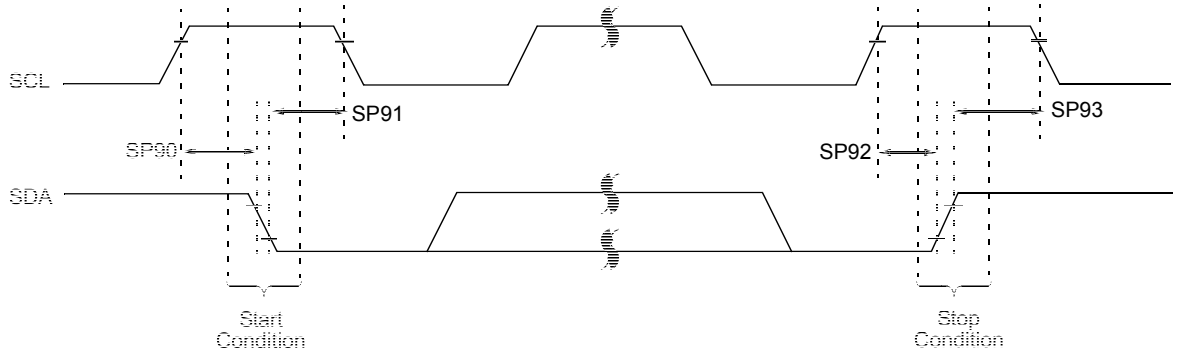
Note 1: A TAD of 8 μs is recommended measuring the 1/3 tap point on the VBAT.

FIGURE 39-10: ADC CONVERSION TIMING (ADC CLOCK Fosc-BASED)



PRELIMINARY

FIGURE 39-21: I²C BUS START/STOP BITS TIMING



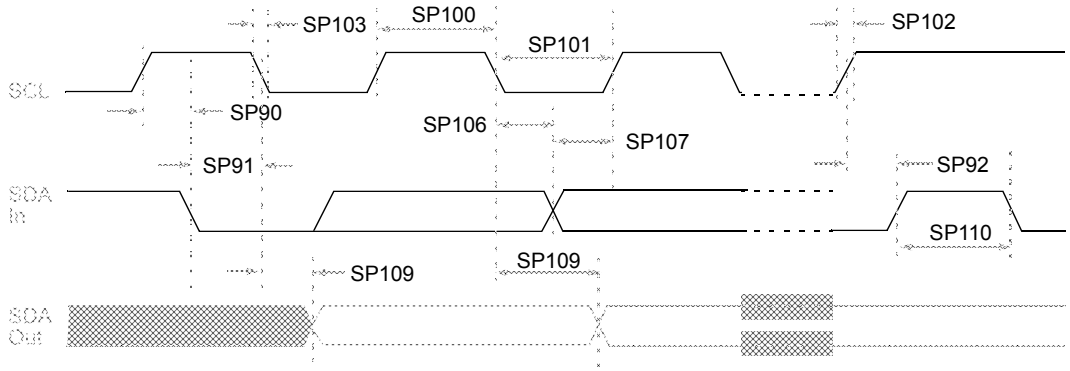
Note: Refer to Figure 39-4 for load conditions.

TABLE 39-25: I²C BUS START/STOP BITS REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
SP90*	TSU:STA	Start condition	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
		Setup time	400 kHz mode	600	—	—		
SP91*	THD:STA	Start condition	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
SP92*	TSU:STO	Stop condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
SP93	THD:STO	Stop condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

FIGURE 39-22: I²C BUS DATA TIMING



Note: Refer to Figure 39-4 for load conditions.