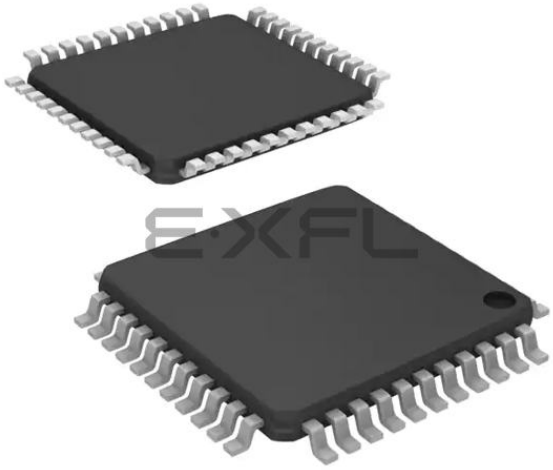

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 31x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19175-e-pt

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides three specific device functions:

- Device Reset (when MCLRE = 1)
- Digital input pin (when MCLRE = 0)
- Device Programming and Debugging

If programming and debugging are not required in the end application then either set the MCLRE Configuration bit to '1' and use the pin as a digital input or clear the MCLRE Configuration bit and leave the pin open to use the internal weak pull-up. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, the programmer $\overline{MCLR}/V_{PP}$ output should be connected directly to the pin so that R1 isolates the capacitor, C1 from the $\overline{MCLR}$ pin during programming and debugging operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be isolated from the programmer by resistors between the application and the device pins or removed from the circuit during programming. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/ emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 41.0 "Development Support"**.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 20											
CPU CORE REGISTERS; see Table 4-3 for specifics											
A0Ch	—	Unimplemented								---- ----	---- ----
A0Dh	—	Unimplemented								---- ----	---- ----
A0Eh	—	Unimplemented								---- ----	---- ----
A0Fh	—	Unimplemented								---- ----	---- ----
A10h	—	Unimplemented								---- ----	---- ----
A11h	—	Unimplemented								---- ----	---- ----
A12h	—	Unimplemented								---- ----	---- ----
A13h	—	Unimplemented								---- ----	---- ----
A14h	—	Unimplemented								---- ----	---- ----
A15h	—	Unimplemented								---- ----	---- ----
A16h	—	Unimplemented								---- ----	---- ----
A17h	—	Unimplemented								---- ----	---- ----
A18h	—	Unimplemented								---- ----	---- ----
A19h	RC2REG	RC2REG								0000 0000	0000 0000
A1Ah	TX2REG	TX2REG								0000 0000	0000 0000
A1Bh	SP2BRGL	SP2BRGL								0000 0000	0000 0000
A1Ch	SP2BRGH	SP2BRGH								0000 0000	0000 0000
A1Dh	RC2STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
A1Eh	TX2STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
A1Fh	BAUD2CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 62 (Continued)											
1F4Eh	ANSELC	ANSC7	ANSC6	—	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	1111 1111	1111 1111
1F4Fh	WPUC	WPUC7	WPUC6	—	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	0000 0000	0000 0000
1F50h	ODCONC	ODCC7	ODCC6	—	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000 0000	0000 0000
1F51h	SLRCONC	SLRC7	SLRC6	—	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	1111 1111	1111 1111
1F52h	INLVLC	INLVLC7	INLVLC6	—	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	1111 1111	1111 1111
1F53h	IOCCP	IOCCP7	IOCCP6	—	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	0000 0000	0000 0000
1F54h	IOCCN	IOCCN7	IOCCN6	—	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	0000 0000	0000 0000
1F55h	IOCCF	IOCCF7	IOCCF6	—	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	0000 0000	0000 0000
1F56h	—	Unimplemented								---- ----	---- ----
1F57h	—	Unimplemented								---- ----	---- ----
1F58h	—	Unimplemented								---- ----	---- ----
1F59h	ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	1111 1111	1111 1111
1F5Ah	WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	0000 0000	0000 0000
1F5Bh	ODCOND	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000 0000	0000 0000
1F5Ch	SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	1111 1111	1111 1111
1F5Dh	INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	1111 1111	1111 1111
1F5Eh	—	Unimplemented								---- ----	---- ----
1F5Fh	—	Unimplemented								---- ----	---- ----
1F60h	—	Unimplemented								---- ----	---- ----
1F61h	—	Unimplemented								---- ----	---- ----
1F62h	—	Unimplemented								---- ----	---- ----
1F63h	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

REGISTER 14-5: WPUA: WEAK PULL-UP PORTA REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUA7	WPUA6	WPUA5(2)	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUA<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.
2: Bit not used when $\overline{V_{BATEN}}$ = 0.

REGISTER 14-6: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCA7	ODCA6	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **ODCA<7:6>:** PORTA Open-Drain Enable bits
For RA<7:6> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **ODCA<4:0>:** PORTA Open-Drain Enable bits
For RA<4:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

TABLE 14-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	229
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	229
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	230
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	230
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	231
ODCONB	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	231
SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	232
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	232
HIDRVB	—	—	—	—	—	—	HIDB1	—	232

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

REGISTER 19-22: ADPREVH: ADC PREVIOUS RESULT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
PREV<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PREV<15:8>**: Previous ADC Results bits
If ADPSIS = 1:
Upper byte of FLTR at the start of current ADC conversion
If ADPSIS = 0:
Upper bits of ADRES at the start of current ADC conversion(1)

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the FM bit.

REGISTER 19-23: ADPREVL: ADC PREVIOUS RESULT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
PREV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PREV<7:0>**: Previous ADC Results bits
If ADPSIS = 1:
Lower byte of FLTR at the start of current ADC conversion
If ADPSIS = 0:
Lower bits of ADRES at the start of current ADC conversion(1)

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the FM bit.

21.6 Register Definitions: DAC Control

REGISTER 21-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **DAC1EN:** DAC1 Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **DAC1OE1:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT1 pin
0 = DAC voltage level is disconnected from the DAC1OUT1 pin

bit 4 **DAC1OE2:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT2 pin
0 = DAC voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 **DAC1PSS<1:0>:** DAC1 Positive Source Select bits
11 = Reserved, do not use
10 = FVR output
01 = V_{REF+} pin
00 = V_{DD}

bit 1-0 **Unimplemented:** Read as ‘0’

REGISTER 21-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	DAC1R<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DAC1R<4:0>:** DAC1 Voltage Output Select bits
$V_{OUT} = (V_{SRC+} - V_{SRC-})*(DAC1R<4:0>/32) + V_{SRC}$

REGISTER 27-4: TxRST: TIMER2/4 EXTERNAL RESET SIGNAL SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	RSEL<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

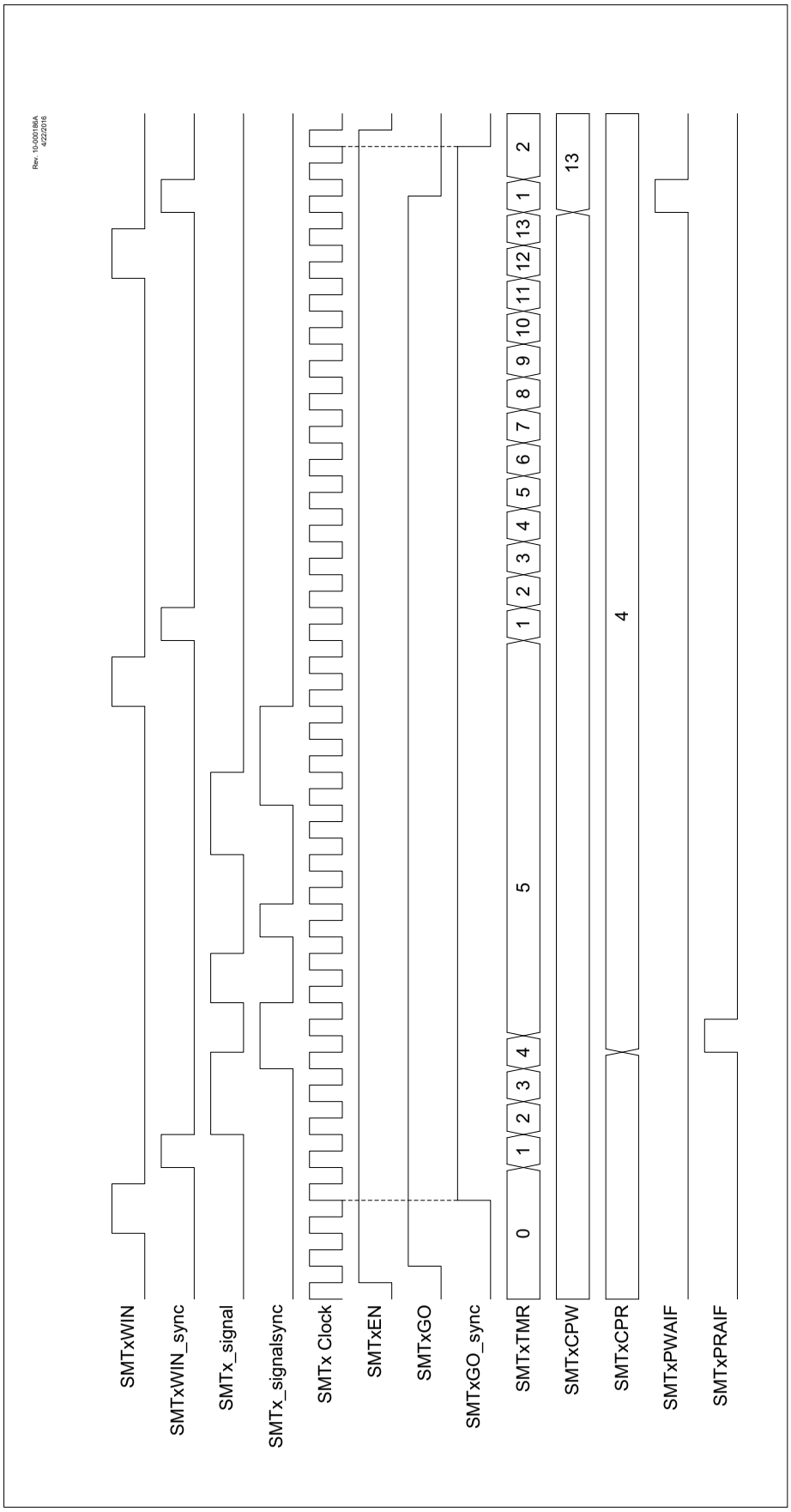
bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **RSEL<3:0>:** Timer2/4 External Reset Signal Source Selection bits

1111 = Reserved
1110 = RTCC_Seconds
1101 = LC4_out
1100 = LC3_out
1011 = LC2_out
1010 = LC1_out
1001 = ZCD1_output
1000 = C2OUT_sync
0111 = C1OUT_sync
0110 = PWM3_out
0101 = PWM4_out
0100 = CCP2_out
0011 = CCP1_out
0010 = TMR4_postscaled(2)
0001 = TMR2_postscaled(1)
0000 = T2INPPS

Note 1: For Timer2, this bit is Reserved.
2: For Timer4, this bit is Reserved.

FIGURE 28-14: TIME OF FLIGHT MODE REPEAT ACQUISITION TIMING DIAGRAM



31.12 Configuring the CWG

The following steps illustrate how to properly configure the CWG.

1. Ensure that the TRIS control bits corresponding to the desired CWG pins for your application are set so that the pins are configured as inputs.
2. Clear the EN bit, if not already cleared.
3. Set desired mode of operation with the MODE bits.
4. Set desired dead-band times, if applicable to mode, with the CWG1DBR and CWG1DBF registers.
5. Setup the following controls in the CWG1AS0 and CWG1AS1 registers.
   a. Select the desired shutdown source.
   b. Select both output overrides to the desired levels (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
   c. Set which pins will be affected by auto-shutdown with the CWG1AS1 register.
   d. Set the SHUTDOWN bit and clear the REN bit.
6. Select the desired input source using the CWG1ISM register.
7. Configure the following controls.
   a. Select desired clock source using the CWG1CLKCON register.
   b. Select the desired output polarities using the CWG1CON1 register.
   c. Set the output enables for the desired outputs.
8. Set the EN bit.
9. Clear TRIS control bits corresponding to the desired output pins to configure these pins as outputs.
10. If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit to start the CWG.

31.12.1 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown input is true, are controlled by the LSBD and LSAC bits of the CWG1AS0 register. LSBD<1:0> controls the CWG1B and D override levels and LSAC<1:0> controls the CWG1A and C override levels. The control bit logic level corresponds to the output logic drive level while in the shutdown state. The polarity control does not affect the override level.

31.12.2 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the REN bit of the CWG1CON2 register. Waveforms of software controlled and automatic restarts are shown in Figure 31-13 and Figure 31-14.

31.12.2.1 Software Controlled Restart

When the REN bit of the CWG1AS0 register is cleared, the CWG must be restarted after an auto-shutdown event by software. Clearing the shutdown state requires all selected shutdown inputs to be low, otherwise the SHUTDOWN bit will remain set. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

31.12.2.2 Auto-Restart

When the REN bit of the CWG1CON2 register is set, the CWG will restart from the auto-shutdown state automatically. The SHUTDOWN bit will clear automatically when all shutdown sources go low. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

32.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

32.1.1 DATA SELECTION

There are 40 signals available as inputs to the configurable logic. Four 40-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 32-2. Data inputs in the figure are identified by a generic numbered input name.

Table 32-2 correlates the generic input name to the actual signal for each CLC module. The column labeled 'LCxDyS<5:0> Value' indicates the MUX selection code for the selected data input. LCxDyS is an abbreviation to identify specific multiplexers: LCxD1S<5:0> through LCxD4S<5:0>.

Data inputs are selected with CLCxSEL0 through CLCxSEL3 registers (Register 32-3 through Register 32-6).

TABLE 32-2: CLCx DATA INPUT SELECTION

LCxDyS<5:0> Value	CLCx Input Source
100101 to 111111	Reserved
100100	EUSART2 (TX/CK) output
100011	EUSART2 (DT) output
100010	CWG1B output
100001	CWG1A output
100000	RTCC seconds
011111	MSSP1 SCK output
011110	MSSP1 SDO output
011101	EUSART1 (TX/CK) output
011100	EUSART1 (DT) output
011011	CLC4 output
011010	CLC3 output
011001	CLC2 output
011000	CLC1 output
010111	IOCIF
010110	ZCD output
010101	C2OUT
010100	C1OUT
010011	PWM4 output
010010	PWM3 output
010001	CCP2 output
010000	CCP1 output
001111	SMT overflow
001110	Timer4 overflow
001101	Timer2 overflow
001100	Timer1 overflow
001011	Timer0 overflow
001010	ADCRC
001001	SOSC
001000	MFINTOSC (32 kHz)
000111	MFINTOSC (500 kHz)
000110	LFINTOSC
000101	HFINTOSC
000100	FOSC
000011	CLCIN3PPS
000010	CLCIN2PPS
000001	CLCIN1PPS
000000	CLCIN0PPS

TABLE 32-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx (continued)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CLC4GLS1	LC4G2D4T	LC4G2D4N	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	506
CLC4GLS2	LC4G3D4T	LC4G3D4N	LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	507
CLC4GLS3	LC4G4D4T	LC4G4D4N	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	508
CLCIN0PPS	—	—	—	CLCIN0PPS<4:0>					264
CLCIN1PPS	—	—	—	CLCIN1PPS<4:0>					264
CLCIN2PPS	—	—	—	CLCIN2PPS<4:0>					264
CLCIN3PPS	—	—	—	CLCIN3PPS<4:0>					264

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

33.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULES

33.1 MSSP Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

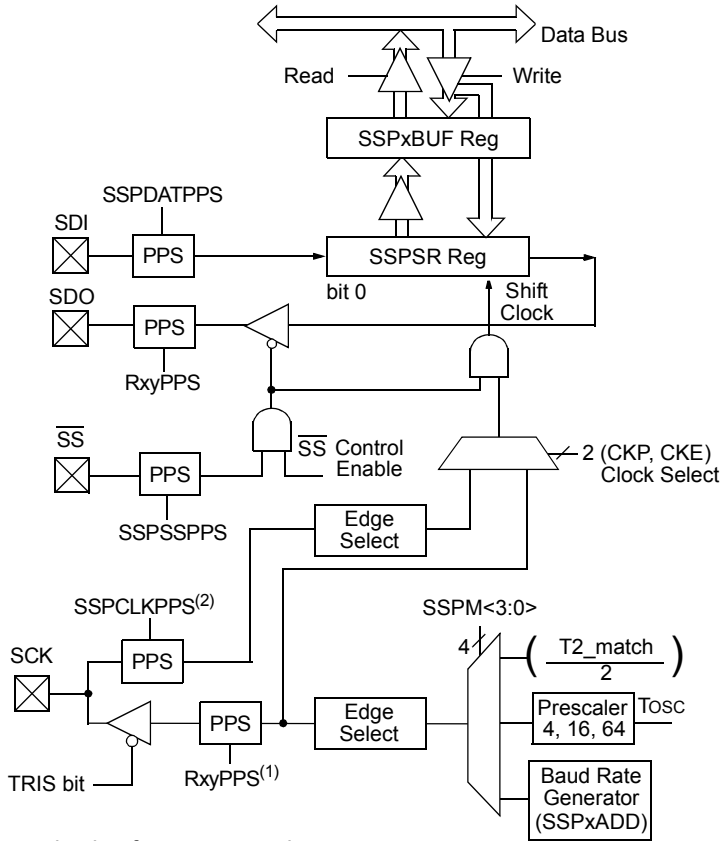
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

The SPI interface supports the following modes and features:

- Master mode
- Slave mode
- Clock Polarity
- Slave Select Synchronization (Slave mode only)
- Daisy-chain connection of slave devices

Figure 33-1 is a block diagram of the SPI interface module.

FIGURE 33-1: MSSP BLOCK DIAGRAM (SPI MODE)



Note 1: Output selection for master mode

2: Input selection for slave mode

33.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level (Case 1).
b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 33-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 33-37.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 33-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

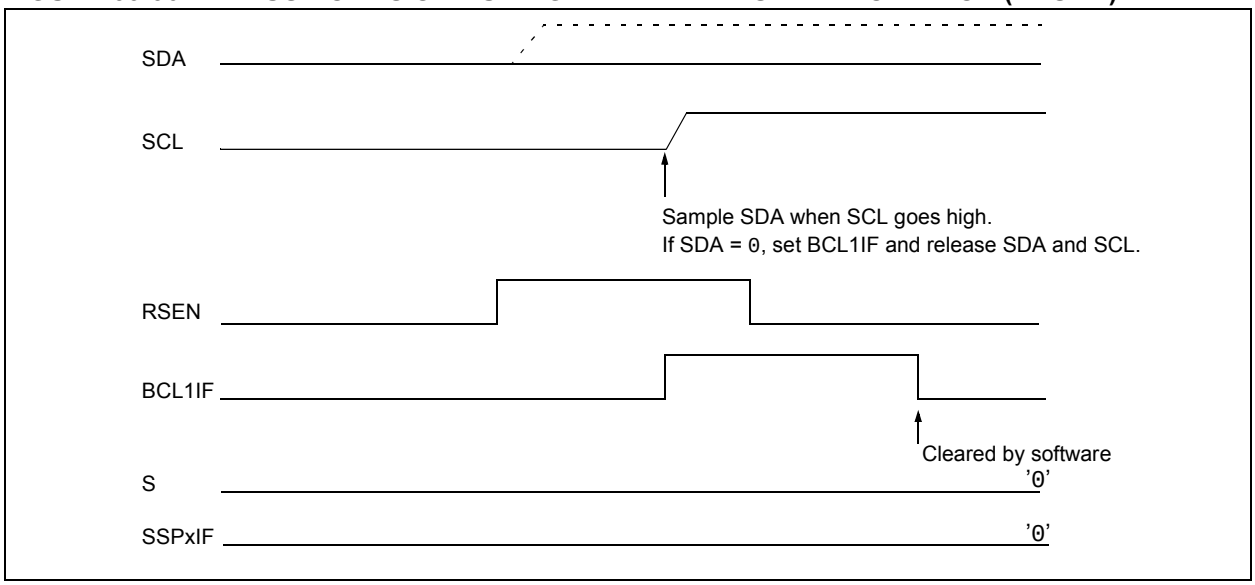


FIGURE 33-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

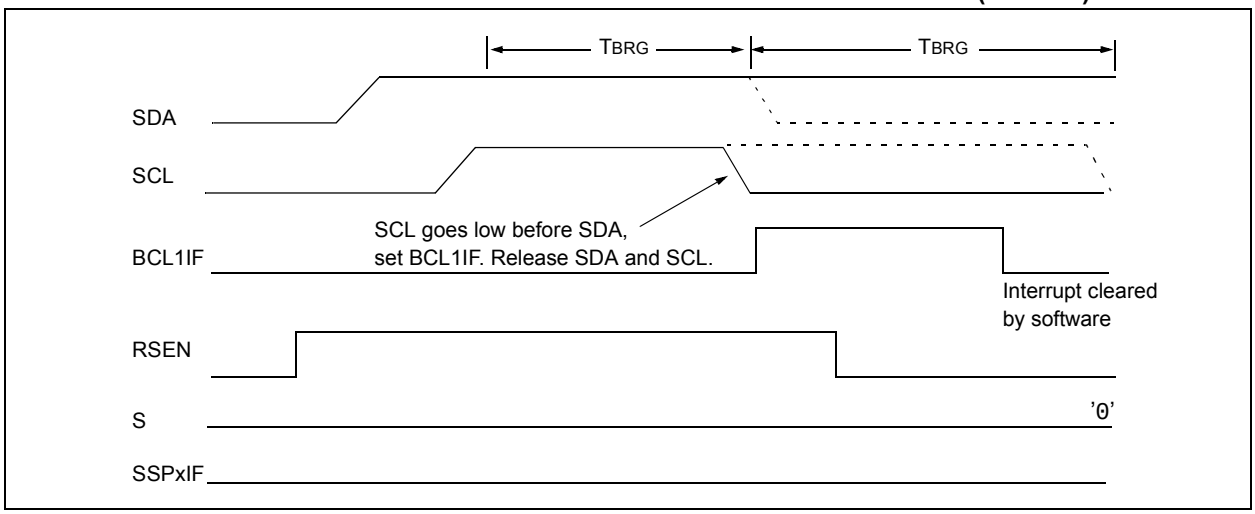


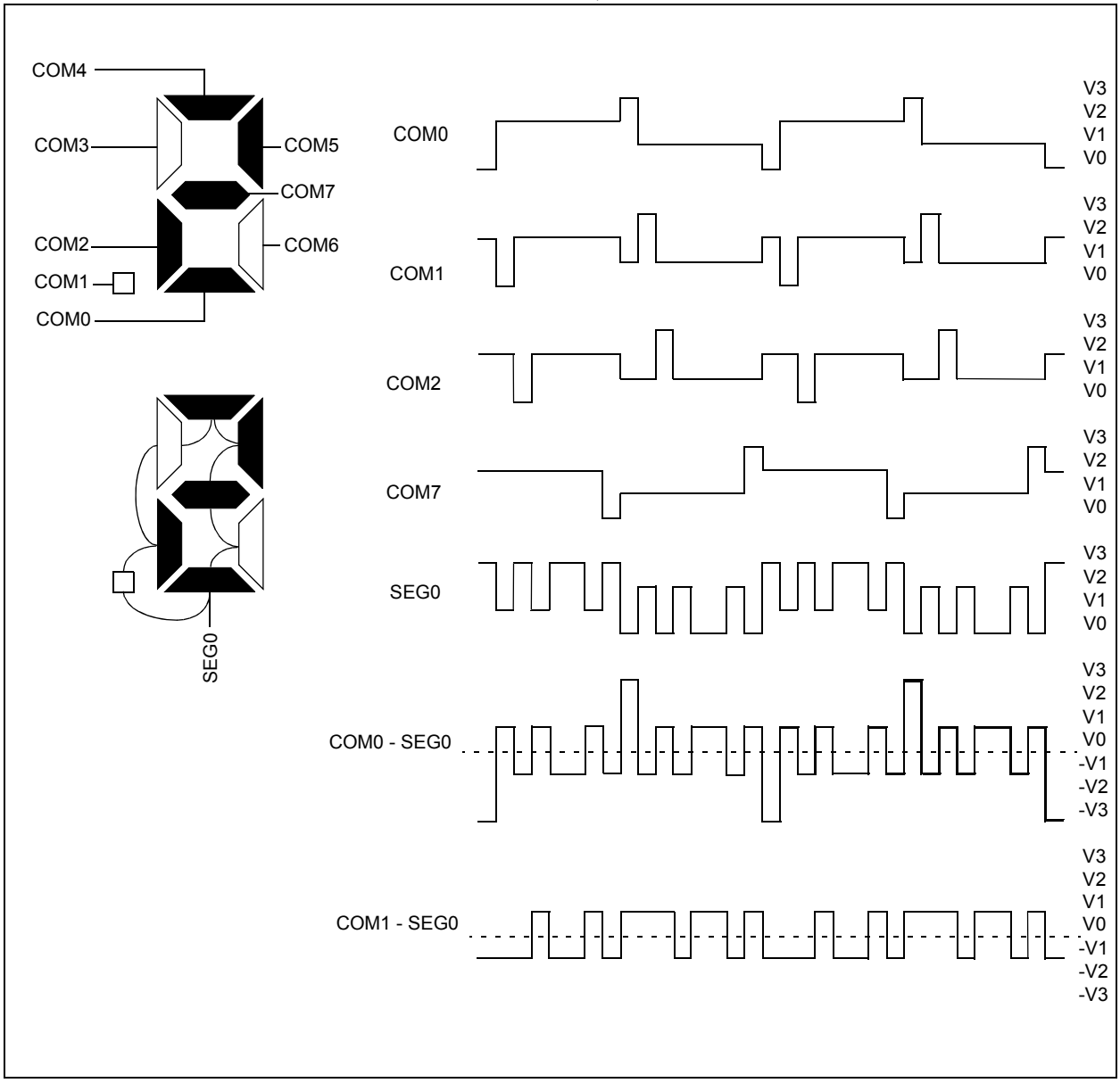
TABLE 35-4: LCDDATAX REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS (40/44-PIN)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDDATA0	SEG7 COM0	SEG6 COM0	—	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	—	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0
LCDDATA2	SEG23 COM0	SEG22 COM0	—	SEG20 COM0	SEG19 COM0	SEG18 COM0	—	—
LCDDATA3	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
LCDDATA4	—	—	—	—	—	SEG34 COM0	SEG33 COM0	SEG32 COM0
LCDDATA5	—	—	—	—	—	—	—	—
LCDDATA6	SEG7 COM1	SEG6 COM1	—	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1
LCDDATA7	SEG15 COM1	SEG14 COM1	SEG13 COM1	—	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1
LCDDATA8	SEG23 COM1	SEG22 COM1	—	SEG20 COM1	SEG19 COM1	SEG18 COM1	—	—
LCDDATA9	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
LCDDATA10	—	—	—	—	—	SEG34 COM1	SEG33 COM1	SEG32 COM1
LCDDATA11	—	—	—	—	—	—	—	—
LCDDATA12	SEG7 COM2	SEG6 COM2	—	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2
LCDDATA13	SEG15 COM2	SEG14 COM2	SEG13 COM2	—	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2
LCDDATA14	SEG23 COM2	SEG22 COM2	—	SEG20 COM2	SEG19 COM2	SEG18 COM2	—	—
LCDDATA15	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
LCDDATA16	—	—	—	—	—	SEG34 COM2	SEG33 COM2	SEG32 COM2
LCDDATA17	—	—	—	—	—	—	—	—
LCDDATA18	SEG7 COM3	SEG6 COM3	—	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3
LCDDATA19	SEG15 COM3	SEG14 COM3	SEG13 COM3	—	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3
LCDDATA20	SEG23 COM3	SEG22 COM3	—	SEG20 COM3	SEG19 COM3	SEG18 COM3	—	—
LCDDATA21	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3
LCDDATA22	—	—	—	—	—	SEG34 COM3	SEG33 COM3	SEG32 COM3
LCDDATA23	—	—	—	—	—	—	—	—
LCDDATA24	SEG7 COM4	SEG6 COM4	—	SEG4 COM4	SEG3 COM4	SEG2 COM4	SEG1 COM4	SEG0 COM4
LCDDATA25	SEG15 COM4	SEG14 COM4	SEG13 COM4	—	SEG11 COM4	SEG10 COM4	SEG9 COM4	SEG8 COM4
LCDDATA26	SEG23 COM4	SEG22 COM4	—	SEG20 COM4	SEG19 COM4	SEG18 COM4	—	—
LCDDATA27	SEG31 COM4	SEG30 COM4	SEG29 COM4	SEG28 COM4	SEG27 COM4	SEG26 COM4	SEG25 COM4	SEG24 COM4
LCDDATA28	—	—	—	—	—	SEG34 COM4	SEG33 COM4	SEG32 COM4
LCDDATA29	—	—	—	—	—	—	—	—
LCDDATA30	SEG7 COM5	SEG6 COM5	—	SEG4 COM5	SEG3 COM5	SEG2 COM5	SEG1 COM5	SEG0 COM5
LCDDATA31	SEG15 COM5	SEG14 COM5	SEG13 COM5	—	SEG11 COM5	SEG10 COM5	SEG9 COM5	SEG8 COM5
LCDDATA32	SEG23 COM5	SEG22 COM5	—	SEG20 COM5	SEG19 COM5	SEG18 COM5	—	—
LCDDATA33	SEG31 COM5	SEG30 COM5	SEG29 COM5	SEG28 COM5	SEG27 COM5	SEG26 COM5	SEG25 COM5	SEG24 COM5
LCDDATA34	—	—	—	—	—	SEG34 COM5	SEG33 COM5	SEG32 COM5
LCDDATA35	—	—	—	—	—	—	—	—
LCDDATA36	SEG7 COM6	SEG6 COM6	—	SEG4 COM6	SEG3 COM6	SEG2 COM6	SEG1 COM6	SEG0 COM6
LCDDATA37	SEG15 COM6	SEG14 COM6	SEG13 COM6	—	SEG11 COM6	SEG10 COM6	SEG9 COM6	SEG8 COM6
LCDDATA38	SEG23 COM6	SEG22 COM6	—	SEG20 COM6	SEG19 COM6	SEG18 COM6	—	—
LCDDATA39	SEG31 COM6	SEG30 COM6	SEG29 COM6	SEG28 COM6	SEG27 COM6	SEG26 COM6	SEG25 COM6	SEG24 COM6
LCDDATA40	—	—	—	—	—	SEG34 COM6	SEG33 COM6	SEG32 COM6
LCDDATA41	—	—	—	—	—	—	—	—
LCDDATA42	SEG7 COM7	SEG6 COM7	—	SEG4 COM7	SEG3 COM7	SEG2 COM7	SEG1 COM7	SEG0 COM7
LCDDATA43	SEG15 COM7	SEG14 COM7	SEG13 COM7	—	SEG11 COM7	SEG10 COM7	SEG9 COM7	SEG8 COM7
LCDDATA44	SEG23 COM7	SEG22 COM7	—	SEG20 COM7	SEG19 COM7	SEG18 COM7	—	—
LCDDATA45	SEG31 COM7	SEG30 COM7	SEG29 COM7	SEG28 COM7	SEG27 COM7	SEG26 COM7	SEG25 COM7	SEG24 COM7
LCDDATA46	—	—	—	—	—	SEG34 COM7	SEG33 COM7	SEG32 COM7
LCDDATA47	—	—	—	—	—	—	—	—

TABLE 35-5: LCDDATAX REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS (48-PIN)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDDATA0	SEG7 COM0	SEG6 COM0	—	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	—	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0
LCDDATA2	SEG23 COM0	SEG22 COM0	—	SEG20 COM0	SEG19 COM0	SEG18 COM0	—	—
LCDDATA3	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
LCDDATA4	—	—	—	—	—	SEG34 COM0	SEG33 COM0	SEG32 COM0
LCDDATA5	SEG47 COM0	SEG46 COM0	SEG45 COM0	SEG44 COM0	SEG43 COM0	SEG42 COM0	SEG41 COM0	SEG40 COM0
LCDDATA6	SEG7 COM1	SEG6 COM1	—	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1
LCDDATA7	SEG15 COM1	SEG14 COM1	SEG13 COM1	—	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1
LCDDATA8	SEG23 COM1	SEG22 COM1	—	SEG20 COM1	SEG19 COM1	SEG18 COM1	—	—
LCDDATA9	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
LCDDATA10	—	—	—	—	—	SEG34 COM1	SEG33 COM1	SEG32 COM1
LCDDATA11	SEG47 COM1	SEG46 COM1	SEG45 COM1	SEG44 COM1	SEG43 COM1	SEG42 COM1	SEG41 COM1	SEG40 COM1
LCDDATA12	SEG7 COM2	SEG6 COM2	—	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2
LCDDATA13	SEG15 COM2	SEG14 COM2	SEG13 COM2	—	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2
LCDDATA14	SEG23 COM2	SEG22 COM2	—	SEG20 COM2	SEG19 COM2	SEG18 COM2	—	—
LCDDATA15	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
LCDDATA16	—	—	—	—	—	SEG34 COM2	SEG33 COM2	SEG32 COM2
LCDDATA17	SEG47 COM2	SEG46 COM2	SEG45 COM2	SEG44 COM2	SEG43 COM2	SEG42 COM2	SEG41 COM2	SEG40 COM2
LCDDATA18	SEG7 COM3	SEG6 COM3	—	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3
LCDDATA19	SEG15 COM3	SEG14 COM3	SEG13 COM3	—	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3
LCDDATA20	SEG23 COM3	SEG22 COM3	—	SEG20 COM3	SEG19 COM3	SEG18 COM3	—	—
LCDDATA21	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3
LCDDATA22	—	—	—	—	—	SEG34 COM3	SEG33 COM3	SEG32 COM3
LCDDATA23	SEG47 COM3	SEG46 COM3	SEG45 COM3	SEG44 COM3	SEG43 COM3	SEG42 COM3	SEG41 COM3	SEG40 COM3
LCDDATA24	SEG7 COM4	SEG6 COM4	—	SEG4 COM4	SEG3 COM4	SEG2 COM4	SEG1 COM4	SEG0 COM4
LCDDATA25	SEG15 COM4	SEG14 COM4	SEG13 COM4	—	SEG11 COM4	SEG10 COM4	SEG9 COM4	SEG8 COM4
LCDDATA26	SEG23 COM4	SEG22 COM4	—	SEG20 COM4	SEG19 COM4	SEG18 COM4	—	—
LCDDATA27	SEG31 COM4	SEG30 COM4	SEG29 COM4	SEG28 COM4	SEG27 COM4	SEG26 COM4	SEG25 COM4	SEG24 COM4
LCDDATA28	—	—	—	—	—	SEG34 COM4	SEG33 COM4	SEG32 COM4
LCDDATA29	SEG47 COM4	SEG46 COM4	SEG45 COM4	SEG44 COM4	SEG43 COM4	SEG42 COM4	SEG41 COM4	SEG40 COM4
LCDDATA30	SEG7 COM5	SEG6 COM5	—	SEG4 COM5	SEG3 COM5	SEG2 COM5	SEG1 COM5	SEG0 COM5
LCDDATA31	SEG15 COM5	SEG14 COM5	SEG13 COM5	—	SEG11 COM5	SEG10 COM5	SEG9 COM5	SEG8 COM5
LCDDATA32	SEG23 COM5	SEG22 COM5	—	SEG20 COM5	SEG19 COM5	SEG18 COM5	—	—
LCDDATA33	SEG31 COM5	SEG30 COM5	SEG29 COM5	SEG28 COM5	SEG27 COM5	SEG26 COM5	SEG25 COM5	SEG24 COM5
LCDDATA34	—	—	—	—	—	SEG34 COM5	SEG33 COM5	SEG32 COM5
LCDDATA35	SEG47 COM5	SEG46 COM5	SEG45 COM5	SEG44 COM5	SEG43 COM5	SEG42 COM5	SEG41 COM5	SEG40 COM5
LCDDATA36	SEG7 COM6	SEG6 COM6	—	SEG4 COM6	SEG3 COM6	SEG2 COM6	SEG1 COM6	SEG0 COM6
LCDDATA37	SEG15 COM6	SEG14 COM6	SEG13 COM6	—	SEG11 COM6	SEG10 COM6	SEG9 COM6	SEG8 COM6
LCDDATA38	SEG23 COM6	SEG22 COM6	—	SEG20 COM6	SEG19 COM6	SEG18 COM6	—	—
LCDDATA39	SEG31 COM6	SEG30 COM6	SEG29 COM6	SEG28 COM6	SEG27 COM6	SEG26 COM6	SEG25 COM6	SEG24 COM6
LCDDATA40	—	—	—	—	—	SEG34 COM6	SEG33 COM6	SEG32 COM6
LCDDATA41	SEG47 COM6	SEG46 COM6	SEG45 COM6	SEG44 COM6	SEG43 COM6	SEG42 COM6	SEG41 COM6	SEG40 COM6
LCDDATA42	SEG7 COM7	SEG6 COM7	—	SEG4 COM7	SEG3 COM7	SEG2 COM7	SEG1 COM7	SEG0 COM7
LCDDATA43	SEG15 COM7	SEG14 COM7	SEG13 COM7	—	SEG11 COM7	SEG10 COM7	SEG9 COM7	SEG8 COM7
LCDDATA44	SEG23 COM7	SEG22 COM7	—	SEG20 COM7	SEG19 COM7	SEG18 COM7	—	—
LCDDATA45	SEG31 COM7	SEG30 COM7	SEG29 COM7	SEG28 COM7	SEG27 COM7	SEG26 COM7	SEG25 COM7	SEG24 COM7
LCDDATA46	—	—	—	—	—	SEG34 COM7	SEG33 COM7	SEG32 COM7
LCDDATA47	SEG47 COM7	SEG46 COM7	SEG45 COM7	SEG44 COM7	SEG43 COM7	SEG42 COM7	SEG41 COM7	SEG40 COM7

FIGURE 35-19: TYPE-B WAVEFORMS IN 1/8 MUX, 1/3 BIAS DRIVE



37.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- Byte Oriented
- Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 37-3 lists the instructions recognized by the MPASM™ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine entry takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

37.1 Read-Modify-Write Operations

Any WRITE instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the working (W) register, or the originating file register, depending on the state of the destination designator 'd' (see Table 37-1 for more information).

TABLE 37-1: OPCODE FIELD DESCRIPTIONS

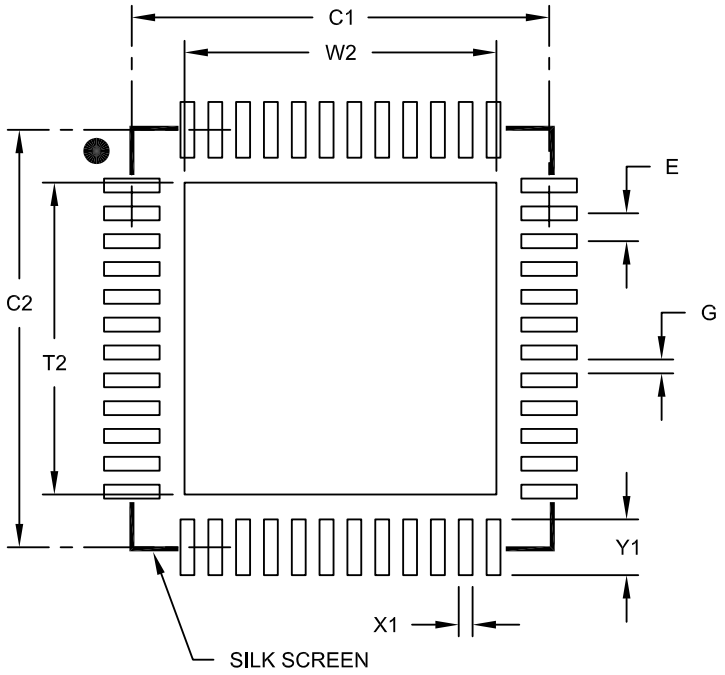
Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f.
n	FSR or INDF number. (0-1)
mm	Prepost increment-decrement mode selection

TABLE 37-2: ABBREVIATION DESCRIPTIONS

Field	Description
PC	Program Counter
$\overline{TO}$	Time-Out bit
C	Carry bit
DC	Digit Carry bit
Z	Zero bit
$\overline{PD}$	Power-Down bit

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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