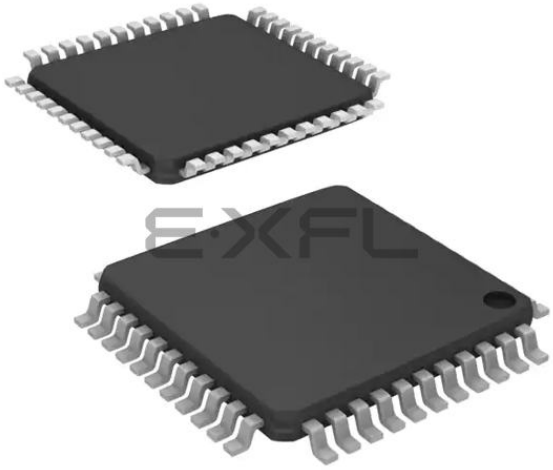

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Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 31x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
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TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RC0	15	30	32	34	—	—	—	—	—	T1CKI(1) SMTWIN1(1)	—	—	—	—	—	—	—	—	IOCC0	—	Y	SOSCO
RC1	16	31	35	35	—	—	—	—	—	SMTSIG1(1) T4IN(1)	CCP2(1)	—	—	—	—	—	—	—	IOCC1	—	Y	SOSCI
RC2	17	32	36	36	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM2 SEG18	IOCC2	—	Y	—
RC3	18	33	37	37	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG19	IOCC3	—	Y	—
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG20	IOCC4	—	Y	—
RC6	25	40	44	44	ANC6	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	SEG22 VLCD2	IOCC6	—	Y	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1)	—	—	SEG23 VLCD1	IOCC7	—	Y	—
RD0	19	34	38	38	AND0	—	—	—	—	—	—	—	—	—	—	—	—	SEG24	—	—	Y	—
RD1	20	35	39	39	AND1	—	—	—	—	—	—	—	—	—	—	—	—	SEG25	—	—	Y	—
RD2	21	36	40	40	AND2	—	—	—	—	—	—	—	—	—	—	—	—	COM5 SEG26	—	—	Y	—
RD3	22	37	41	41	AND3	—	—	—	—	—	—	—	—	—	—	—	—	COM4 SEG27	—	—	Y	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	SEG28	—	—	Y	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	SEG29	—	—	Y	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	SEG30	—	—	Y	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	SEG31	—	—	Y	—
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	SEG32	—	—	Y	—
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	COM6 SEG33	—	—	Y	—
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	COM7 SEG34	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	—	Y	$\overline{MCLR}$

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
VLCD3	24	39	43	43	—	—	—	—	—	—	—	—	—	—	—	—	—	VLCD3	—	—	—	—
VDD	11 32	7 26	7 28	7 28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	12 31	6 27	6 29	6 30	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 1-2: PIC16(L)F19155/56 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC0/T1CKI(1)/SMTWIN1(1)/IOCC0/SOSCO	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	T1CKI(1)	—	—	Timer1 clock input.
	SMTWIN1(1)	—	—	SMT window input.
	IOCC0	TTL/ST	—	Interrupt-on-change input.
	SOSCO	#VALUE!	AN	32.768 kHz secondary oscillator crystal driver output.
RC1/T4IN(1)/SMTSIG1(1)/CCP2(1)/IOCC1/SOSCI	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	T4IN(1)	—	—	Timer4 external input.
	SMTSIG1(1)	—	—	SMT signal input.
	CCP2(1)	—	—	CCP Capture Input.
	IOCC1	TTL/ST	—	Interrupt-on-change input.
	SOSCI	—	—	32.768 kHz secondary oscillator crystal driver input.
RC2/CCP1(1)/IOCC2/ANC2/SEG18/COM2	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	CCP1(1)	—	—	CCP Capture Input.
	IOCC2	TTL/ST	—	Interrupt-on-change input.
	ANC2	AN	—	ADC Channel input.
	SEG18	—	AN	LCD Analog output.
	COM2	—	AN	LCD Driver Common Outputs.
RC3/T2IN/SCL(3,4)/SCK(1)/SEG19	RC3	TTL/ST	CMOS/OD	General purpose I/O.
	T2IN(1)	—	—	Timer2 external input.
	SCL(3,4)	I^2C	OD	MSSP I^2Cclock input/output.
	SCK(1)	TTL/ST	—	MSSP SPI clock input/output
	IOCC3	TTL/ST	—	Interrupt-on-change input.
	ANC3	AN	—	ADC Channel input.
	SEG19	—	AN	LCD Analog output.
RC4/SDA(3,4)/SDI(1)/IOCC4/ANC4/SEG20	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	SDA(3,4)	TTL/ST	—	MSSP I^2C data input/output.
	SDI(1)	I^2C	OD	MSSP SPI serial data in.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
	ANC4	AN	—	ADC Channel input.
	SEG20	—	AN	LCD Analog output.
RC6/CK1(3)/TX1(1)/IOCC6/ANC6/SEG22/COM5/VLCD2	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	CK1(3)	—	—	EUSART synchronous clock out
	TX1(1)	—	—	EUSART asynchronous TX data out
	IOCC6	TTL/ST	—	Interrupt-on-change input.
	ANC6	AN	—	ADC Channel input.
	SEG22	—	AN	LCD Analog output.
	COM5	—	AN	LCD Driver Common Outputs.
	VLCD2	AN	—	LCD analog input

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input'; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 17											
CPU CORE REGISTERS; see Table 4-3 for specifics											
88Ch	CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE2	DOZE1	DOZE0	0000 -000	0000 -000
88Dh	OSCCON1	—	NOSC<2:0>			NDIV<3:0>				-qqq 0000	-qqq 0000
88Eh	OSCCON2	—	COSC<2:0>			CDIV<3:0>				-qqq qqqq	-qqq qqqq
88Fh	OSCCON3	CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	00-- 00--	00-- 00--
890h	OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	q000 qq-0	qqqq qq-q
891h	OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	0000 00--	0000 00--
892h	OSCTUNE	—	—	HFTUN<5:0>						1000 0000	1000 0000
893h	OSCFRQ	—	—	—	—	—	HFFRQ<2:0>			---- -qqq	---- -qqq
894h	ACTCON	ACTEN	ACTUD	—	—	ACTLOCK	—	ACTORS	—	00-- 0-0-	00-- 0-0-
895h	—	Unimplemented								---- ----	---- ----
896h	—	Unimplemented								---- ----	---- ----
897h	—	Unimplemented								---- ----	---- ----
898h	—	Unimplemented								---- ----	---- ----
899h	—	Unimplemented								---- ----	---- ----
89Ah	—	Unimplemented								---- ----	---- ----
89Bh	—	Unimplemented								---- ----	---- ----
89Ch	—	Unimplemented								---- ----	---- ----
89Dh	—	Unimplemented								---- ----	---- ----
89Eh	—	Unimplemented								---- ----	---- ----
89Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 58 (continued)											
1D2Ah	LCDDATA18	S15C3	S14C3	S13C3	—	SE11C3	S10C3	S09C3	S08C3	0000 0000	0000 0000
1D2Bh	LCDDATA19	S23C3	S22C3	—	S20C3	S19C3	S18C3	—	—	0000 0000	0000 0000
1D2Ch	LCDDATA20	S31C3	S30C3	S29C3	S28C3	S27C3	S26C3	S25C3	S24C3	0000 0000	0000 0000
1D2Dh	LCDDATA21	—	—	—	—	—	S34C3	S33C3	S32C3	0000 0000	0000 0000
1D2Eh	LCDDATA22	S47C3	S46C3	S45C3	S44C3	S43C3	S42C3	S41C3	S40C3	0000 0000	0000 0000
1D2Fh	LCDDATA23	S07C4	S06C4	—	S04C4	S03C4	S02C4	S01C4	S00C4	0000 0000	0000 0000
1D30h	LCDDATA24	S15C4	S14C4	S13C4	—	S11C4	S10C4	S09C4	S08C4	0000 0000	0000 0000
1D31h	LCDDATA25	S23C4	S22C4	—	S20C4	S19C4	S18C4	—	—	0000 0000	0000 0000
1D32h	LCDDATA26	S31C4	S30C4	S29C4	S28C4	S27C4	S26C4	S25C4	S24C4	0000 0000	0000 0000
1D33h	LCDDATA27	—	—	—	—	—	S34C4	S33C4	S32C4	0000 0000	0000 0000
1D34h	LCDDATA28	S47C4	S46C4	S45C4	S44C4	S43C4	S42C4	S41C4	S40C4	0000 0000	0000 0000
1D35h	LCDDATA29	S07C5	S06C5	—	S04C5	S03C5	S02C5	S01C5	S00C5	0000 0000	0000 0000
1D36h	LCDDATA30	S15C5	S14C5	S13C5	—	S11C5	S10C5	S09C5	S08C5	0000 0000	0000 0000
1D37h	LCDDATA31	S23C5	S22C5	—	S20C5	S19C5	S18C5	—	—	0000 0000	0000 0000
1D38h	LCDDATA32	S31C5	S30C5	S29C5	S28C5	S27C5	S26C5	S25C5	S24C5	0000 0000	0000 0000
1D39h	LCDDATA33	—	—	—	—	—	S34C5	S33C5	S32C5	0000 0000	0000 0000
1D3Ah	LCDDATA34	S47C5	S46C5	S45C5	S44C5	S43C5	S42C5	S41C5	S40C5	0000 0000	0000 0000
1D3Bh	LCDDATA35	S07C6	S06C6	—	S04C6	S03C6	S02C6	S01C6	S00C6	0000 0000	0000 0000
1D3Ch	LCDDATA36	S15C6	S14C6	S13C6	—	S11C6	S10C6	S09C6	S08C6	0000 0000	0000 0000
1D3Dh	LCDDATA37	S23C6	S22C6	—	S20C6	S19C6	S18C6	—	—	0000 0000	0000 0000
1D3Eh	LCDDATA38	S31C6	S30C6	S29C6	S28C6	S27C6	S26C6	S25C6	S24C6	0000 0000	0000 0000
1D3Fh	LCDDATA39	—	—	—	—	—	S34C6	S33C6	S32C6	0000 0000	0000 0000
1D40h	LCDDATA40	S47C6	S46C6	S45C6	S44C6	S43C6	S42C6	S41C6	S40C6	0000 0000	0000 0000
1D41h	LCDDATA41	S07C7	S06C7	—	S04C7	S03C7	S02C7	S01C7	S00C7	0000 0000	0000 0000
1D42h	LCDDATA42	S15C7	S14C7	S13C7	—	S11C7	S10C7	S09C7	S08C7	0000 0000	0000 0000
1D43h	LCDDATA43	S23C7	S22C7	—	S20C7	S19C7	S18C7	—	—	0000 0000	0000 0000
1D44h	LCDDATA44	S31C7	S30C7	S29C7	S28C7	S27C7	S26C7	S25C7	S24C7	0000 0000	0000 0000
1D45h	LCDDATA45	—	—	—	—	—	S34C7	S33C7	S32C7	0000 0000	0000 0000
1D46h	LCDDATA46	S47C7	S46C7	S45C7	S44C7	S43C7	S42C7	S41C7	S40C7	0000 0000	0000 0000
1D47h	LCDDATA47	S07C0	S06C0	—	S04C0	S03C0	S02C0	S01C0	S00C0	0000 0000	0000 0000

10.6 Register Definitions: Interrupt Control

REGISTER 10-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R/W-1/1
GIE	PEIE	—	—	—	—	—	INTEDG
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-3: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail Interrupt
0 = Disables the Oscillator Fail Interrupt

bit 6 **CSWIE:** Clock Switch Complete Interrupt Enable bit
1 = The clock switch module interrupt is enabled
0 = The clock switch module interrupt is disabled

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **ADTIE:** Analog-to-Digital Converter (ADC) Threshold Compare Interrupt Enable bit
1 = Enables the ADC threshold compare interrupt
0 = Disables the ADC threshold compare interrupt

bit 0 **ADIE:** Analog-to-Digital Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

REGISTER 12-2: WDTCON1: WATCHDOG TIMER CONTROL REGISTER 1

U-0	R/W(3)-q/q(1)	R/W(3)-q/q(1)	R/W(3)-q/q(1)	U-0	R/W(4)-q/q(2)	R/W(4)-q/q(2)	R/W(4)-q/q(2)
—	WDTCS<2:0>			—	WINDOW<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **WDTCS<2:0>:** Watchdog Timer Clock Select bits

111 = Reserved
•
•
•
010 = SOSC 32.768 kHz
001 = MFINTOSC 31.25 kHz
000 = LFINTOSC 31 kHz

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **WINDOW<2:0>:** Watchdog Timer Window Select bits

WINDOW<2:0>	Window delay Percent of time	Window opening Percent of time
111	N/A	100
110	12.5	87.5
101	25	75
100	37.5	62.5
011	50	50
010	62.5	37.5
001	75	25
000	87.5	12.5

Note 1: If WDTCCS <2:0> in CONFIG3 = 111, the Reset value of WDTCS<2:0> is 000.

2: The Reset value of WINDOW<2:0> is determined by the value of WDTCWS<2:0> in the CONFIG3 register.

3: If WDTCCS<2:0> in CONFIG3 ≠ 111, these bits are read-only.

4: If WDTCWS<2:0> in CONFIG3 ≠ 111, these bits are read-only.

TABLE 14-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	229
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	229
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	230
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	230
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	231
ODCONB	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	231
SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	232
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	232
HIDRVB	—	—	—	—	—	—	HIDB1	—	232

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

21.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC1) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DAC1OUT pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DAC1EN bit of the DAC1CON0 register.

21.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DAC1R<4:0> bits of the DAC1CON1 register.

The DAC output voltage is determined by Equation 21-1:

EQUATION 21-1: DAC OUTPUT VOLTAGE

$$V_{OUT} = \left(V_{SOURCE+} - V_{SOURCE-} \times \frac{DAC1R\langle 4:0 \rangle}{2^5} \right) + (V_{SOURCE-})$$

$$V_{SOURCE+} = V_{DD} \text{ or } V_{REF+} \text{ or } FVR$$

$$V_{SOURCE-} = V_{SS} \text{ or } V_{REF-}$$

21.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in Table 39-16.

21.3 DAC Voltage Reference Output

The DAC voltage can be output to the DAC1OUT1/2 pins by setting the DAC1OE1/2 bits of the DAC1CON0 register, respectively. Selecting the DAC reference voltage for output on the DAC1OUT1/2 pins automatically overrides the digital output buffer and digital input threshold detector functions, disables the weak pull-up, and disables the current-controlled drive function of that pin. Reading the DAC1OUT1/2 pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to the DAC1OUT1/2 pins. Figure 21-2 shows an example buffering technique.

When ALRMRPT = 00 and the CHIME bit = 0 (ALRMCON), the repeat function is disabled and only a single alarm will occur. The alarm can be repeated up to 255 times by loading the ALRMRPT register with FFh with the CHIME bit = 1.

After each alarm is issued, the ALRMRPT register is decremented by one. Once the register has reached '00', the alarm will be issued one last time. After the alarm is issued a last time, the ALRMEN bit is cleared automatically and the alarm turned off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the ALRMRPT register reaches '00', it will roll over to FFh and continue counting when CHIME = 1.

24.2.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated and the RTCCIF bit is set. Additionally, an alarm pulse output is provided that operates at half the frequency of the alarm.

The alarm pulse output is completely synchronous with the RTCC clock and can be used as a trigger clock to other peripherals.

24.3 VBAT Operation

This device is equipped with a VBAT pin that allows the user to connect an external battery or Supercap. In the event of the VDD supply failing or dropping below the supply voltage level on the VBAT pin, the power source connected to the VBAT pin will keep the SOSC and RTCC blocks running. VBAT is enabled via the VBATEN bit in Configuration Word 1.

24.4 Sleep Mode

The timer and alarm continue to operate while in Sleep mode. The operation of the alarm is not affected by Sleep, as an alarm event can always wake-up the CPU. Idle mode does not affect the operation of the timer or alarm.

24.5 Resets

The RTCCON and RTCCAL registers are only reset on a POR or BOR event. Only a POR or BOR event will turn the RTCC module off if VBAT is invalid.

If the VBAT module is enabled and active during a POR or BOR, the RTCCON and RTCCAL registers will not reset. The RTCC module will continue with normal operation during the reset.

The timer prescaler values can only be reset by writing to the SECONDS register. No device reset will affect the prescaler values.

26.3 Timer Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

26.4 Secondary Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins SOSCI (input) and SOSCO (amplifier output). This internal circuit is designed to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the SOSCEN bit of the OSCEN register. The oscillator will continue to run during Sleep.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, SOSCEN should be set and a suitable delay observed prior to using Timer1 with the SOSC source. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

26.5 Timer Operation in Asynchronous Counter Mode

If the control bit $\overline{\text{SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 26.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

26.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

26.6 Timer Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using the time gate circuitry. This is also referred to as Timer Gate Enable.

The timer gate can also be driven by multiple selectable sources.

26.6.1 TIMER GATE ENABLE

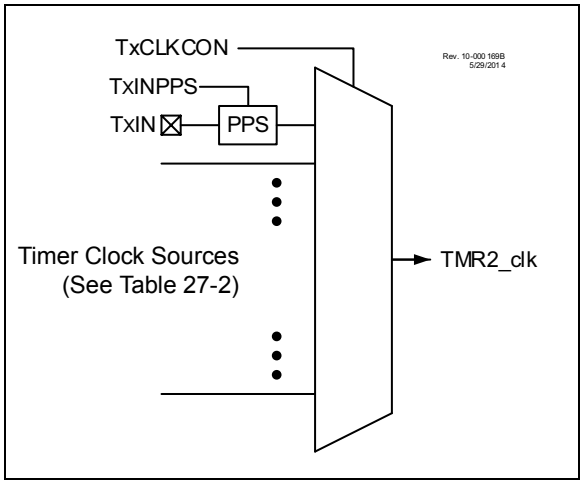
The Timer Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer Gate Enable signal is enabled, the timer will increment on the rising edge of the Timer1 clock source. When Timer Gate Enable signal is disabled, the timer always increments, regardless of the GE bit. See Figure 26-3 for timing details.

TABLE 26-2: TIMER GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer Operation
↑	1	1	Counts
↑	1	0	Holds Count
↑	0	1	Holds Count
↑	0	0	Counts

FIGURE 27-2: TIMER2/4 CLOCK SOURCE BLOCK DIAGRAM



27.1 Timer2/4 Operation

Timer2 operates in three major modes:

- Free Running Period
- One-shot
- Monostable

Within each mode there are several options for starting, stopping, and reset. Table 27-1 lists the options.

In all modes, the TMR2 count register is incremented on the rising edge of the clock signal from the programmable prescaler. When TMR2 equals T2PR, a high level is output to the postscaler counter. TMR2 is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a TMR2 count Reset. In Gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the TMR2 count is reset on either the level or edge from the external source.

The TMR2 and T2PR registers are both directly readable and writable. The TMR2 register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset
- External Reset Source event that resets the timer.

Note:	TMR2 is not cleared when T2CON is written.

27.1.1 FREE RUNNING PERIOD MODE

The value of TMR2 is compared to that of the Period register, T2PR, on each TMR2_clk cycle. When the two values match, the comparator resets the value of TMR2 to 00h on the next rising TMR2_clk edge and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS<4:0> bits of the TMRxCON1 register, a one TMR2_clk period wide pulse occurs on the TMR2_postscaled output, and the postscaler count is cleared.

27.1.2 ONE-SHOT MODE

The One-Shot mode is identical to the Free Running Period mode except that the ON bit is cleared and the timer is stopped when TMR2 matches T2PR and will not restart until the T2ON bit is cycled off and on. Postscaler OUTPS<4:0> values other than 0 are meaningless in this mode because the timer is stopped at the first period event and the postscaler is reset when the timer is restarted.

27.1.3 MONOSTABLE MODE

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

27.2 Timer2/4 Output

The Timer2 module's primary output is TMR2_postscaled, which pulses for a single TMR2_clk period when the postscaler counter matches the value in the OUTPS bits of the TMR2CON register. The T2PR postscaler is incremented each time the TMR2 value matches the T2PR value. This signal can be selected as an input to several other input modules:

- The ADC module, as an Auto-conversion Trigger
- COG, as an auto-shutdown source

In addition, the Timer2 is also used by the CCP module for pulse generation in PWM mode. Both the actual TMR2 value as well as other internal signals are sent to the CCP module to properly clock both the period and pulse width of the PWM signal. See **Section 29.0 "Capture/Compare/PWM Modules"** for more details on setting up Timer2/4 for use with the CCP, as well as the timing diagrams in **Section 27.5 "Operation Examples"** for examples of how the varying Timer2 modes affect CCP PWM output.

27.3 External Reset Sources

In addition to the clock source, the Timer2 also takes in an external Reset source. This external Reset source is selected for Timer2 with the T2RST register. This source can control starting and stopping of the timer, as well as resetting the timer, depending on which mode the timer is in. The mode of the timer is controlled by the MODE<4:0> bits of the TMRxHLT register. Edge-Triggered modes require six Timer clock periods between external triggers. Level-Triggered modes require the triggering level to be at least three Timer clock periods long. External triggers are ignored while in Debug Freeze mode.

28.0 SIGNAL MEASUREMENT TIMER (SMT)

The SMT is a 24-bit counter with advanced clock and gating logic, which can be configured for measuring a variety of digital signal parameters such as pulse width, frequency and duty cycle, and the time difference between edges on two signals.

Features of the SMT include:

- 24-bit timer/counter
  - Three 8-bit registers (SMTxTMRL/H/U)
  - Readable and writable
  - Optional 16-bit operating mode
- Two 24-bit measurement capture registers
- One 24-bit period match register
- Multi-mode operation, including relative timing measurement
- Interrupt on period match
- Multiple clock, gate and signal sources
- Interrupt on acquisition complete
- Ability to read current input values

REGISTER 31-3: CWG1DBR: CWG1 RISING DEAD-BAND COUNTER REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	DBR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DBR<5:0>:** Rising Event Dead-Band Value for Counter bits

REGISTER 31-4: CWG1DBF: CWG1 FALLING DEAD-BAND COUNTER REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	DBF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DBF<5:0>:** Falling Event Dead-Band Value for Counter bits

33.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

33.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

33.4 I²C MODE OPERATION

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC® microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

33.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

33.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I²C specification.

33.4.3 SDA AND SCL PINS

When selecting any I²C mode, the SCL and SDA pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note 1:	Any device pin can be selected for SDA and SCL functions with the PPS peripheral. These functions are bidirectional. The SDA input is selected with the SSPDATPPS registers. The SCL input is selected with the SSPCLKPPS registers. Outputs are selected with the RxyPPS registers. It is the user's responsibility to make the selections so that both the input and the output for each function is on the same pin.

FIGURE 33-34: BUS COLLISION DURING START CONDITION (SCL = 0)

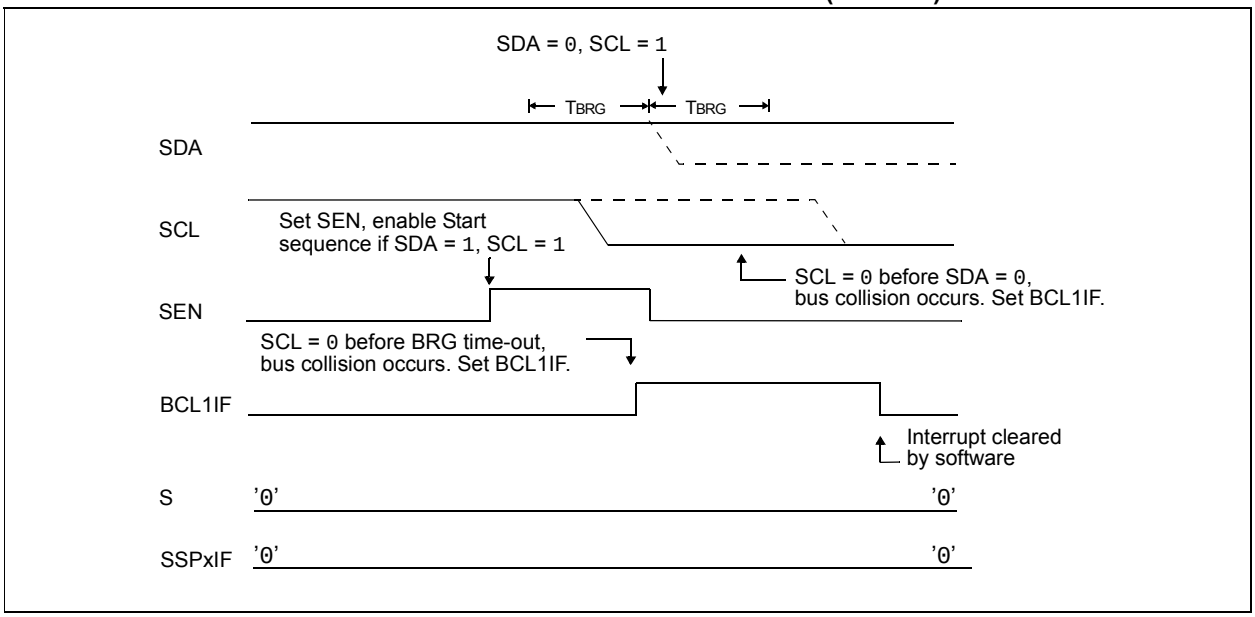


FIGURE 33-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION

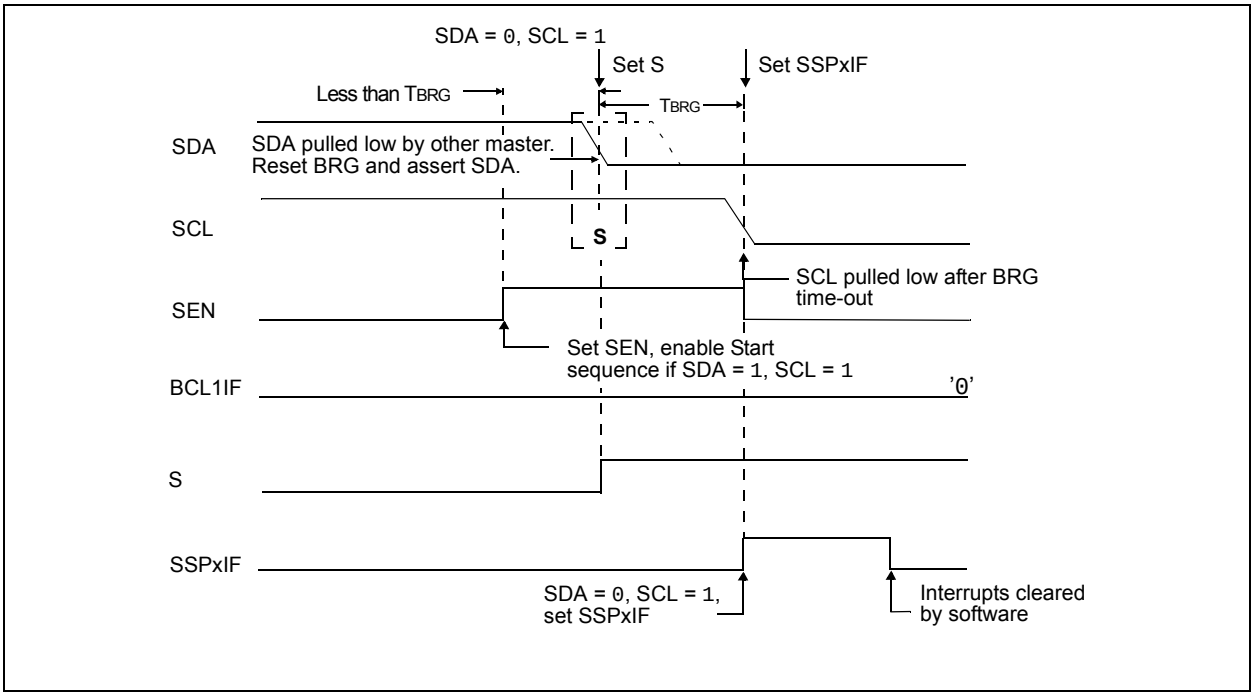
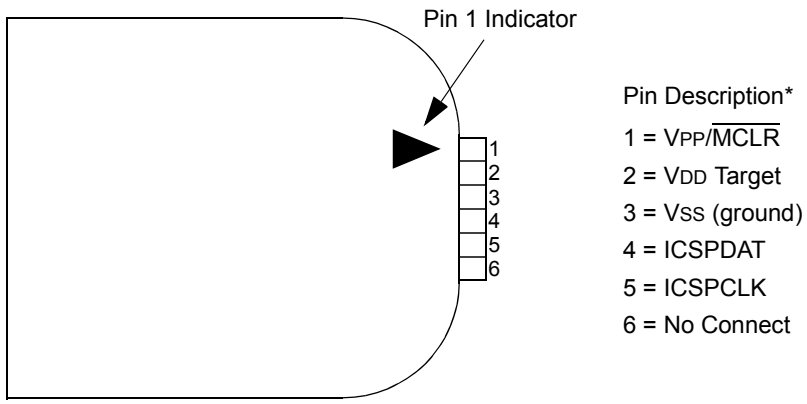
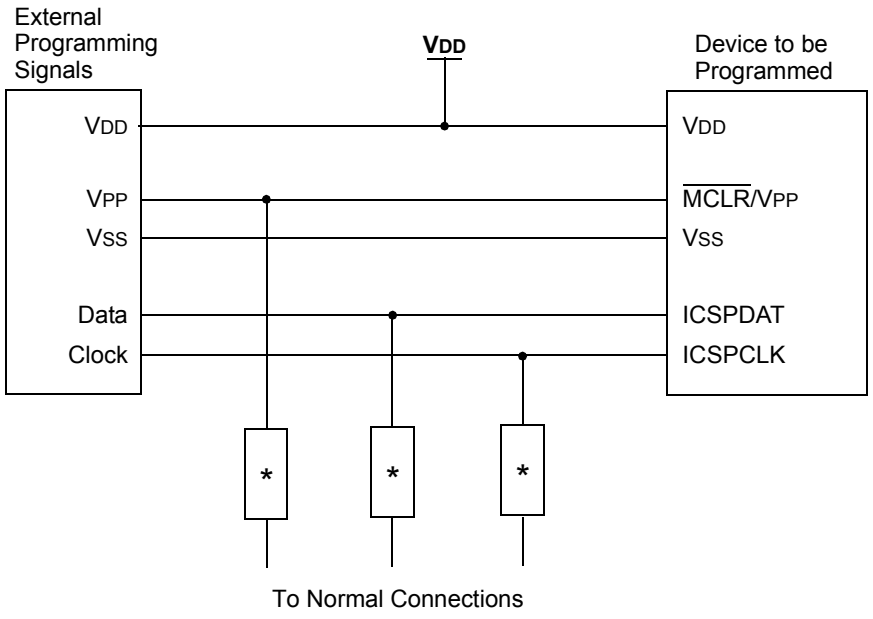


FIGURE 36-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE



* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 36-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING



* Isolation devices (as required).

FIGURE 39-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

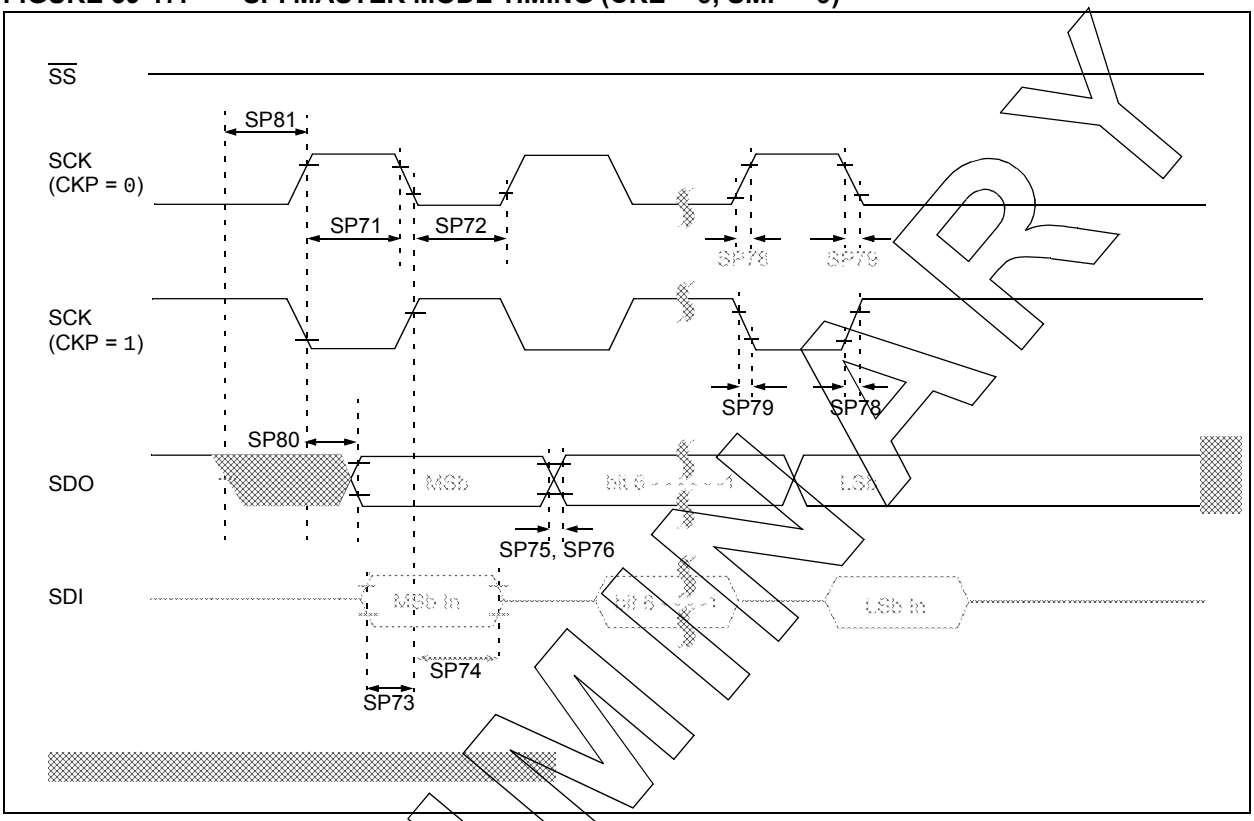
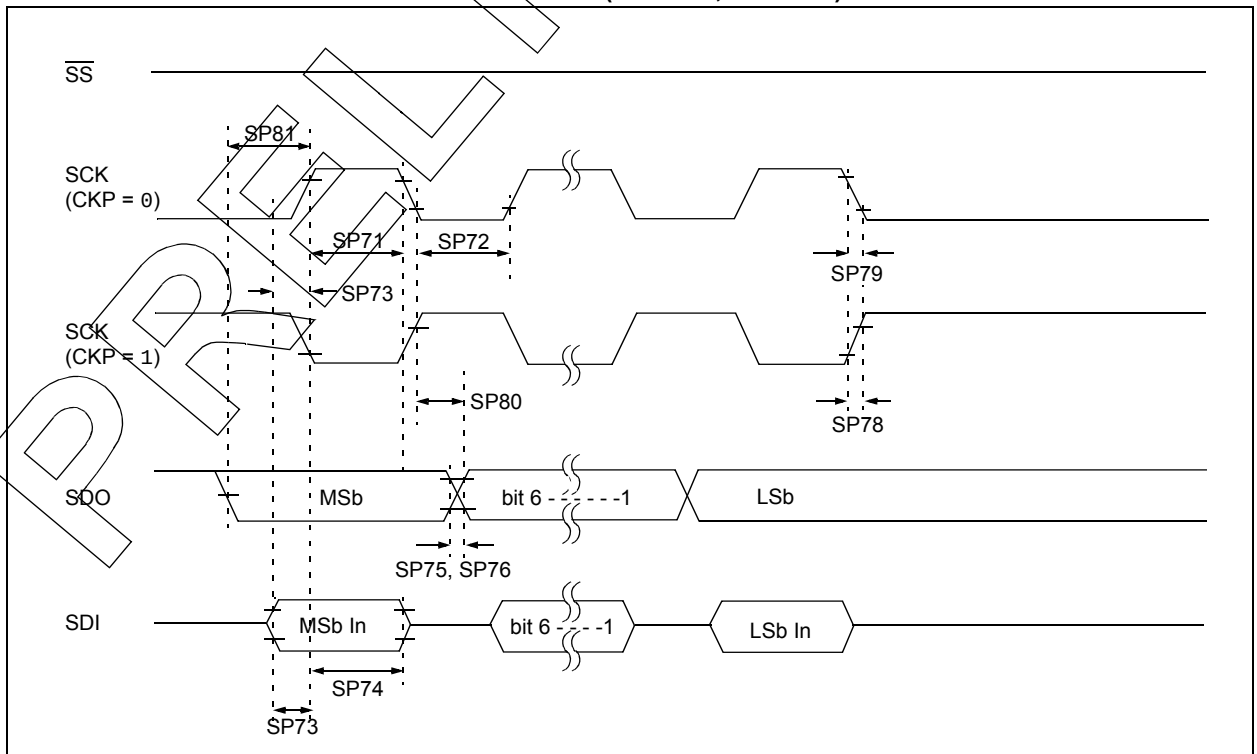


FIGURE 39-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 39-4 for load conditions.

41.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

41.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradeable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

41.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

41.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

41.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.