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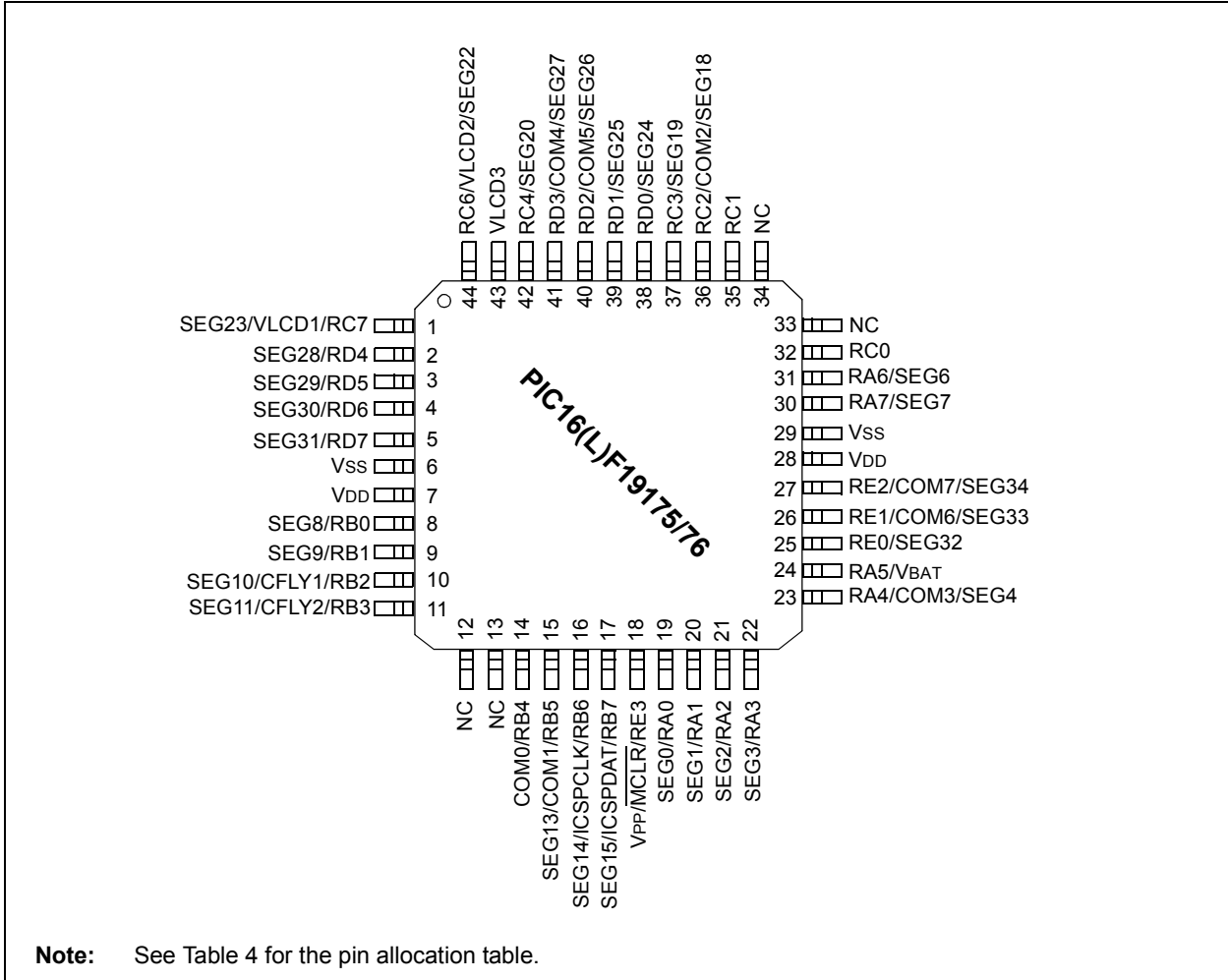
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19185-e-mv">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19185-e-mv</a>

# PIC16(L)F19155/56/75/76/85/86

**FIGURE 5: 44-PIN TQFP PIN DIAGRAM FOR PIC16(L)F19175/76**



# PIC16(L)F19155/56/75/76/85/86

**TABLE 1-3: PIC16(L)F19175/76 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RC0/T1CKI <sup>(1)</sup> /SMTWIN1 <sup>(1)</sup> /IOCC0/SOSCO	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	T1CKI <sup>(1)</sup>	—	—	Timer1 clock input.
	SMTWIN1 <sup>(1)</sup>	—	—	SMT window input.
	IOCC0	TTL/ST	—	Interrupt-on-change input.
	SOSCO	—	AN	32.768 kHz secondary oscillator crystal driver output.
RC1/T4IN <sup>(1)</sup> /SMTSIG1 <sup>(1)</sup> /CCP2 <sup>(1)</sup> /IOCC1/SOSCI	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	T4IN <sup>(1)</sup>	—	—	Timer4 external input.
	SMTSIG1 <sup>(1)</sup>	—	—	SMT signal input.
	CCP2 <sup>(1)</sup>	—	—	CCP Capture Input.
	IOCC1	TTL/ST	—	Interrupt-on-change input.
	SOSCI	—	—	32.768 kHz secondary oscillator crystal driver input.
RC2/CCP1 <sup>(1)</sup> /IOCC2/ANC2/SEG18/COM2	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	CCP1 <sup>(1)</sup>	—	—	CCP Capture Input.
	IOCC2	TTL/ST	—	Interrupt-on-change input.
	ANC2	AN	—	ADC Channel input.
	SEG18	—	AN	LCD Analog output.
	COM2	—	AN	LCD Driver Common Outputs.
RC3/T2IN <sup>(1)</sup> /SCL <sup>(3,4)</sup> /SCK <sup>(1)</sup> /SEG19	RC3	TTL/ST	CMOS/OD	General purpose I/O.
	T2IN <sup>(1)</sup>	—	—	Timer2 external input.
	SCL <sup>(3,4)</sup>	I <sup>2</sup> C	OD	MSSP I <sup>2</sup> C clock input/output.
	SCK <sup>(1)</sup>	TTL/ST	—	MSSP SPI clock input/output
	IOCC3	TTL/ST	—	Interrupt-on-change input.
	ANC3	AN	—	ADC Channel input.
	SEG19	—	AN	LCD Analog output.
RC4/SDA <sup>(3,4)</sup> /SDI <sup>(1)</sup> /IOCC4/ANC4/SEG20	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	SDA <sup>(3,4)</sup>	TTL/ST	—	MSSP I <sup>2</sup> C data input/output.
	SDI <sup>(1)</sup>	I <sup>2</sup> C	OD	MSSP SPI serial data in.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
	ANC4	AN	—	ADC Channel input.
	SEG20	—	AN	LCD Analog output.
RC6/CK1 <sup>(3)</sup> /TX1 <sup>(1)</sup> /IOCC6/ANC6/SEG22/VLCD2	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	CK1 <sup>(3)</sup>	—	—	EUSART synchronous clock out
	TX1 <sup>(1)</sup>	—	—	EUSART asynchronous TX data out
	IOCC6	TTL/ST	—	Interrupt-on-change input.
	ANC6	AN	—	ADC Channel input.
	SEG22	—	AN	LCD Analog output.
VLCD2	AN	—	LCD analog input	

**Legend:** AN = Analog input or output      CMOS = CMOS compatible input or output      OD = Open-Drain  
TTL = TTL compatible input'      ST = Schmitt Trigger input with CMOS levels      I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage      XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

**TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
<b>Bank 62 (Continued)</b>											
1F4Eh	ANSELC	ANSC7	ANSC6	—	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	1111 1111	1111 1111
1F4Fh	WPUC	WPUC7	WPUC6	—	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	0000 0000	0000 0000
1F50h	ODCONC	ODCC7	ODCC6	—	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000 0000	0000 0000
1F51h	SLRCONC	SLRC7	SLRC6	—	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	1111 1111	1111 1111
1F52h	INLVLC	INLVLC7	INLVLC6	—	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	1111 1111	1111 1111
1F53h	IOCCP	IOCCP7	IOCCP6	—	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	0000 0000	0000 0000
1F54h	IOCCN	IOCCN7	IOCCN6	—	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	0000 0000	0000 0000
1F55h	IOCCF	IOCCF7	IOCCF6	—	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	0000 0000	0000 0000
1F56h	—	Unimplemented								----	----
1F57h	—	Unimplemented								----	----
1F58h	—	Unimplemented								----	----
1F59h	ANSELD	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
1F5Ah	WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	0000 0000	0000 0000
1F5Bh	ODCOND	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000 0000	0000 0000
1F5Ch	SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	1111 1111	1111 1111
1F5Dh	INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	1111 1111	1111 1111
1F5Eh	—	Unimplemented								----	----
1F5Fh	—	Unimplemented								----	----
1F60h	—	Unimplemented								----	----
1F61h	—	Unimplemented								----	----
1F62h	—	Unimplemented								----	----
1F63h	—	Unimplemented								----	----

**Legend:** x = unknown, u = unchanged, c = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

**Note 1:** Unimplemented data memory locations, read as '0'.

## 5.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory are controlled independently. Internal access to the program memory is unaffected by any code protection setting.

### 5.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the CP bit in Configuration Words. When CP = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Self-writing the program memory is dependent upon the write protection setting. See **Section 5.4 "Write Protection"** for more information.

### 5.3.2 DATA MEMORY PROTECTION

The entire data EEPROM is protected from external reads and writes by the WRTD bit in the Configuration Words. When WRTD = 0, external reads and writes of EEPROM memory are inhibited and a read will return all '0's. The CPU can continue to read and write EEPROM memory, regardless of the protection bit settings.

## 5.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRTAPP, WRTSAF, WRTB, WRTC bits in Configuration Words (Register 5-4) define whether the corresponding region of the program memory block is protected or not.

## 5.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 13.4.7 "NVMREG Access to Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Words"** for more information on accessing these memory locations. For more information on checksum calculation, see the "*PIC16(L)F191XX Memory Programming Specification*" (DS40001880).

# PIC16(L)F19155/56/75/76/85/86

## REGISTER 8-3: PCON1: POWER CONTROL REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HC-1/u	R/W/HC-q/u
—	—	—	—	—	—	MEMV	VBATBOR
bit 7						bit 0	

### Legend:

HC = Bit is cleared by hardware

HS = Bit is set by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-m/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7-2 **Unimplemented:** Read as '0'.

bit 1 **MEMV:** Memory Violation Flag bit

1 = No Memory Violation Reset occurred or set to '1' by firmware

0 = A Memory Violation Reset occurred (set '0' in hardware when a Memory Violation occurs)

bit 0 **VBATBOR:** VBAT Brown-Out Reset Status Bit

1 = No VBAT Brown-out Reset occurred.

0 = A VBAT Brown-out Reset occurred.

## 8.17 VBAT System

The VBAT subsystem allows the RTCC and SOSC to run from a battery connected to the VBAT pin in the event of a VDD failure. Typically, the battery is a 3V coin cell, however the system is designed to operate over the entire VDD voltage range. If VDD is greater than VBAT, the RTCC and SOSC will be powered by VDD. If VDD is less than VBAT, the RTCC and SOSC will switch over to VBAT. See Table 4-5 and Table 4-8 for more information on the VBAT registers.

**Note:** It should be noted that in this second scenario, VDD may still be in the valid operating range, but anytime the VDD drops below VBAT, the RTCC and SOSC will switch over to VBAT. This means that in a system with a 3V battery and a 2.8V VDD, the RTCC and SOSC will run off VBAT even when VDD is present.

### 8.17.1 VBAT GPR SEMAPHORE REGISTERS

The VBAT voltage domain offers the user four registers: VB0GPR, VB1GPR, VB3GPR and VB4GPR. These registers can be used by firmware to write any information that needs to survive a VDD failure. As long as either VDD or VBAT is valid, these registers will hold the last value written.

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## REGISTER 14-5: WPUA: WEAK PULL-UP PORTA REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUA7	WPUA6	WPUA5 <sup>(2)</sup>	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0      **WPUA<7:0>**: Weak Pull-up Register bits<sup>(1)</sup>  
                   1 = Pull-up enabled  
                   0 = Pull-up disabled

- Note 1:** The weak pull-up device is automatically disabled if the pin is configured as an output.  
**2:** Bit not used when  $\overline{VBATEN} = 0$ .

## REGISTER 14-6: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCA7	ODCA6	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

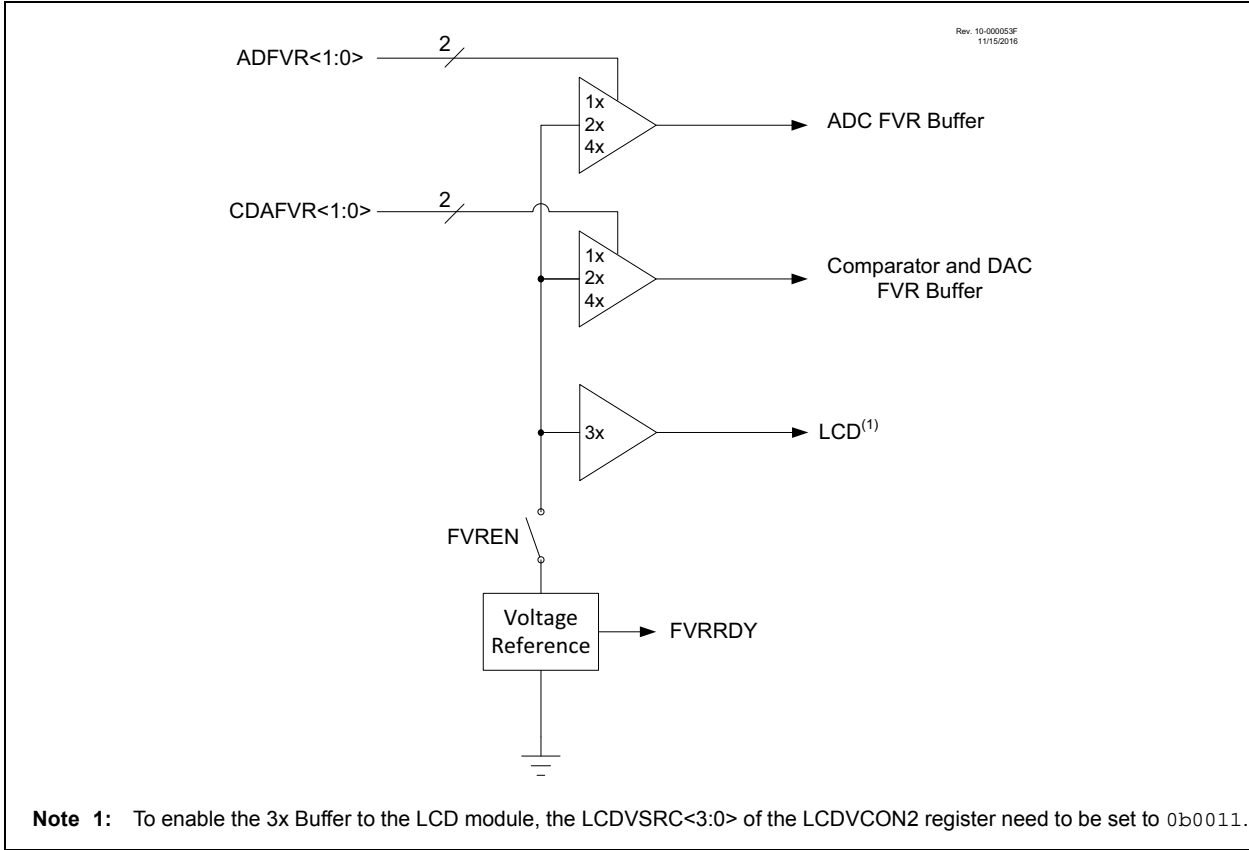
bit 7-6      **ODCA<7:6>**: PORTA Open-Drain Enable bits  
                   For RA<7:6> pins, respectively  
                   1 = Port pin operates as open-drain drive (sink current only)  
                   0 = Port pin operates as standard push-pull drive (source and sink current)

bit 5      **Unimplemented:** Read as '0'

bit 4-0      **ODCA<4:0>**: PORTA Open-Drain Enable bits  
                   For RA<4:0> pins, respectively  
                   1 = Port pin operates as open-drain drive (sink current only)  
                   0 = Port pin operates as standard push-pull drive (source and sink current)

# PIC16(L)F19155/56/75/76/85/86

**FIGURE 18-1: VOLTAGE REFERENCE BLOCK DIAGRAM**

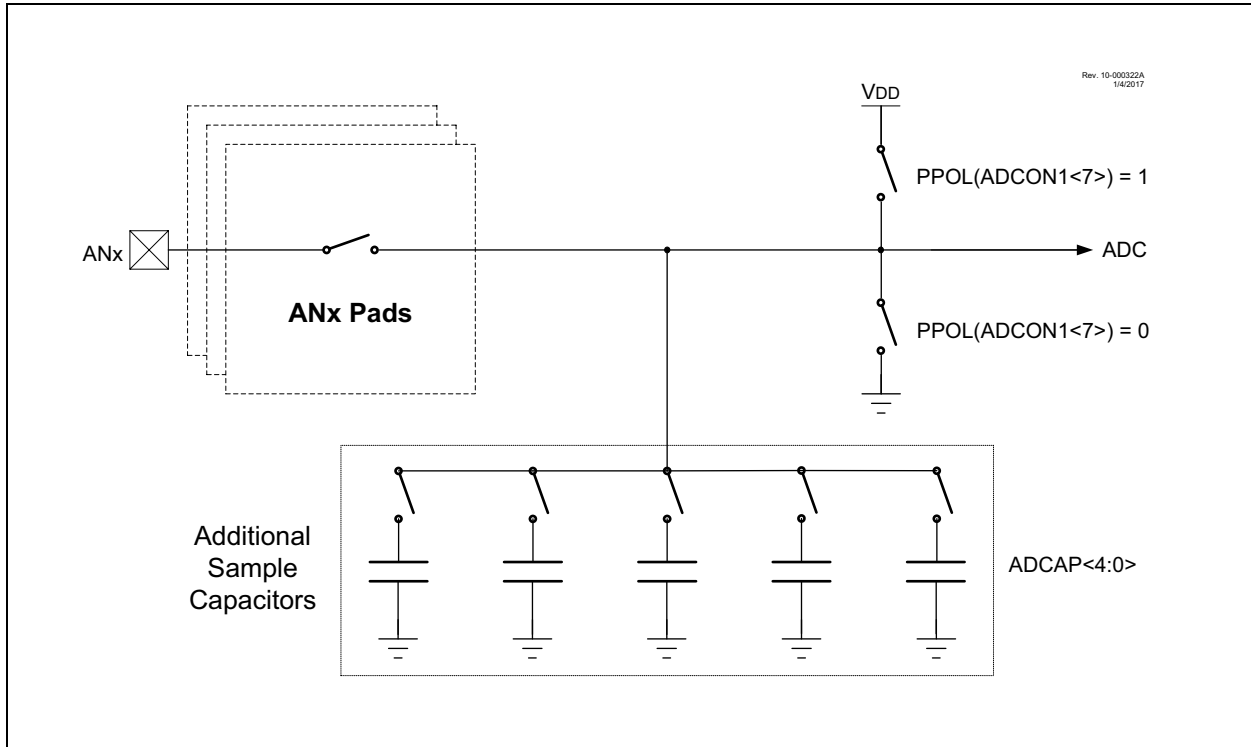




## 19.4 Capacitive Voltage Divider (CVD) Features

The ADC module contains several features that allow the user to perform a relative capacitance measurement on any ADC channel using the internal ADC sample and hold capacitance as a reference. This relative capacitance measurement can be used to implement capacitive touch or proximity sensing applications. Figure 19-6 shows the basic block diagram of the CVD portion of the ADC module.

**FIGURE 19-6: HARDWARE CAPACITIVE VOLTAGE DIVIDER BLOCK DIAGRAM**



## 26.3 Timer Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

## 26.4 Secondary Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins SOSC1 (input) and SOSCO (amplifier output). This internal circuit is designed to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the SOSSEN bit of the OSCEN register. The oscillator will continue to run during Sleep.

**Note:** The oscillator requires a start-up and stabilization time before use. Thus, SOSSEN should be set and a suitable delay observed prior to using Timer1 with the SOSC source. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

## 26.5 Timer Operation in Asynchronous Counter Mode

If the control bit SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 26.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”**).

**Note:** When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

### 26.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

## 26.6 Timer Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using the time gate circuitry. This is also referred to as Timer Gate Enable.

The timer gate can also be driven by multiple selectable sources.

### 26.6.1 TIMER GATE ENABLE

The Timer Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer Gate Enable signal is enabled, the timer will increment on the rising edge of the Timer1 clock source. When Timer Gate Enable signal is disabled, the timer always increments, regardless of the GE bit. See Figure 26-3 for timing details.

**TABLE 26-2: TIMER GATE ENABLE SELECTIONS**

T1CLK	T1GPOL	T1G	Timer Operation
↑	1	1	Counts
↑	1	0	Holds Count
↑	0	1	Holds Count
↑	0	0	Counts

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## 26.12 Register Definitions: Timer1 Control

**REGISTER 26-1: T1CON: TIMER1 CONTROL REGISTER**

U-0	U-0	R/W-0/u	R/W-0/u	U-0	R/W-0/u	R/W-0/u	R/W-0/u
—	—	CKPS<1:0>		—	SYN $\bar{C}$	RD16	ON
bit 7				bit 0			

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6      **Unimplemented:** Read as '0'

bit 5-4      **CKPS<1:0>:** Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3      **Unimplemented:** Read as '0'

bit 2      **SYNC:** Timer1 Synchronization Control bit

When TMR1CLK = Fosc or Fosc/4

This bit is ignored. The timer uses the internal clock and no additional synchronization is performed.

ELSE

0 = Synchronize external clock input with system clock

1 = Do not synchronize external clock input

bit 1      **RD16:** 16-bit Read/Write Mode Enable bit

0 = Enables register read/write of Timer1 in two 8-bit operation

1 = Enables register read/write of Timer1 in one 16-bit operation

bit 0      **ON:** Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1 and clears Timer1 gate flip-flop

## 31.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces half-bridge, full-bridge, and steering of PWM waveforms. It is backwards compatible with previous ECCP functions.

The CWG has the following features:

- Six Operating modes:
  - Synchronous Steering mode
  - Asynchronous Steering mode
  - Full-Bridge mode, Forward
  - Full-Bridge mode, Reverse
  - Half-Bridge mode
  - Push-Pull mode
- Output Polarity Control
- Output Steering:
  - Synchronized to rising event
  - Immediate effect
- Independent 6-Bit Rising and Falling Event Dead-Band Timers:
  - Clocked dead band
  - Independent rising and falling dead-band enables
- Auto-Shutdown Control with:
  - Selectable shutdown sources
  - Auto-restart enable
  - Auto-shutdown pin override control

The CWG modules available are shown in Table 31-1.

**TABLE 31-1: AVAILABLE CWG MODULES**

Device	CWG1
PIC16(L)F19155/56/75/76/85/86	•

## 31.1 Fundamental Operation

The CWG module can operate in six different modes, as specified by MODE of the CWG1CON0 register:

- Half-Bridge mode (Figure 31-9)
- Push-Pull mode (Figure 31-2)
  - Full-Bridge mode, Forward (Figure 31-3)
  - Full-Bridge mode, Reverse (Figure 31-3)
- Steering mode (Figure 31-10)
- Synchronous Steering mode (Figure 31-11)

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. Thus, all output modes support auto-shutdown, which is covered in **Section 31.10 “Auto-Shutdown”**.

### 31.1.1 HALF-BRIDGE MODE

In Half-Bridge mode, two output signals are generated as true and inverted versions of the input as illustrated in Figure 31-9. A non-overlap (dead-band) time is inserted between the two outputs as described in **Section 31.5 “Dead-Band Control”**.

The unused outputs CWG1C and CWG1D drive similar signals, with polarity independently controlled by the POLC and POLD bits of the CWG1CON1 register, respectively.

## 31.3 Selectable Input Sources

The CWG generates the output waveforms from the input sources (See Register 31-9).

The input sources are selected using the CWG1ISM register.

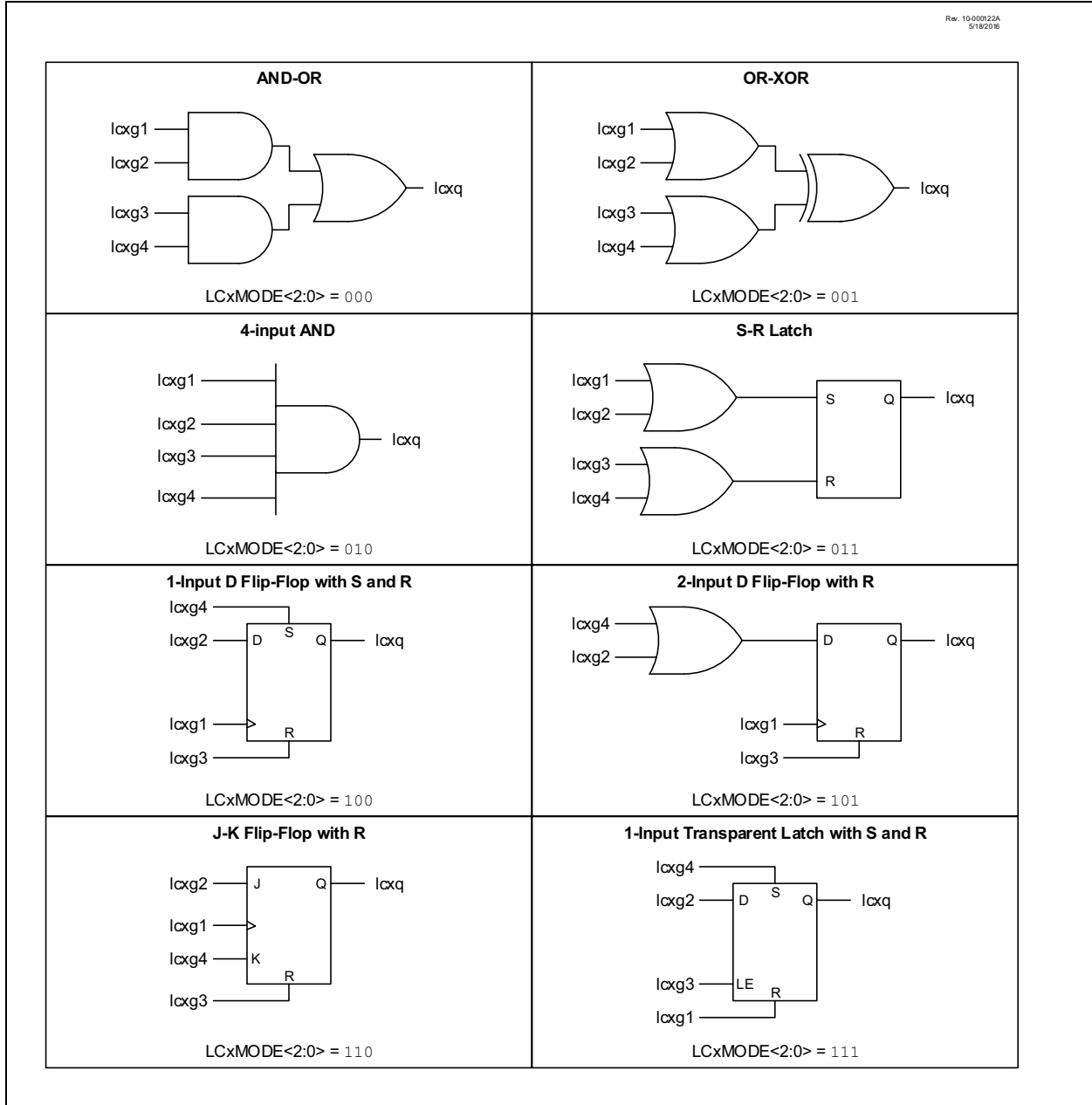
## 31.4 Output Control

### 31.4.1 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the POLx bits of the CWG1CON1. Auto-shutdown and steering options are unaffected by polarity.

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**FIGURE 32-3: PROGRAMMABLE LOGIC FUNCTIONS**





## 34.1.1.5 TSR Status

The TRMT bit of the TXxSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXxREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

**Note:** The TSR register is not mapped in data memory, so it is not available to the user.

## 34.1.1.6 Transmitting 9-Bit Characters

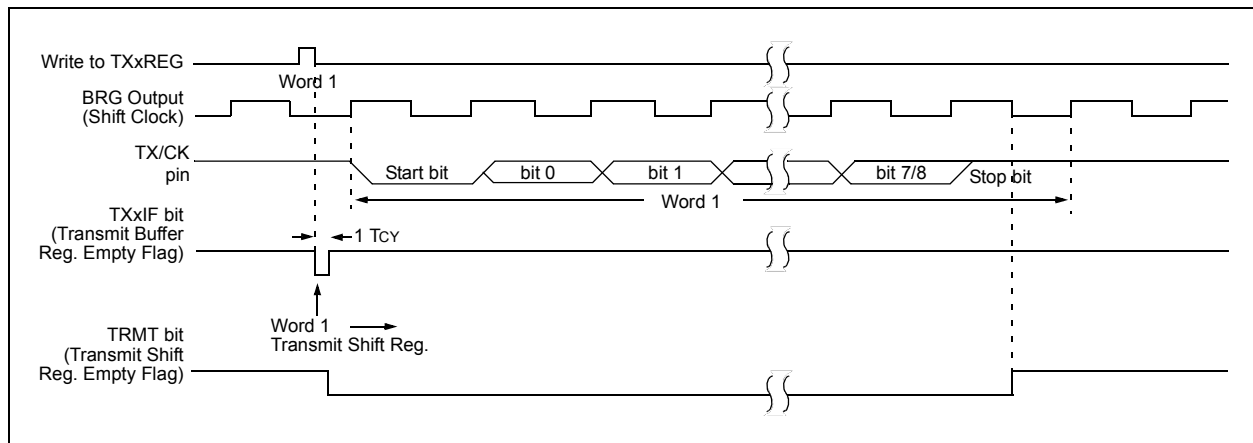
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXxSTA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXxSTA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXxREG. All nine bits of data will be transferred to the TSR register immediately after the TXxREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 34.1.2.7 “Address Detection”** for more information on the Address mode.

## 34.1.1.7 Asynchronous Transmission Set-up:

1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 34.3 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXxIF interrupt bit to be set.
6. If interrupts are desired, set the TXxIE interrupt enable bit of the PIE3 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXxREG register. This will start the transmission.

**FIGURE 34-3: ASYNCHRONOUS TRANSMISSION**





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**TABLE 34-4: BAUD RATE FOR ASYNCHRONOUS MODES (CONTINUED)**

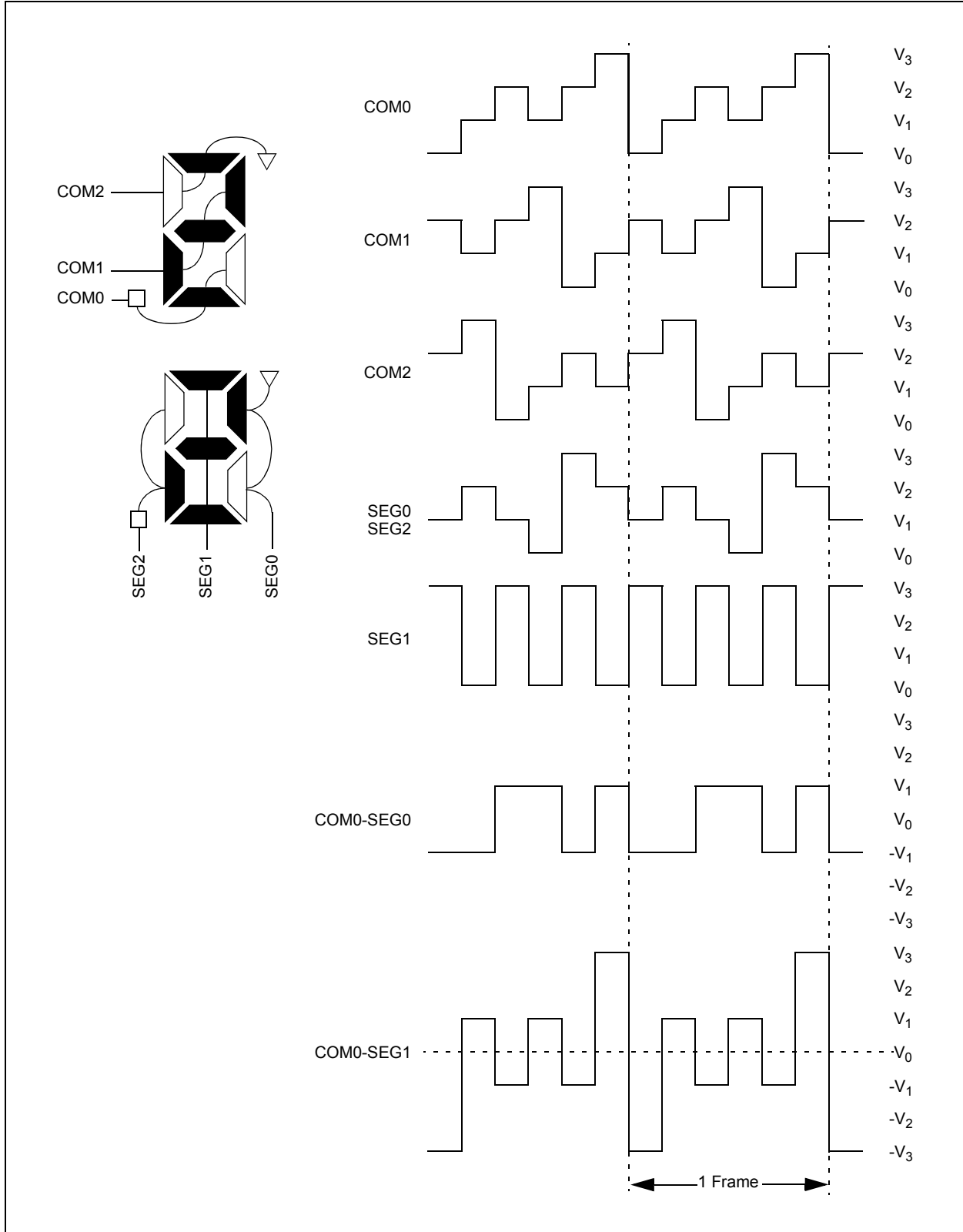
BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	—	—	—
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—
115.2k	—	—	—	—	—	—	115.2k	0.00	1	—	—	—

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

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FIGURE 35-15: TYPE-A WAVEFORMS IN 1/3 MUX, 1/3 BIAS DRIVE



## 35.13 LCD Interrupts

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame, which produces a visually crisp transition of the image.

This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver can be synchronized for segment data updates to the LCD frame.

A new frame is defined as beginning at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a fixed interval before the frame boundary (TFINT), as shown in Figure 35-20.

The LCD controller will begin to access the next frame between the interrupt and when the controller accesses the data (TFWR). New data must be written within TFWR, as this is when the LCD controller will begin to access the data for the next frame.

When the LCD driver is running with Type-B waveforms, and the LMUX<3:0> bits are not equal to '0001', the following issues may arise.

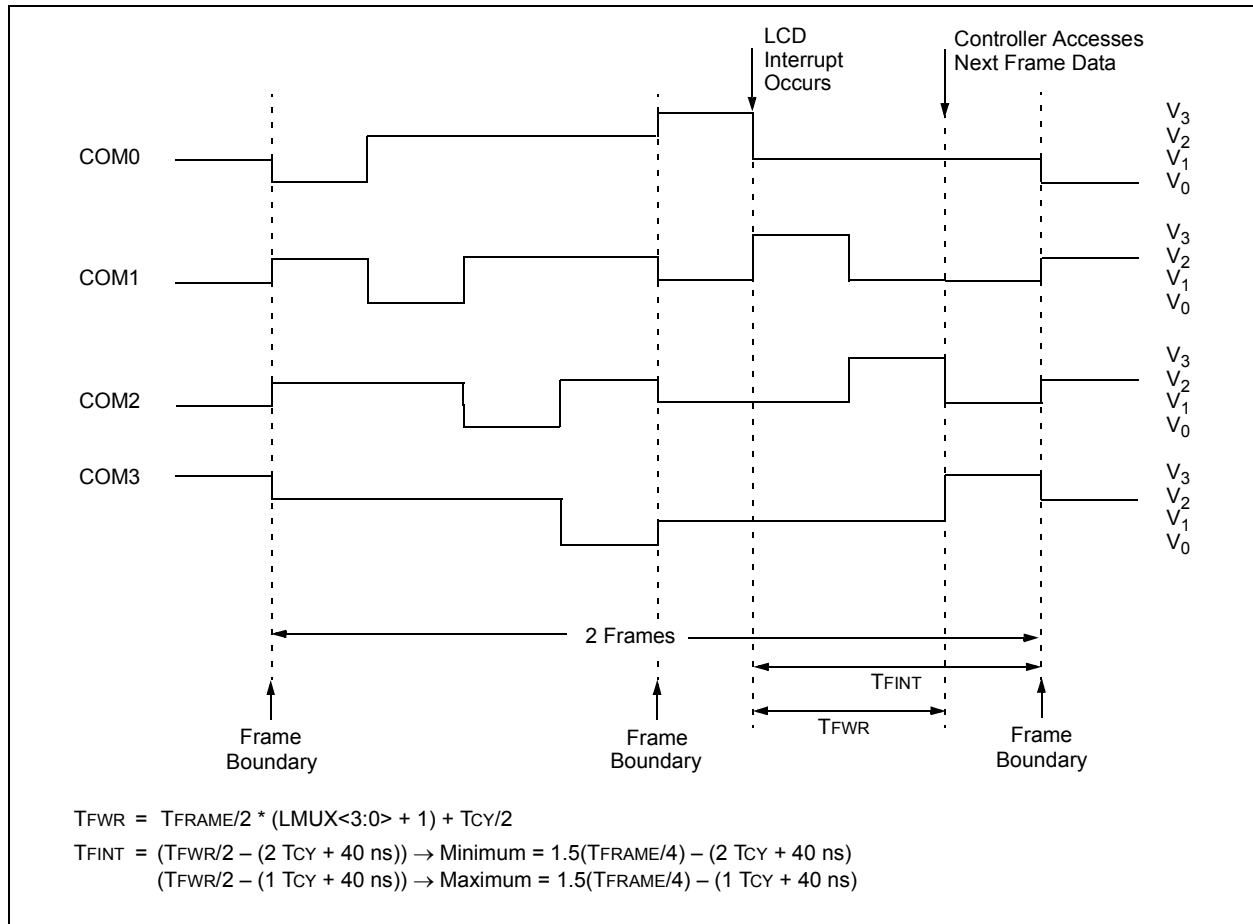
Since the DC voltage on the pixel takes two frames to maintain 0V, the pixel data must not change between subsequent frames. If the pixel data were allowed to change, the waveform for the odd frames would not necessarily be the complement of the waveform generated in the even frames and a DC component would be introduced into the panel.

Because of this, using Type-B waveforms requires synchronizing the LCD pixel updates to occur within a sub-frame after the frame interrupt.

To correctly sequence writing in Type-B, the interrupt only occurs on complete phase intervals. If the user attempts to write when the write is disabled, the WERR bit (LCDCON<5>) is set.

**Note:** The interrupt is not generated when the Type-A waveform is selected and when the Type-B with no multiplex (static) is selected.

**FIGURE 35-20: EXAMPLE WAVEFORMS AND INTERRUPT TIMING IN QUARTER DUTY CYCLE DRIVE**



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## 35.14 Operation During Sleep

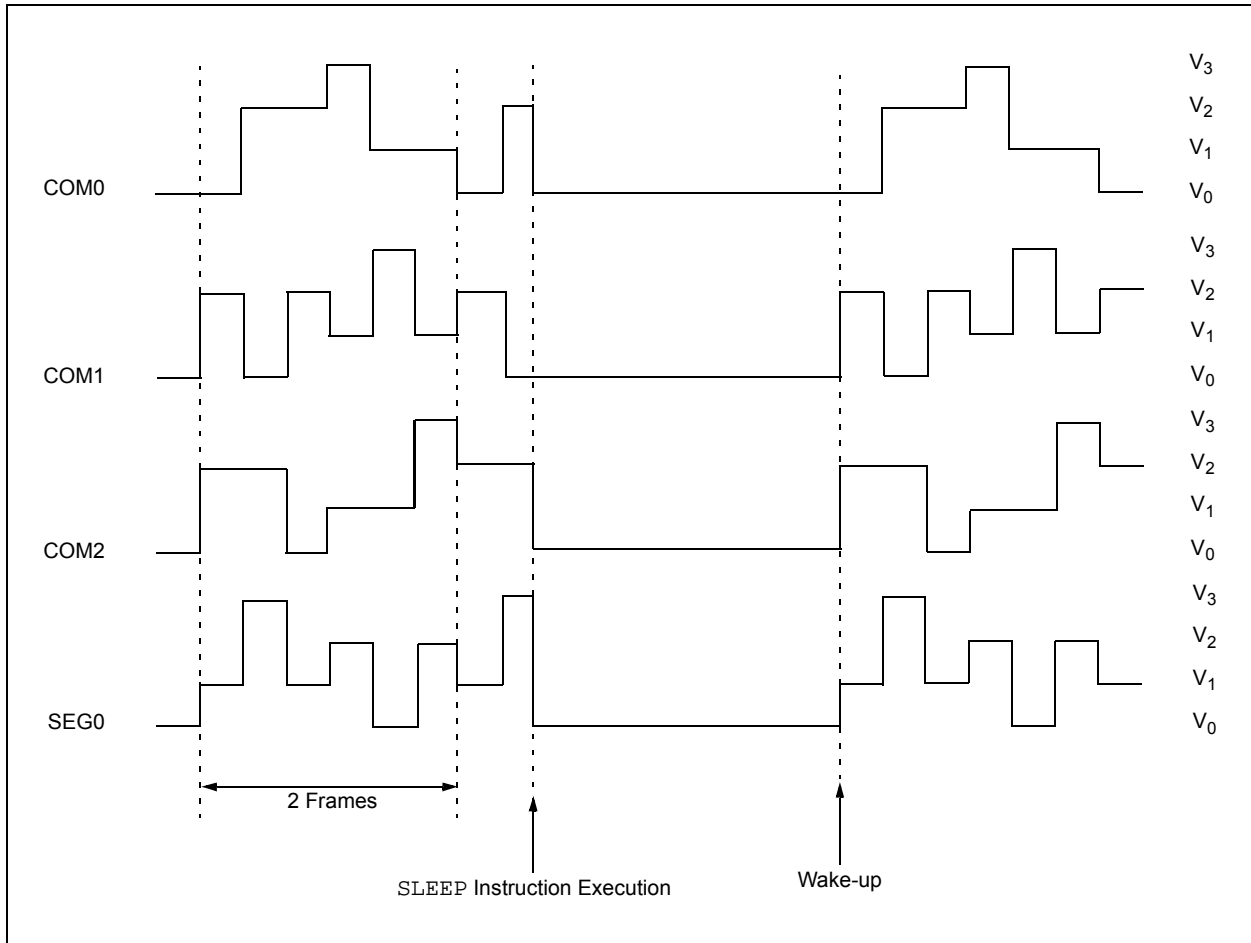
The LCD module can operate during Sleep. The selection is controlled by the SLPEN bit (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very low-current consumption mode. The module will stop operation immediately and drive 0 voltage on both segment and common lines. Figure 35-21 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. The LCD data cannot be changed.

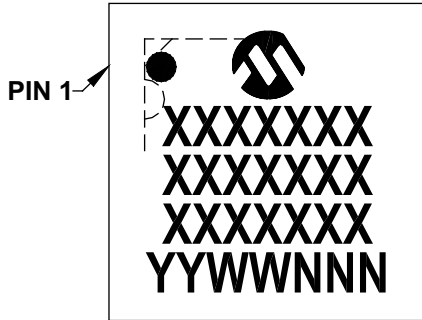
**FIGURE 35-21: SLEEP ENTRY/EXIT WHEN SLPEN = 1 OR CS<1:0> = 00**



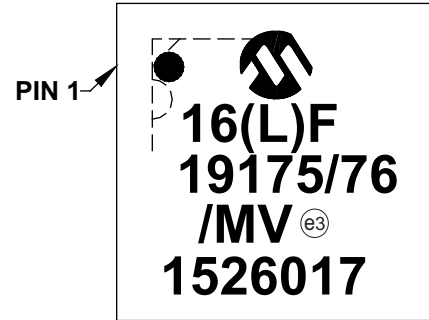
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## 42.1 Package Marking Information (Continued)

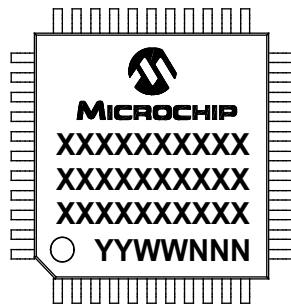
40-Lead UQFN (5x5x0.5 mm)



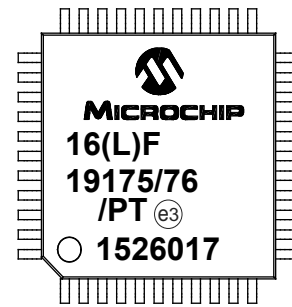
Example



44-Lead TQFP (10x10x1 mm)



Example



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	