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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19185-e-pt

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F19155/56) (CONTINUED)

I/O(2)	28-Pin SPDIP/SSOP/SOIC	28-Pin UQFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	SEG14	IOCB6	—	Y	ICDCLK/ ICSPCLK
RB7	28	25	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	SEG15	IOCB7	—	Y	ICDDAT/ ICSPDAT
RC0	11	8	—	—	—	—	—	T1CKI(1) SMTWIN1(1)	—	—	—	—	—	—	—	—	IOCC0	—	Y	SOSCO
RC1	12	9	—	—	—	—	—	SMTSIG1(1) T4IN(1)	CCP2(1)	—	—	—	—	—	—	—	IOCC1	—	Y	SOSCI
RC2	13	10	ANC2	—	—	—	—	—	CCP1(1)	—	—	—	—	—	—	COM2 SEG18	IOCC2	—	Y	—
RC3	14	11	ANC3	—	—	—	—	T2IN(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	SEG19	IOCC3	—	Y	—
RC4	15	12	ANC4	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	—	—	SEG20	IOCC4	—	Y	—
RC6	17	14	ANC6	—	—	—	—	—	—	—	—	—	TX1(1) CK1(1)	—	—	COM5 SEG22 VLCD2	IOCC6	—	Y	—
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1)	—	—	SEG23 COM4 VLCD1	IOCC7	—	Y	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	—	Y	$\overline{MCLR}$
VLCD3	16	13	—	—	—	—	—	—	—	—	—	—	—	—	—	VLCD3	—	—	—	—
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8 19	5 16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 10											
CPU CORE REGISTERS; see Table 4-3 for specifics											
50Ch	—	Unimplemented								---- ----	---- ----
50Dh	—	Unimplemented								---- ----	---- ----
50Eh	—	Unimplemented								---- ----	---- ----
50Fh	—	Unimplemented								---- ----	---- ----
510h	—	Unimplemented								---- ----	---- ----
511h	—	Unimplemented								---- ----	---- ----
512h	—	Unimplemented								---- ----	---- ----
513h	—	Unimplemented								---- ----	---- ----
514h	—	Unimplemented								---- ----	---- ----
515h	—	Unimplemented								---- ----	---- ----
516h	—	Unimplemented								---- ----	---- ----
517h	—	Unimplemented								---- ----	---- ----
518h	—	Unimplemented								---- ----	---- ----
519h	—	Unimplemented								---- ----	---- ----
51Ah	—	Unimplemented								---- ----	---- ----
51Bh	—	Unimplemented								---- ----	---- ----
51Ch	—	Unimplemented								---- ----	---- ----
51Dh	—	Unimplemented								---- ----	---- ----
51Eh	—	Unimplemented								---- ----	---- ----
51Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

7.0 DEVICE CONFIGURATION INFORMATION

The Device Configuration Information (DCI) is a dedicated region in the Program Flash Memory mapped from 8200h to 821Fh. The data stored in the DCI memory is hard-coded into the device during manufacturing.

Refer to Table 7-1 for the complete DCI table address and description. The DCI holds information about the device which is useful for programming and bootloader applications. These locations are read-only and cannot be erased or modified.

TABLE 7-1: DEVICE CONFIGURATION INFORMATION FOR PIC16(L)F19155/56/75/76/85/86 FAMILY OF DEVICES

ADDRESS	Name	DESCRIPTION	VALUE	UNITS
8200h	ERSIZ	Erase Row Size	32	Words
8201h	WLSIZ	Number of write latches	32	
8202h	URSIZ	Number of User Rows	See Table 7-2	Rows
8203h	EESIZ	EE Data memory size	256	Bytes
8204h	PCNT	Pin Count	28/40/44/48	Pins

TABLE 7-2: MEMORY SIZE AND NUMBER OF USER ROWS

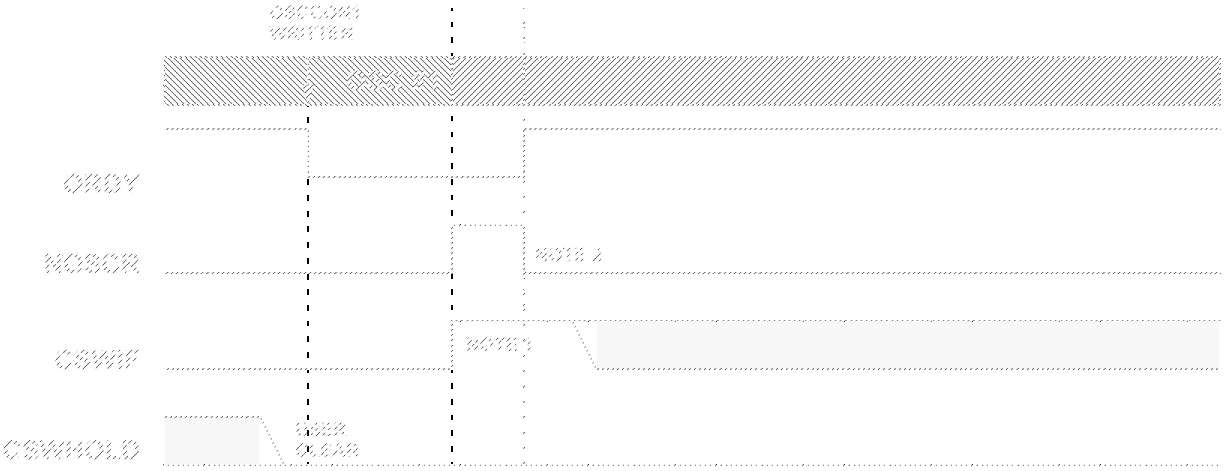
Part Name	Memory size	Number of User rows
PIC16(L)F19155	8k	256
PIC16(L)F19175	8k	256
PIC16(L)F19185	8k	256
PIC16(L)F19156	16k	512
PIC16(L)F19176	16k	512
PIC16(L)F19186	16k	512

7.1 DIA and DCI Access

The DIA and DCI addresses are read-only and cannot be erased or modified. See **Section 13.4.7 “NVMREG Access to Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Words”** for more information on accessing these memory locations.

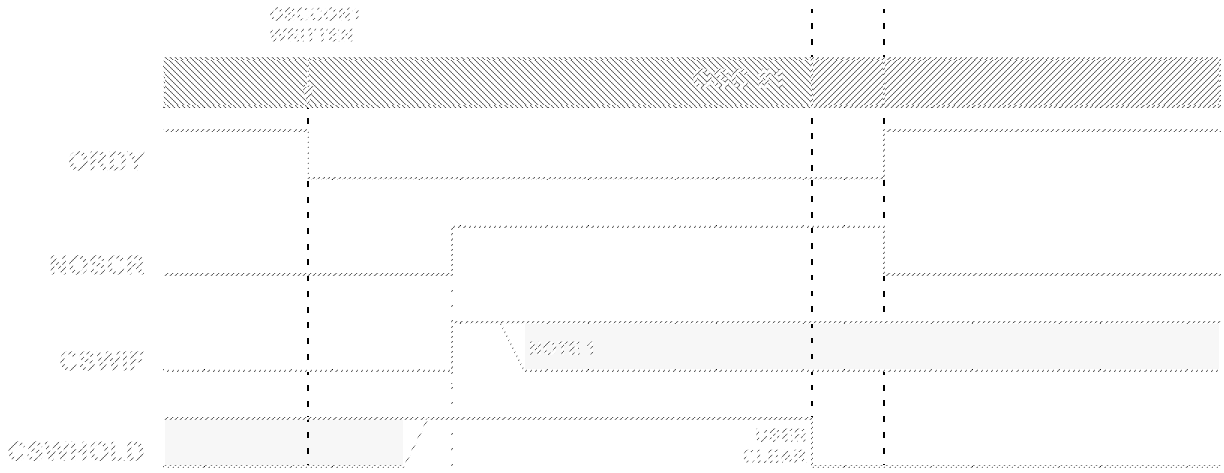
Development tools, such as device programmers and debuggers, may be used to read the DIA and DCI regions, similar to the Device ID and Revision ID.

FIGURE 9-4: CLOCK SWITCH (CSWHOLD = 0)



Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 9-5: CLOCK SWITCH (CSWHOLD = 1)



Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON1	—	NOSC<2:0>			NDIV<3:0>				152
OSCCON2	—	COSC<2:0>			CDIV<3:0>				152
OSCCON3	CWSHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	154
OSCFRQ	—	—	—	—	—	HFFRQ<2:0>			157
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	155
OSCTUNE	—	—	HFTUN<5:0>						157
OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	156
ACTCON	ACTEN	ACTUD	—	—	ACTLOCK	—	ACTORS		158

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	—	CSWEN	LCDPEN	$\overline{\text{VBATEN}}$	$\overline{\text{CLKOUTEN}}$	120
	7:0	—	RSTOSC<2:0>			—	FEXTOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

REGISTER 10-13: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	R/W/HS-0/0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	ZCDIF	—	—	—	—	C2IF	C1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **Unimplemented**: Read as '0'

bit 6 **ZCDIF:** Zero-Cross Detect (ZCD1) Interrupt Flag bit
1 = An enabled rising and/or falling ZCD1 event has been detected (must be cleared in software)
0 = No ZCD1 event has occurred

bit 5-2 **Unimplemented**: Read as '0'

bit 1 **C2IF**: Comparator C2 Interrupt Flag bit
1 = Comparator 2 interrupt asserted (must be cleared in software)
0 = Comparator 2 interrupt not asserted

bit 0 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Comparator 1 interrupt asserted (must be cleared in software)
0 = Comparator 1 interrupt not asserted

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

13.2 Data EEPROM Memory

Data EEPROM Memory consists of 256 bytes of user data memory. The EEPROM provides storage locations for 8-bit user defined data. EEPROM can be read and/or written through:

- FSR/INDF indirect access (**Section 13.3 "FSR and INDF Access"**)
- NVMREG access (**Section 13.4 "NVMREG Access"**)
- In-Circuit Serial Programming™ (ICSP™)

Unlike PFM, which must be written to by row, EEPROM can be written to word by word.

13.3 FSR and INDF Access

The FSR and INDF registers allow indirect access to the PFM.

13.3.1 FSR READ

With the intended address loaded into an FSR register a `MOVIW` instruction or read of INDF will read data from the PFM.

Reading from NVM requires one instruction cycle. The CPU operation is suspended during the read, and resumes immediately after. Read operations return a single byte of memory.

13.3.2 FSR WRITE

Writing/erasing the NVM through the FSR registers (ex. `MOVWI` instruction) is not supported in the PIC16(L)F19155/56/75/76/85/86 devices.

13.4 NVMREG Access

The NVMREG interface allows read/write access to all the locations accessible by FSRs, and also read/write access to the User ID locations, and read-only access to the device identification, revision, and Configuration data.

Writing, or erasing of NVM via the NVMREG interface is prevented when the device is write-protected.

13.4.1 NVMREG READ OPERATION

To read a NVM location using the NVMREG interface, the user must:

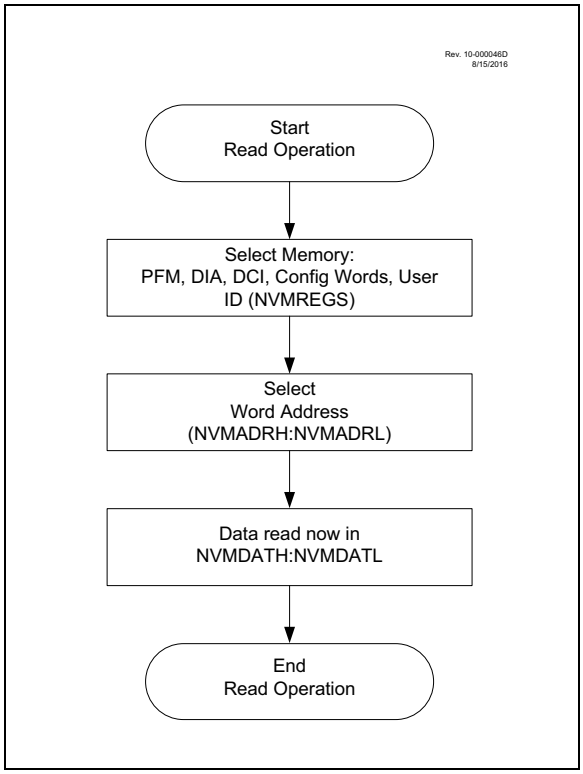
1. Clear the NVMREGS bit of the NVMCON1 register if the user intends to access PFM locations, or set NMVREGS if the user intends to access User ID, or Configuration locations.
2. Write the desired address into the NVMADRH:NVMADRL register pair (Table 13-2).
3. Set the RD bit of the NVMCON1 register to initiate the read.

Once the read control bit is set, the CPU operation is suspended during the read, and resumes immediately after. The data is available in the very next cycle, in the NVMDATH:NVMDATL register pair; therefore, it can be read as two bytes in the following instructions.

NVMDATH:NVMDATL register pair will hold this value until another read or until it is written to by the user.

Upon completion, the RD bit is cleared by hardware.

FIGURE 13-1: FLASH PROGRAM MEMORY READ FLOWCHART



21.6 Register Definitions: DAC Control

REGISTER 21-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **DAC1EN:** DAC1 Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **DAC1OE1:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT1 pin
0 = DAC voltage level is disconnected from the DAC1OUT1 pin

bit 4 **DAC1OE2:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT2 pin
0 = DAC voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 **DAC1PSS<1:0>:** DAC1 Positive Source Select bits
11 = Reserved, do not use
10 = FVR output
01 = V_{REF+} pin
00 = V_{DD}

bit 1-0 **Unimplemented:** Read as ‘0’

REGISTER 21-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	DAC1R<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DAC1R<4:0>:** DAC1 Voltage Output Select bits
$V_{OUT} = (V_{SRC+} - V_{SRC-})*(DAC1R<4:0>/32) + V_{SRC}$

REGISTER 24-5: WEEKDAY(1): WEEKDAY VALUE REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal value of weekdays '1' digit; valid values from 0 to 6

Note 1: Writes to the WDAY registers are only allowed when RTCWREN = 1.

REGISTER 24-6: DAY(1): DAY VALUE REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYH<1:0>		DAYL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYH<1:0>:** Binary Coded Decimal value of days '10' digit; valid values from 0 to 3

bit 3-0 **DAYL<3:0>:** Binary Coded Decimal value of days '1' digit; valid values from 0 to 9

Note 1: Writes to the DAY registers are only allowed when RTCWREN = 1.

REGISTER 24-7: HOURS(1): HOUR VALUE REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRH<1:0>		HRL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRH<1:0>:** Binary Coded Decimal value of hours '10' digit; valid values from 0 to 2

bit 3-0 **HRL<3:0>:** Binary Coded Decimal value of hours '1' digit; valid values from 0 to 9

Note 1: Writes to the HOURS registers are only allowed when RTCWREN = 1.

27.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the TxCON register are cleared).
- The diagrams illustrate any clock except Fosc/4 and show clock-sync delays of at least two full cycles for both ON and Timer2/4_ers. When using Fosc/4, the clock-sync delay is at least one instruction period for Timer2/4_ers; ON applies in the next instruction period.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 29.0 "Capture/Compare/PWM Modules"**. The signals are not a part of the Timer2/4 module.

27.5.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2/4 operation. The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the TMRx count equals the PRx period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 27-4. With PRx = 5, the counter advances until TMRx = 5, and goes to zero with the next clock.

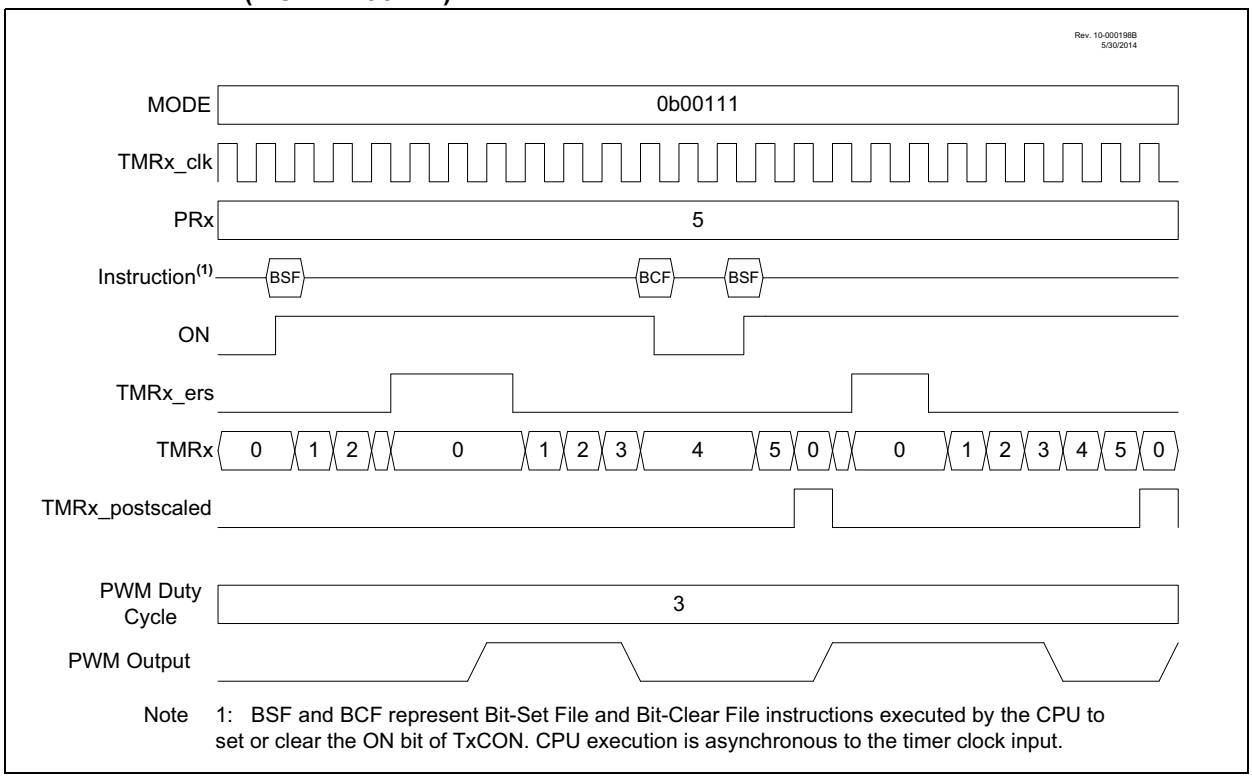
27.5.4 LEVEL-TRIGGERED HARDWARE LIMIT MODE

In the Level-Triggered Hardware Limit Timer modes the counter is reset by high or low levels of the external signal TMRx_ers, as shown in Figure 27-7. Selecting MODE<4:0> = 00110 will cause the timer to reset on a low level external signal. Selecting MODE<4:0> = 00111 will cause the timer to reset on a high level external signal. In the example, the counter is reset while TMRx_ers = 1. ON is controlled by BSF and BCF instructions. When ON = 0 the external signal is ignored.

When the CCP uses the timer as the PWM time base then the PWM output will be set high when the timer starts counting and then set low only when the timer count matches the CCPRx value. The timer is reset when either the timer count matches the PRx value or two clock periods after the external Reset signal goes true and stays true.

The timer starts counting, and the PWM output is set high, on either the clock following the PRx match or two clocks after the external Reset signal relinquishes the Reset. The PWM output will remain high until the timer counts up to match the CCPRx pulse width value. If the external Reset signal goes true while the PWM output is high then the PWM output will remain high until the Reset signal is released allowing the timer to count up to match the CCPRx value.

FIGURE 27-7: LEVEL-TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE = 00111)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

FIGURE 28-8: HIGH AND LOW-MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM

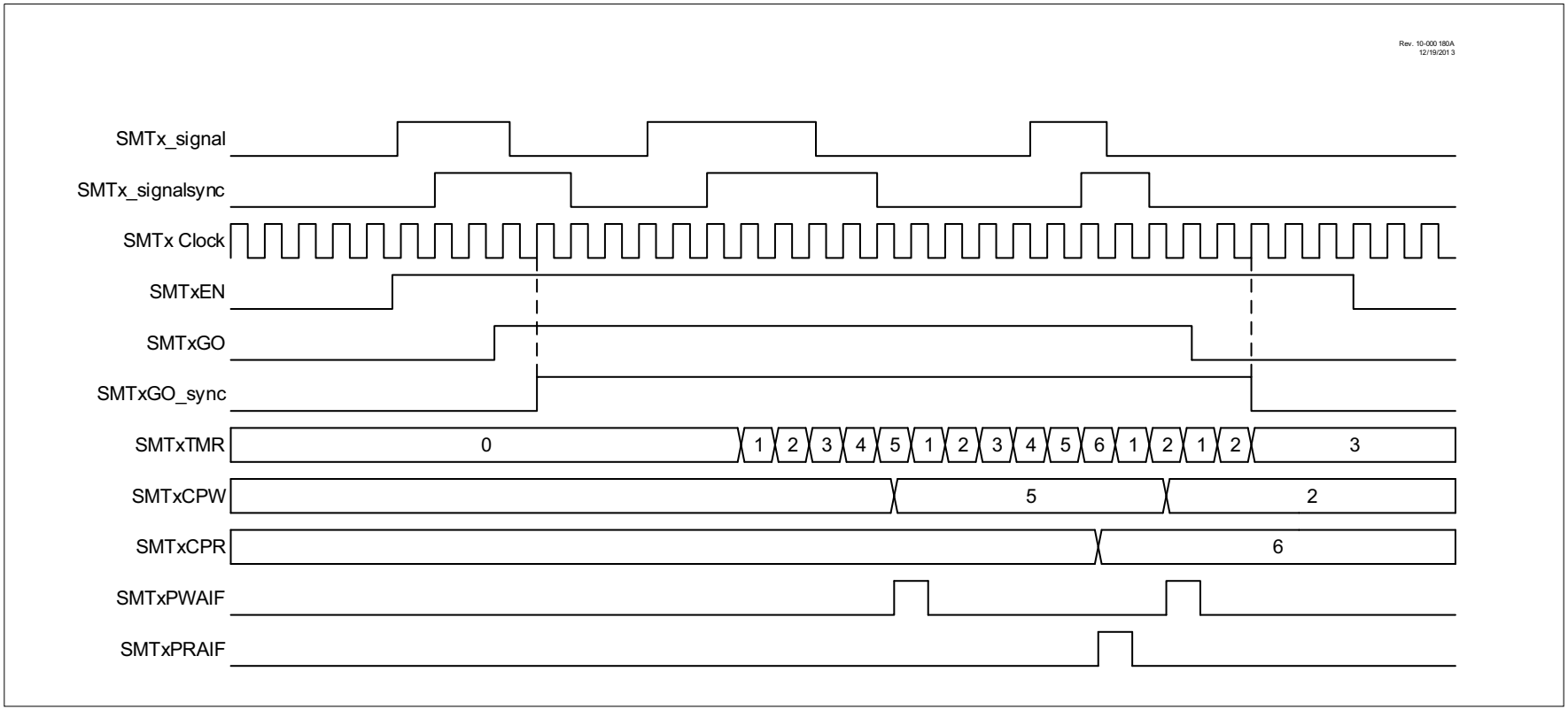


FIGURE 33-20: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

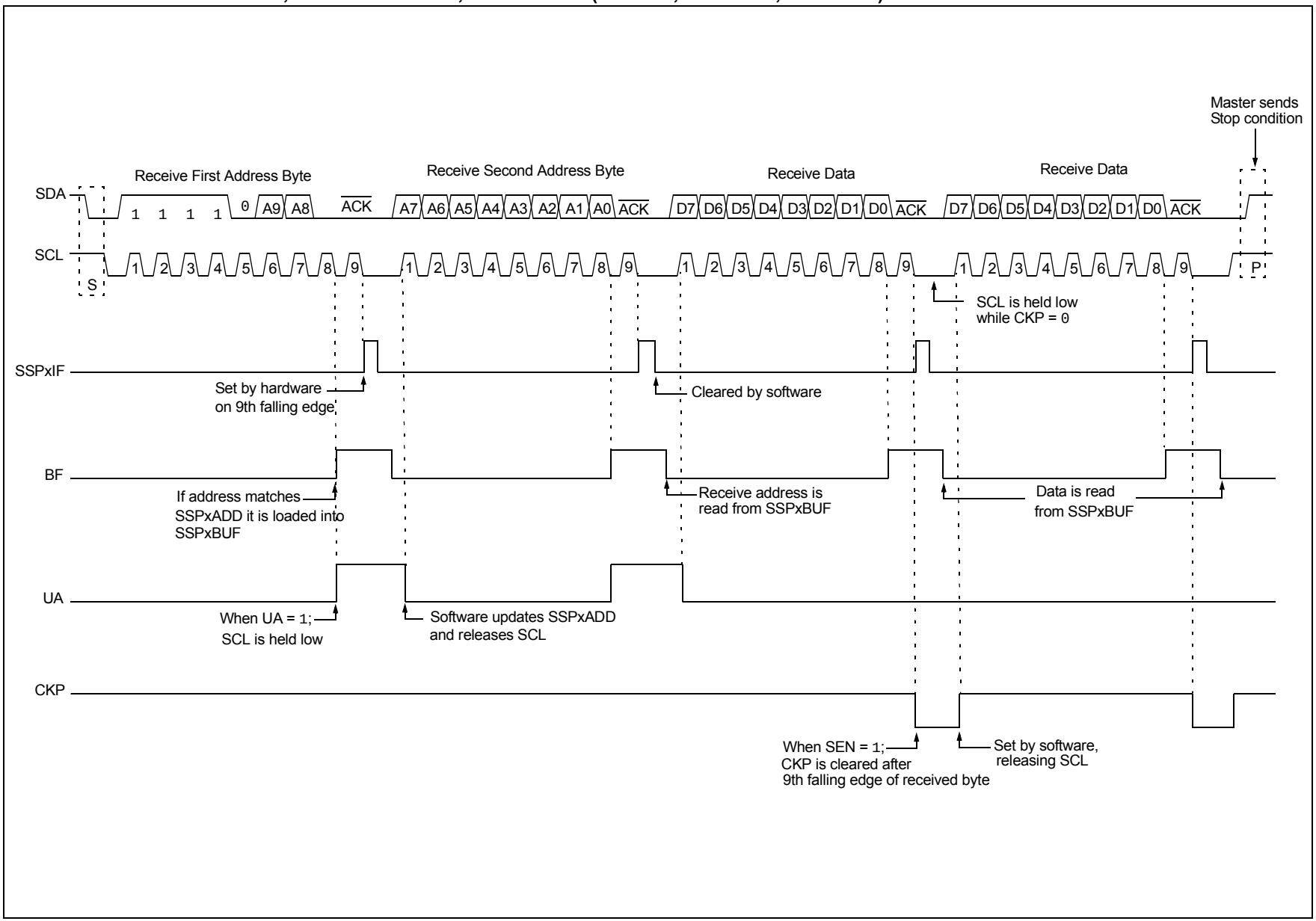


FIGURE 33-34: BUS COLLISION DURING START CONDITION (SCL = 0)

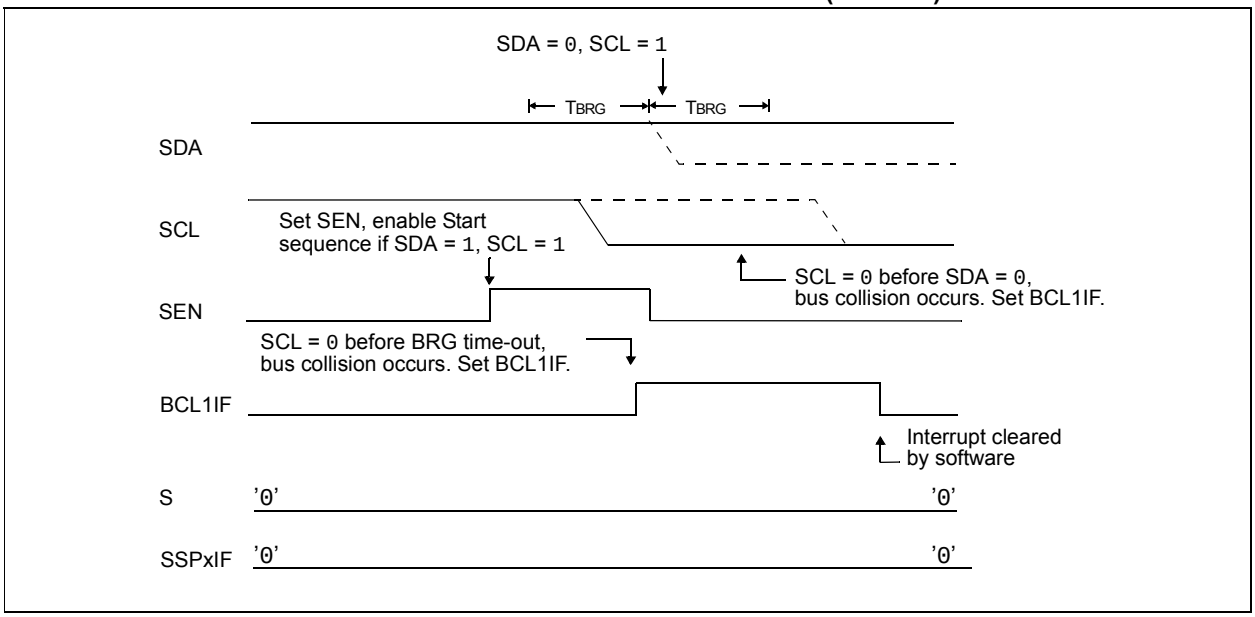
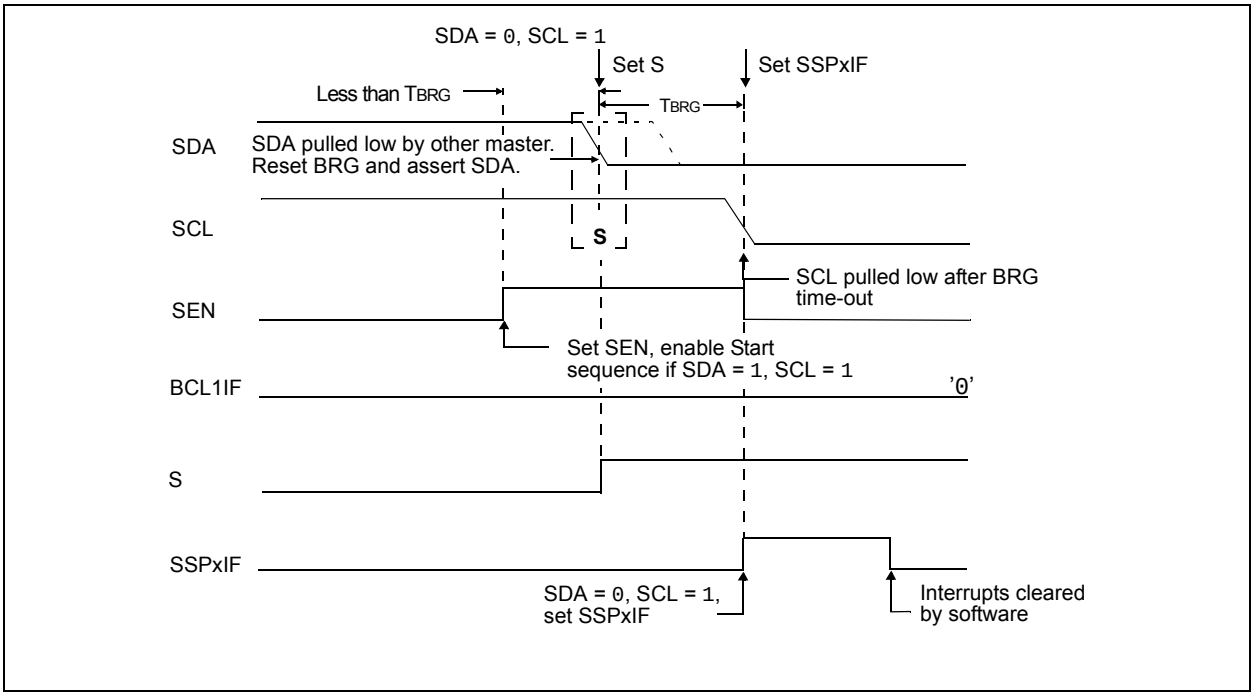


FIGURE 33-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



34.4.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note:	If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

34.4.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCxREG is read to access the FIFO. When this happens the OERR bit of the RCxSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCxREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

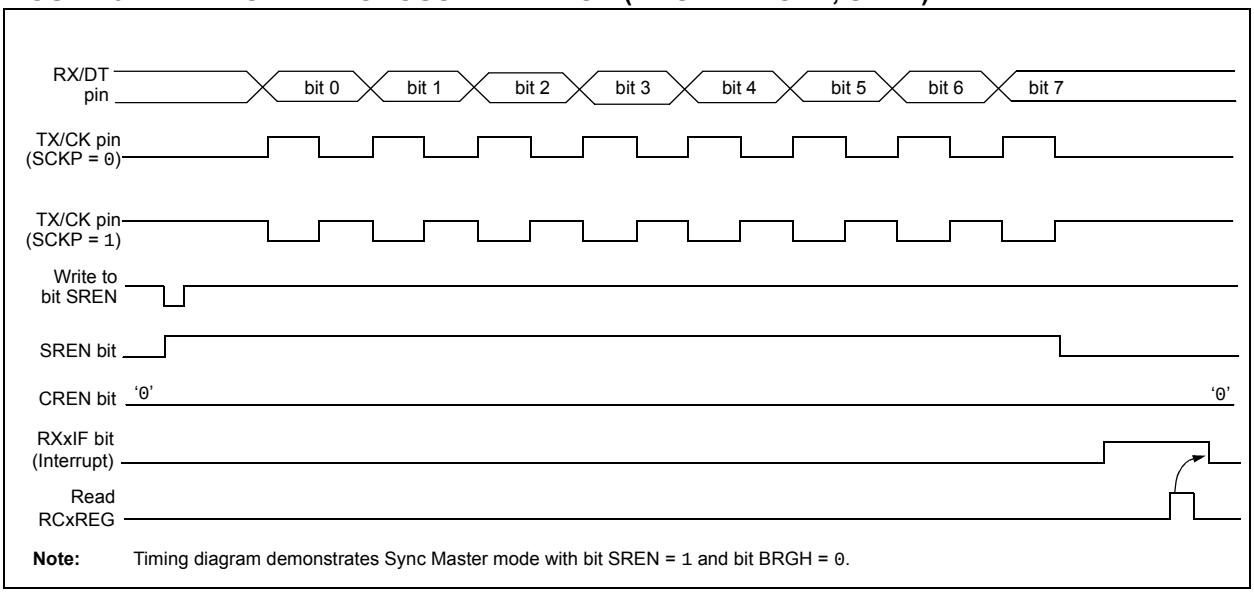
34.4.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

34.4.1.9 Synchronous Master Reception Set-up:

1. Initialize the SPxBRGH, SPxBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RXxIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RXxIE was set.
9. Read the RCxSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCxREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

FIGURE 34-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

35.8 LCD Multiplex Types

The LCD driver module can be configured into four multiplex types:

- Static (only COM0 used)
- 1/2 multiplex (COM0 and COM1 are used)
- 1/3 multiplex (COM0, COM1 and COM2 are used)
- 1/4 multiplex (COM0, COM1, COM2 and COM3 are used)
- 1/5 multiplex (COM0, COM1, COM2, COM3 and COM4 are used)
- 1/6 multiplex (COM0, COM1, COM2, COM3, COM4 and COM5 are used)
- 1/7 multiplex (COM0, COM1, COM2, COM3, COM4, COM5 and COM6 are used)
- 1/8 multiplex (COM0, COM1, COM2, COM3, COM4, COM5, COM6 and COM7 are used)

The LMUX<3:0> setting (LCDCON<3:0>) decides the function of the COM pins. (For details, see Table 35-8).

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

Note: On a Power-on Reset, the LMUX<3:0> bits are '0000'.

TABLE 35-8: COM<7:0> PIN FUNCTIONS

LMUX<3:0>	COM7 Pin	COM6 Pin	COM5 Pin	COM4 Pin	COM3 Pin	COM2 Pin	COM1 Pin	COM0 Pin
1000	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
0111	I/O Pin	COM6	COM5	COM4	COM3	COM2	COM1	COM0
0110	I/O Pin	I/O Pin	COM5	COM4	COM3	COM2	COM1	COM0
0101	I/O Pin	I/O Pin	I/O Pin	COM4	COM3	COM2	COM1	COM0
0100	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM3	COM2	COM1	COM0
0011	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM2	COM1	COM0
0010	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM1	COM0
0001	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM0
0000	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin

TABLE 35-10: SUMMARY OF REGISTERS ASSOCIATED WITH LCD MODULE (CONTINUED)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
LCDDATA34	S47C5	S46C5	S45C5	S44C5	S43C5	S42C5	S41C5	S40C5	624
LCDDATA35	S07C6	S06C6	—	S04C6	S03C6	S02C6	S01C6	S00C6	624
LCDDATA36	S15C6	S14C6	S13C6	—	S11C6	S10C6	S09C6	S08C6	624
LCDDATA37	S23C6	S22C6	—	S20C6	S19C6	S18C6	—	—	624
LCDDATA38	S31C6	S30C6	S29C6	S28C6	S27C6	S26C6	S25C6	S24C6	624
LCDDATA39	—	—	—	—	—	S34C6	S33C6	S32C6	624
LCDDATA40	S47C6	S46C6	S45C6	S44C6	S43C6	S42C6	S41C6	S40C6	624
LCDDATA41	S07C7	S06C7	—	S04C7	S03C7	S02C7	S01C7	S00C7	624
LCDDATA42	S15C7	S14C7	S13C7	—	S11C7	S10C7	S09C7	S08C7	624
LCDDATA43	S23C7	S22C7	—	S20C7	S19C7	S18C7	—	—	624
LCDDATA44	S31C7	S30C7	S29C7	S28C7	S27C7	S26C7	S25C7	S24C7	624
LCDDATA45	—	—	—	—	—	S34C7	S33C7	S32C7	624
LCDDATA46	S47C7	S46C7	S45C7	S44C7	S43C7	S42C7	S41C7	S40C7	624
LCDDATA47	S07C0	S06C0	—	S04COM0	S03C0	S02C0	S01C0	S00C0	624

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1E95h	—	Unimplemented								
1E96h	—	Unimplemented								
1E97h	—	Unimplemented								
1E98h	—	Unimplemented								
1E99h	—	Unimplemented								
1E9Ah	—	Unimplemented								
1E9Bh	—	Unimplemented								
1E9Ch	T2AINPPS	—	—	—	T2INPPS<4:0>					264
1E9Dh	T4AINPPS	—	—	—	T4INPPS<4:0>					264
1E9Eh	—	Unimplemented								
1E9Fh	—	Unimplemented								
1EA0h	—	Unimplemented								
1EA1h	CCP1PPS	—	—	—	CCP1PPS<4:0>					264
1EA2h	CCP2PPS	—	—	—	CCP2PPS<4:0>					264
1EA3h	—	Unimplemented								
1EA4h	—	Unimplemented								
1EA5h	—	Unimplemented								
1EA6h	—	Unimplemented								
1EA7h	—	Unimplemented								
1EA8h	—	Unimplemented								
1EA9h	SMT1WINPPS	—	—	—	SMT1WINPPS<4:0>					264
1EAAh	SMT1SIGPPS	—	—	—	SMT1SIGPPS<4:0>					264
1EABh	—	Unimplemented								
1EACh	—	Unimplemented								
1EADh	—	Unimplemented								
1EAEh	—	Unimplemented								
1EAFh	—	Unimplemented								
1EB0h	—	Unimplemented								
1EB1h	CWG1PPS	—	—	—	CWG1PPS<4:0>					264
1EB2h	—	Unimplemented								
1EB3h	—	Unimplemented								
1EB4h	—	Unimplemented								
1EB5h	—	Unimplemented								
1EB6h	—	Unimplemented								
1EB7h	—	Unimplemented								
1EB8h	—	Unimplemented								
1EB9h	—	Unimplemented								
1EBAh	—	Unimplemented								
1EBBh	CLCIN0PPS	—	—	—	CLCIN0PPS<4:0>					264
1EBCh	CLCIN1PPS	—	—	—	CLCIN1PPS<4:0>					264
1EBDh	CLCIN2PPS	—	—	—	CLCIN2PPS<4:0>					264

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 39-5: MEMORY PROGRAMMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
High Voltage Entry Programming Mode Specifications							
MEM01	V_{IHH}	Voltage on $\overline{MCLR}$/VPP pin to enter programming mode	8	—	9	V	**(Note 2, Note 3)**
MEM02	I_{PPGM}	Current on $\overline{MCLR}$/VPP pin during programming mode	—	1	—	mA	**(Note 2)**
Programming Mode Specifications							
MEM10	V_{BE}	VDD for Bulk Erase	—	2.7	—	V	
MEM11	I_{DDPGM}	Supply Current during Programming operation	—	—	10	mA	
Data EEPROM Memory Specifications							
MEM20	ED	DataEE Byte Endurance	100k			E/W	-40°C ≤ TA ≤ +85°C
MEM21	TD-RET	Characteristic Retention		40		Year	Provided no other specifications are violated
MEM22	ND_REF	Total Erase/Write Cycles before Refresh			100k	E/W	
MEM23	VD_RW	Vdd for Read or Erase/Write operation	VDDMIN		VDDMAX	V	
MEM24	TD_BEW	Byte Erase and Write Cycle Time		4.0	5.0	ms	
Program Flash Memory Specifications							
MEM30	E_P	Flash Memory Cell Endurance	10k	—	—	E/W	-40°C ≤ TA ≤ +85°C (**Note 1**)
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	VDD for Read operation	VDDMIN	—	VDDMAX	V	
MEM34	V_{P_REW}	VDD for Row Erase or Write operation	VDDMIN	—	VDDMAX	V	
MEM35	T_{P_REW}	Self-Timed Row Erase or Self-Timed Write	—	2.0	2.5	ms	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

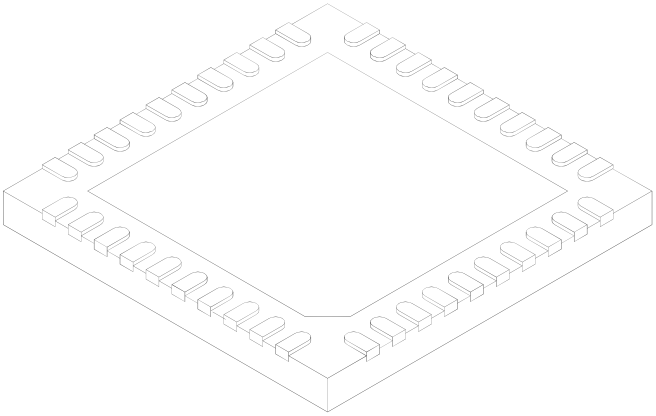
Note 1: Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.

2: Required only if CONFIG4, bit LVP is disabled.

3: The MPLAB® ICD2 does not support variable VPP output. Circuitry to limit the ICD2 VPP voltage must be placed between the ICD2 and target system when programming or debugging with the ICD2.

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2