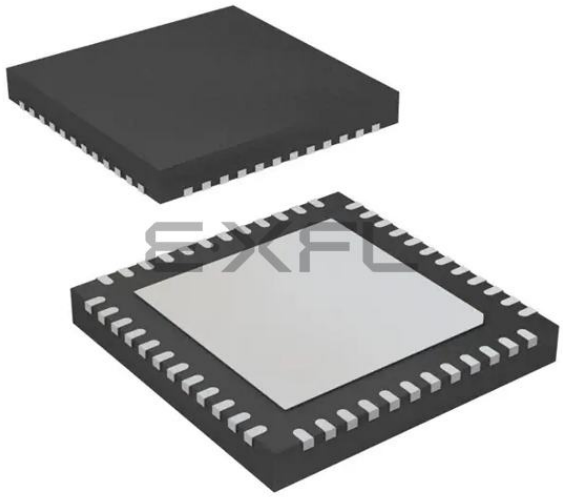

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19185t-i-mv

3.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 10.5 "Automatic Context Saving"** for more information.

3.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 4.5 "Stack"** for more details.

3.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers, program memory, and data EEPROM, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. See **Section 4.6 "Indirect Addressing"** for more details.

3.4 Instruction Set

There are 48 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 37.0 "Instruction Set Summary"** for more details.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 10											
CPU CORE REGISTERS; see Table 4-3 for specifics											
50Ch	—	Unimplemented								---- ----	---- ----
50Dh	—	Unimplemented								---- ----	---- ----
50Eh	—	Unimplemented								---- ----	---- ----
50Fh	—	Unimplemented								---- ----	---- ----
510h	—	Unimplemented								---- ----	---- ----
511h	—	Unimplemented								---- ----	---- ----
512h	—	Unimplemented								---- ----	---- ----
513h	—	Unimplemented								---- ----	---- ----
514h	—	Unimplemented								---- ----	---- ----
515h	—	Unimplemented								---- ----	---- ----
516h	—	Unimplemented								---- ----	---- ----
517h	—	Unimplemented								---- ----	---- ----
518h	—	Unimplemented								---- ----	---- ----
519h	—	Unimplemented								---- ----	---- ----
51Ah	—	Unimplemented								---- ----	---- ----
51Bh	—	Unimplemented								---- ----	---- ----
51Ch	—	Unimplemented								---- ----	---- ----
51Dh	—	Unimplemented								---- ----	---- ----
51Eh	—	Unimplemented								---- ----	---- ----
51Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Banks 30-57											
CPU CORE REGISTERS; see Table 4-3 for specifics											
F0Ch — 1C9Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 8-5: VDD VS. VBAT

VDD	VBAT	Description
>VBOR	>VBOR	• If VDD > VBAT, then all active modules operate on VDD. If VBAT > VDD, then RTCC and SOSC operate on Vbat and all other active modules operate on VDD. • $\overline{\text{VBATBOR}}$ bit in PCON1 unchanged • $\overline{\text{BOR}}$ bit in PCON0 unchanged
>VBOR	<VBOR	• All active modules operate on VDD • $\overline{\text{VBATBOR}}$ bit in PCON1 unchanged • $\overline{\text{BOR}}$ bit in PCON0 unchanged
<VBOR	>VBOR	• The RTCC, SOSC operate on VBAT • All other modules are held in Reset • $\overline{\text{VBATBOR}}$ bit in PCON1 unchanged • Clear $\overline{\text{BOR}}$ bit in PCON0 to indicate VDDBOR
<VBOR	<VBOR	• All modules are held in Reset. • The $\overline{\text{VBATBOR}}$ bit in PCON1 cleared to indicate $\overline{\text{VBATBOR}}$ • The $\overline{\text{BOR}}$ bit in PCON0 cleared to indicate VDDBOR

TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	—	—	—	—	—	—	BORRDY	135
PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	140
PCON1	—	—	—	—	—	—	$\overline{\text{MEMV}}$	$\overline{\text{VBATBOR}}$	141
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	50
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	196
VB0GPR	VB0GPR								
VB1GPR	VB1GPR								
VP2GPR	VP2GPR								
VP3GPR	VP3GPR								

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

EXAMPLE 13-5: DEVICE ID ACCESS

```
; This write routine assumes the following:
; 1. A full row of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
; stored in little endian format
; 3. A valid starting address (the least significant bits = 00000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
; 5. NVM interrupts are not taken into account
BANKSEL NVMADRH
MOVF ADDRH,W
MOVWF NVMADRH               ; Load initial address
MOVF ADDRL,W
MOVWF NVMADRL
MOVLW LOW DATA_ADDR           ; Load initial data address
MOVWF FSR0L
MOVLW HIGH DATA_ADDR
MOVWF FSR0H
BCF NVMCON1,NVMREGS           ; Set PFM as write location
BSF NVMCON1,WREN              ; Enable writes
BSF NVMCON1,LWLO             ; Load only write latches
LOOP
MOVIW FSR0++
MOVWF NVMDATL             ; Load first data byte
MOVIW FSR0++
MOVWF NVMDATH               ; Load second data byte
CALL UNLOCK_SEQ             ; If not, go load latch
INCF NVMADRL,F              ; Increment address
MOVF NVMADRL,W
XORLW 0x1F                  ; Check if lower bits of address are 00000
ANDLW 0x1F                  ; and if on last of 32 addresses
BTFSC STATUS,Z             ; Last of 32 words?
GOTO START_WRITE            ; If so, go write latches into memory
GOTO LOOP
START_WRITE
BCF NVMCON1,LWLO            ; Latch writes complete, now write memory
CALL UNLOCK_SEQ             ; Perform required unlock sequence
BCF NVMCON1,LWLO            ; Disable writes
UNLOCK_SEQ
MOVLW 55h
BCF INTCON,GIE               ; Disable interrupts
MOVWF NVMCON2                ; Begin unlock sequence
MOVLW AAh
MOVWF NVMCON2
BSF NVMCON1,WR
BSF INTCON,GIE               ; Unlock sequence complete, re-enable interrupts
```

REGISTER 13-5: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER

U-0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—	NVMREGS	LWLO	FREE	WRERR(1,2,3)	WREN	WR(4,5,6)	RD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **Unimplemented:** Read as '0'

bit 6 **NVMREGS:** Configuration Select bit
1 = Access EEPROM, DIA, DCI, Configuration, User ID and Device ID Registers
0 = Access PFM

bit 5 **LWLO:** Load Write Latches Only bit
When FREE = 0:
1 = The next WR command updates the write latch for this word within the row; no memory operation is initiated.
0 = The next WR command writes data or erases
Otherwise: The bit is ignored

bit 4 **FREE:** PFM Erase Enable bit
When NVMREGS:NVMADR points to a PFM location:
1 = Performs an erase operation with the next WR command; the 32-word pseudo-row containing the indicated address is erased (to all 1s) to prepare for writing.
0 = All erase operations have completed normally

bit 3 **WRERR:** Program/Erase Error Flag bit(1,2,3)
This bit is normally set by hardware.
1 = A write operation was interrupted by a Reset, interrupted unlock sequence, or WR was written to one while NVMADR points to a write-protected address.
0 = The program or erase operation completed normally

bit 2 **WREN:** Program/Erase Enable bit
1 = Allows program/erase cycles
0 = Inhibits programming/erasing of program Flash

bit 1 **WR:** Write Control bit(4,5,6)
When NVMREG:NVMADR points to a PFM location:
1 = Initiates the operation indicated by Table 13-4
0 = NVM program/erase operation is complete and inactive.

bit 0 **RD:** Read Control bit(7)
1 = Initiates a read at address = NVMADR1, and loads data to NVMDAT Read takes one instruction cycle and the bit is cleared when the operation is complete. The bit can only be set (not cleared) in software.
0 = NVM read operation is complete and inactive

Note 1: Bit is undefined while WR = 1.
2: Bit must be cleared by software; hardware will not clear this bit.
3: Bit may be written to '1' by software in order to implement test sequences.
4: This bit can only be set by following the unlock sequence of **Section 13.4.2 "NVM Unlock Sequence"**.
5: Operations are self-timed, and the WR bit is cleared by hardware when complete.
6: Once a write operation is initiated, setting this bit to zero will have no effect.
7: Reading from EEPROM loads only NVMDATL<7:0> (Register 13-1).

REGISTER 14-3: LATA: PORTA DATA LATCH REGISTER

R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATA7	LATA6	—	LATA4	LATA3	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **LATA<7:6>**: RA<7:6> Output Latch Value bits(1)

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **LATA<4:0>**: RA<4:0> Output Latch Value bits(1)

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 14-4: ANSELA: PORTA ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSA7	ANSA6	—	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **ANSA<7:6>**: Analog Select between Analog or Digital Function on pins RA<7:6>, respectively
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **ANSA<4:0>**: Analog Select between Analog or Digital Function on pins RA<4:0>, respectively
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

TABLE 15-1: PPS INPUT SIGNAL ROUTING OPTIONS

INPUT SIGNAL NAME	Input Register Name	Default Location at POR	Remappable to Pins of PORTx												
			PIC16(L)F19155/56			PIC16(L)F19175/76				PIC16(L)F19185/86					
			PORTA	PORTB	PORTC	PORTA	PORTB	PORTC	PORTD	PORTA	PORTB	PORTC	PORTD	PORTE	PORTF
INT	INTPPS	RB0	•	•		•	•			•	•				
T0CKI	T0CKIPPS	RA4	•	•		•	•			•					•
T1CKI	T1CKIPSS	RC0	•		•	•		•				•		•	
T1G	T1GPPS	RB5		•	•		•	•			•	•			
T2IN	T2INPPS	RC3	•		•	•		•		•		•			
T4IN	T4INPPS	RC1		•	•		•	•			•	•			
CCP1	CCP1PPS	RC2		•	•		•	•				•			•
CCP2	CCP2PPS	RC1		•	•		•	•				•			•
SMT1WIN	SMT1WINPPS	RC0		•	•		•	•				•			•
SMT1SIG	SMT1SIGPPS	RC1		•	•		•	•				•			•
CWG1IN	CWG1INPPS	RB0		•	•		•		•		•		•		
CLCIN0	CLCIN0PPS	RA0	•		•	•		•		•		•			
CLCIN1	CLCIN1PPS	RA1	•		•	•		•		•		•			
CLCIN2	CLCIN2PPS	RB6		•	•		•		•		•		•		
CLCIN3	CLCIN3PPS	RB7		•	•		•		•		•		•		
ADCACT	ADACTPPS	RB4		•	•		•		•		•		•		
SCK1/SCL1	SSP1CLKPPS	RC3		•	•		•	•			•	•			
SDI1/SDA1	SSP1DATPPS	RC4		•	•		•	•			•	•			
SS1	SSP1SS1PPS	RA5	•		•	•			•	•			•		
RX1/DT1	RX1PPS	RC7		•	•		•	•				•			•
CK1	TX1PPS	RC6		•	•		•	•				•			•
RX2/DT2	RX2PPS	RB7		•	•		•		•		•		•		
CK2	TX2PPS	RB6		•	•		•		•		•		•		

19.6 Register Definitions: ADC Control

REGISTER 19-1: ADCON0: ADC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0	R/W-0/0	U-0	R/W/HC-0
ON	CONT	—	CS	—	FM	—	GO
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **ON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled

bit 6 **CONT:** ADC Continuous Operation Enable bit(2)
1 = GO is retriggered upon completion of each conversion trigger until ADTIF is set (if ADSOI is set) or until GO is cleared (regardless of the value of ADSOI)
0 = ADC is cleared upon completion of each conversion trigger

bit 5 **Unimplemented:** Read as '0'

bit 4 **CS:** ADC Clock Selection bit
1 = Clock supplied from FRC dedicated oscillator
0 = Clock supplied by FOSC, divided according to ADCLK register

bit 3 **Unimplemented:** Read as '0'

bit 2 **FM:** ADC results Format/alignment Selection
1 = ADRES and PREV data are right-justified
0 = ADRES and PREV data are left-justified, zero-filled

bit 1 **Unimplemented:** Read as '0'

bit 0 **GO:** ADC Conversion Status bit(1)
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle. The bit is cleared by hardware as determined by the CONT bit
0 = ADC conversion completed/not in progress

Note 1: This bit requires ON bit to be set.

2: If cleared by software while a conversion is in progress, the results of the conversion up to this point will be transfered to ADRES and the state machine will be reset, but the ADIF interrupt flag bit will not be set; filter and threshold operations will not be performed.

REGISTER 19-13: ADCAP: ADC ADDITIONAL SAMPLE CAPACITOR SELECTION REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	ADCAP<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented**: Read as ‘0’

bit 4-0 **ADCAP<4:0>**: ADC Additional Sample Capacitor Selection bits
11111 = 31 pF
11110 = 30 pF
11101 = 29 pF
•
•
•
00011 = 3 pF
00010 = 2 pF
00001 = 1 pF
00000 = No additional capacitance

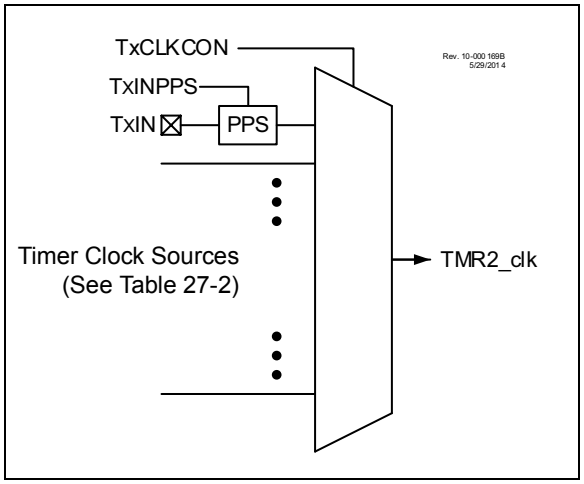
REGISTER 19-14: ADRPT: ADC REPEAT SETTING REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RPT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **RPT<7:0>**: ADC Repeat Threshold bits
Determines the number of times that the ADC is triggered before the threshold is checked when the computation is Low-pass Filter, Burst Average, or Average modes. See Table 19-2 for more details.

FIGURE 27-2: TIMER2/4 CLOCK SOURCE BLOCK DIAGRAM



27.1 Timer2/4 Operation

Timer2 operates in three major modes:

- Free Running Period
- One-shot
- Monostable

Within each mode there are several options for starting, stopping, and reset. Table 27-1 lists the options.

In all modes, the TMR2 count register is incremented on the rising edge of the clock signal from the programmable prescaler. When TMR2 equals T2PR, a high level is output to the postscaler counter. TMR2 is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a TMR2 count Reset. In Gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the TMR2 count is reset on either the level or edge from the external source.

The TMR2 and T2PR registers are both directly readable and writable. The TMR2 register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset
- External Reset Source event that resets the timer.

Note:	TMR2 is not cleared when T2CON is written.

27.1.1 FREE RUNNING PERIOD MODE

The value of TMR2 is compared to that of the Period register, T2PR, on each TMR2_clk cycle. When the two values match, the comparator resets the value of TMR2 to 00h on the next rising TMR2_clk edge and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS<4:0> bits of the TMRxCON1 register, a one TMR2_clk period wide pulse occurs on the TMR2_postscaled output, and the postscaler count is cleared.

27.1.2 ONE-SHOT MODE

The One-Shot mode is identical to the Free Running Period mode except that the ON bit is cleared and the timer is stopped when TMR2 matches T2PR and will not restart until the T2ON bit is cycled off and on. Postscaler OUTPS<4:0> values other than 0 are meaningless in this mode because the timer is stopped at the first period event and the postscaler is reset when the timer is restarted.

27.1.3 MONOSTABLE MODE

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

27.2 Timer2/4 Output

The Timer2 module's primary output is TMR2_postscaled, which pulses for a single TMR2_clk period when the postscaler counter matches the value in the OUTPS bits of the TMR2CON register. The T2PR postscaler is incremented each time the TMR2 value matches the T2PR value. This signal can be selected as an input to several other input modules:

- The ADC module, as an Auto-conversion Trigger
- COG, as an auto-shutdown source

In addition, the Timer2 is also used by the CCP module for pulse generation in PWM mode. Both the actual TMR2 value as well as other internal signals are sent to the CCP module to properly clock both the period and pulse width of the PWM signal. See **Section 29.0 "Capture/Compare/PWM Modules"** for more details on setting up Timer2/4 for use with the CCP, as well as the timing diagrams in **Section 27.5 "Operation Examples"** for examples of how the varying Timer2 modes affect CCP PWM output.

27.3 External Reset Sources

In addition to the clock source, the Timer2 also takes in an external Reset source. This external Reset source is selected for Timer2 with the T2RST register. This source can control starting and stopping of the timer, as well as resetting the timer, depending on which mode the timer is in. The mode of the timer is controlled by the MODE<4:0> bits of the TMRxHLT register. Edge-Triggered modes require six Timer clock periods between external triggers. Level-Triggered modes require the triggering level to be at least three Timer clock periods long. External triggers are ignored while in Debug Freeze mode.

31.3 Selectable Input Sources

The CWG generates the output waveforms from the input sources (See Register 31-9).

The input sources are selected using the CWG1ISM register.

31.4 Output Control

31.4.1 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the POLx bits of the CWG1CON1. Auto-shutdown and steering options are unaffected by polarity.

REGISTER 31-5: CWG1AS0: CWG1 AUTO-SHUTDOWN CONTROL REGISTER 0

R/W/HS-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	U-0	U-0
SHUTDOWN(1, 2)	REN	LSBD<1:0>		LSAC<1:0>		—	—
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SHUTDOWN:** Auto-Shutdown Event Status bit(1, 2)
- 1 = An Auto-Shutdown state is in effect
- 0 = No Auto-shutdown event has occurred

bit 6 **REN:** Auto-Restart Enable bit
- 1 = Auto-restart enabled
- 0 = Auto-restart disabled

bit 5-4 **LSBD<1:0>:** CWG1B and CWG1D Auto-Shutdown State Control bits
- 11 =A logic '1' is placed on CWG1B/D when an auto-shutdown event is present
- 10 =A logic '0' is placed on CWG1B/D when an auto-shutdown event is present
- 01 =Pin is tri-stated on CWG1B/D when an auto-shutdown event is present
- 00 =The inactive state of the pin, including polarity, is placed on CWG1B/D after the required dead-band interval

bit 3-2 **LSAC<1:0>:** CWG1A and CWG1C Auto-Shutdown State Control bits
- 11 =A logic '1' is placed on CWG1A/C when an auto-shutdown event is present
- 10 =A logic '0' is placed on CWG1A/C when an auto-shutdown event is present
- 01 =Pin is tri-stated on CWG1A/C when an auto-shutdown event is present
- 00 =The inactive state of the pin, including polarity, is placed on CWG1A/C after the required dead-band interval

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit may be written while EN = 0 (CWG1CON0 register) to place the outputs into the shutdown configuration.

2: The outputs will remain in auto-shutdown state until the next rising edge of the input signal after this bit is cleared.

32.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

32.1.1 DATA SELECTION

There are 40 signals available as inputs to the configurable logic. Four 40-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 32-2. Data inputs in the figure are identified by a generic numbered input name.

Table 32-2 correlates the generic input name to the actual signal for each CLC module. The column labeled 'LCxDyS<5:0> Value' indicates the MUX selection code for the selected data input. LCxDyS is an abbreviation to identify specific multiplexers: LCxD1S<5:0> through LCxD4S<5:0>.

Data inputs are selected with CLCxSEL0 through CLCxSEL3 registers (Register 32-3 through Register 32-6).

TABLE 32-2: CLCx DATA INPUT SELECTION

LCxDyS<5:0> Value	CLCx Input Source
100101 to 111111	Reserved
100100	EUSART2 (TX/CK) output
100011	EUSART2 (DT) output
100010	CWG1B output
100001	CWG1A output
100000	RTCC seconds
011111	MSSP1 SCK output
011110	MSSP1 SDO output
011101	EUSART1 (TX/CK) output
011100	EUSART1 (DT) output
011011	CLC4 output
011010	CLC3 output
011001	CLC2 output
011000	CLC1 output
010111	IOCIF
010110	ZCD output
010101	C2OUT
010100	C1OUT
010011	PWM4 output
010010	PWM3 output
010001	CCP2 output
010000	CCP1 output
001111	SMT overflow
001110	Timer4 overflow
001101	Timer2 overflow
001100	Timer1 overflow
001011	Timer0 overflow
001010	ADCRC
001001	SOSC
001000	MFINTOSC (32 kHz)
000111	MFINTOSC (500 kHz)
000110	LFINTOSC
000101	HFINTOSC
000100	FOSC
000011	CLCIN3PPS
000010	CLCIN2PPS
000001	CLCIN1PPS
000000	CLCIN0PPS

34.1.2.3 Receive Interrupts

The RXxIF interrupt flag bit of the PIR3 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RXxIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RXxIF interrupts are enabled by setting all of the following bits:

- RXxIE, Interrupt Enable bit of the PIE3 register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RXxIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

34.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCxSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCxREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCxSTA register which resets the EUSART. Clearing the CREN bit of the RCxSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive FIFO have framing errors, repeated reads of the RCxREG will not clear the FERR bit.

34.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCxSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCxSTA register or by resetting the EUSART by clearing the SPEN bit of the RCxSTA register.

34.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

34.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RXxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

REGISTER 34-4: RCxREG(1): RECEIVE DATA REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RCxREG<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RCxREG<7:0>:** Lower eight bits of the received data; read-only; see also RX9D (Register 34-2)

Note 1: RCxREG (including the 9th bit) is double buffered, and data is available while new data is being received.

REGISTER 34-5: TXxREG(1): TRANSMIT DATA REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXxREG<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TXxREG<7:0>:** Lower eight bits of the received data; read-only; see also RX9D (Register 34-1)

Note 1: TXxREG (including the 9th bit) is double buffered, and can be written when previous data has started shifting.

REGISTER 34-6: SPxBRGL(1): BAUD RATE GENERATOR REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPxBRG<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SPxBRG<7:0>:** Lower eight bits of the Baud Rate Generator

Note 1: Writing to SP1BRG resets the BRG counter.

REGISTER 34-7: SPxBRGH(1, 2): BAUD RATE GENERATOR HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPxBRG<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **SPxBRG<15:8>:** Upper eight bits of the Baud Rate Generator

Note 1: SPxBRGH value is ignored for all modes unless BAUDxCON<BRG16> is active.

2: Writing to SPxBRGH resets the BRG counter.

TABLE 35-10: SUMMARY OF REGISTERS ASSOCIATED WITH LCD MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182
PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
PMD5	—	SMT1MD	LCDMD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	274
LCDCON	LCDEN	SLPEN	WERR	CS	LMUX<3:0>				622
LCDPS	WFT	—	LCDA	WA	LP<3:0>				623
LCDSE0	SE07	SE06	SE05	SE04	SE03	SE02	SE01	SE00	624
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	624
LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	624
LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	624
LCDSE4	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	624
LCDSE5	SE47	SE46	SE45	SE44	SE43	SE42	SE41	SE40	624
LCDVCON1	LPEN	EN5V	—	—	—	BIAS<2:0>			625
LCDVCON2	—	—	—	—	LCDVSRC<3:0>				626
LCDREF	—	—	—	—	—	LCDCST<2:0>			628
LCDRL	LRLAP<1:0>		LRLBP<1:0>		LCDIRI	LRLAT<2:0>			627
LCDDATA0	S07C0	S06C0	—	S04C0	S03C0	S02C0	S01C0	S00C0	624
LCDDATA1	S15C0	S14C0	S13C0	—	S11C0	S10C0	S09C0	S08C0	624
LCDDATA2	S23C0	S22C0	—	S20C0	S19C0	S18C0	—	—	624
LCDDATA3	S31C0	S30C0	S29C0	S28C0	S27C0	S26C0	S25C0	S24C0	624
LCDDATA4	—	—	—	—	—	S34C0	S33C0	S32C0	624
LCDDATA5	S47C0	S46C0	S45C0	S44C0	S43C0	S42C0	S41C0	S40C0	624
LCDDATA6	S07C1	S06C1	—	S04C1	S03C1	S02C1	S01C1	S00C1	624
LCDDATA7	S15C1	S14C1	S13C1	—	S11C1	S10C1	S09C1	S08C1	624
LCDDATA8	S23C1	S22C1	—	S20C1	S19C1	S18C1	—	—	624
LCDDATA9	S31C1	S30C1	S29C1	S28C1	S27C1	S26C1	S25C1	S24C1	624
LCDDATA10	—	—	—	—	—	S34C1	S33C1	S32C1	624
LCDDATA11	S47C1	S46C1	S45C1	S44C1	S43C1	S42C1	S41C1	S40C1	624
LCDDATA12	S07C2	S06C2	—	S04C2	S3C2	S2C2	S01C2	S00C2	624
LCDDATA13	S15C2	S14C2	S13C2	—	S11C2	S10C2	S09C2	S08C2	624
LCDDATA14	S23C2	S22C2	—	S20C2	S19C2	S18C2	—	—	624
LCDDATA15	S31C2	S30C2	S29C2	S28C2	S27C2	S26C2	S25C2	S24C2	624
LCDDATA16	—	—	—	—	—	S34C2	S33C2	S32C2	624
LCDDATA17	S47C2	S46C2	S45C2	S44C2	S43C2	S42C2	S41C2	S40C2	624
LCDDATA18	S15C3	S14C3	S13C3	—	SE11C3	S10C3	S09C3	S08C3	624
LCDDATA19	S23C3	S22C3	—	S20C3	S19C3	S18C3	—	—	624
LCDDATA20	S31C3	S30C3	S29C3	S28C3	S27C3	S26C3	S25C3	S24C3	624
LCDDATA21	—	—	—	—	—	S34C3	S33C3	S32C3	624
LCDDATA22	S47C3	S46C3	S45C3	S44C3	S43C3	S42C3	S41C3	S40C3	624
LCDDATA23	S07C4	S06C4	—	S04C4	S03C4	S02C4	S01C4	S00C4	624
LCDDATA24	S15C4	S14C4	S13C4	—	S11C4	S10C4	S09C4	S08C4	624
LCDDATA25	S23C4	S22C4	—	S20C4	S19C4	S18C4	—	—	624
LCDDATA26	S31C4	S30C4	S29C4	S28C4	S27C4	S26C4	S25C4	S24C4	624
LCDDATA27	—	—	—	—	—	S34C4	S33C4	S32C4	624
LCDDATA28	S47C4	S46C4	S45C4	S44C4	S43C4	S42C4	S41C4	S40C4	624
LCDDATA29	S07C5	S06C5	—	S04C5	S03C5	S02C5	S01C5	S00C5	624
LCDDATA30	S15C5	S14C5	S13C5	—	S11C5	S10C5	S09C5	S08C5	624
LCDDATA31	S23C5	S22C5	—	S20C5	S19C5	S18C5	—	—	624
LCDDATA32	S31C5	S30C5	S29C5	S28C5	S27C5	S26C5	S25C5	S24C5	624
LCDDATA33	—	—	—	—	—	S34C5	S33C5	S32C5	624

41.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

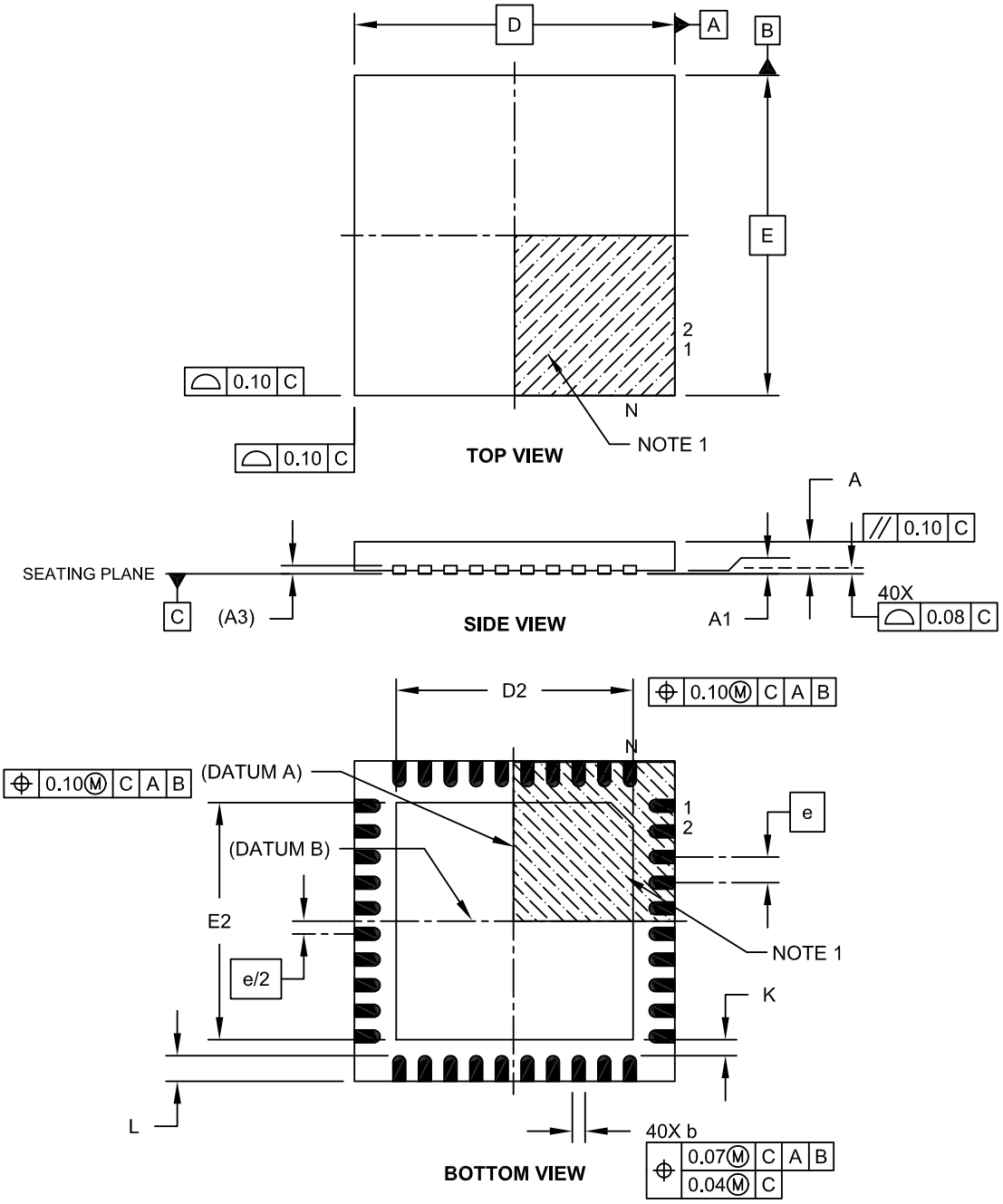
41.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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