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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19186-e-pt

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 60 (Continued)											
1E6Bh	—	Unimplemented								---- ----	---- ----
1E6Ch	—	Unimplemented								---- ----	---- ----
1E6Dh	—	Unimplemented								---- ----	---- ----
1E6Eh	—	Unimplemented								---- ----	---- ----
1E6Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19155/56/75/76/85/86 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 63 (Continued)											
1FA1h	—	Unimplemented								---- ----	---- ----
1FA2h	—	Unimplemented								---- ----	---- ----
1FA3h	—	Unimplemented								---- ----	---- ----
1FA4h	—	Unimplemented								---- ----	---- ----
1FA5h	—	Unimplemented								---- ----	---- ----
1FA6h	—	Unimplemented								---- ----	---- ----
1FA7h	—	Unimplemented								---- ----	---- ----
1FA8h	—	Unimplemented								---- ----	---- ----
1FA9h	—	Unimplemented								---- ----	---- ----
1FAAh	—	Unimplemented								---- ----	---- ----
1FABh	—	Unimplemented								---- ----	---- ----
1FACh	—	Unimplemented								---- ----	---- ----
1FADh	—	Unimplemented								---- ----	---- ----
1FAEh	—	Unimplemented								---- ----	---- ----
1FAFh	—	Unimplemented								---- ----	---- ----
1FB0h	—	Unimplemented								---- ----	---- ----
1FB1h	—	Unimplemented								---- ----	---- ----
1FB2h	—	Unimplemented								---- ----	---- ----
1FB3h	—	Unimplemented								---- ----	---- ----
1FB4h	—	Unimplemented								---- ----	---- ----
1FB5h	—	Unimplemented								---- ----	---- ----
1FB6h	—	Unimplemented								---- ----	---- ----
1FB7h	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 5-1: BOOT BLOCK SIZE BITS

$\overline{\text{BBEN}}$	BBSIZE[2:0]	Actual Boot Block Size User Program Memory Size (words)			Last Boot Block Memory Access
		8k	16k	32k	
1	xxx	0	0	0	—
0	111	512	512	512	01FFh
0	110	1024	1024	1024	03FFh
0	101	2048	2048	2048	07FFh
0	100	4096	4096	4096	0FFFh
0	011	Note 1	8192	8192	1FFFh
0	010			16384	3FFFh
0	001				3FFFh
0	000				3FFFh

Note 1: The maximum boot block size is half the user program memory size. All selections higher than the maximum are set to half size. For example, all BBSIZE = 000 - 100 produce a boot block size of 4 kW on a 8 kW device.

REGISTER 5-5: CONFIGURATION WORD 5: CODE PROTECTION

U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—
bit 13					bit 8

U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1
—	—	—	—	—	—	—	$\overline{\text{CP}}$
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	x = Bit is unknown	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	W = Writable bit	n = Value when blank or after Bulk Erase

bit 13-1 **Unimplemented:** Read as ‘1’

bit 0 **$\overline{\text{CP}}$:** Program Flash Memory Code Protection bit
1 = Program Flash Memory code protection disabled
0 = Program Flash Memory code protection enabled

REGISTER 10-4: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
—	ZCDIE	—	—	—	—	C2IE	C1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6 **ZCDIE:** Zero-Cross Detection (ZCD) Interrupt Enable bit
- 1 = Enables the ZCD interrupt
- 0 = Disables the ZCD interrupt

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **C2IE:** Comparator C2 Interrupt Enable bit
- 1 = Enables the Comparator C2 interrupt
- 0 = Disables the Comparator C2 interrupt

bit 0 **C1IE:** Comparator C1 Interrupt Enable bit
- 1 = Enables the Comparator C1 interrupt
- 0 = Disables the Comparator C1 interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

REGISTER 12-2: WDTCON1: WATCHDOG TIMER CONTROL REGISTER 1

U-0	R/W(3)-q/q(1)	R/W(3)-q/q(1)	R/W(3)-q/q(1)	U-0	R/W(4)-q/q(2)	R/W(4)-q/q(2)	R/W(4)-q/q(2)
—	WDTCS<2:0>			—	WINDOW<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **WDTCS<2:0>:** Watchdog Timer Clock Select bits

111 = Reserved
•
•
•
010 = SOSC 32.768 kHz
001 = MFINTOSC 31.25 kHz
000 = LFINTOSC 31 kHz

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **WINDOW<2:0>:** Watchdog Timer Window Select bits

WINDOW<2:0>	Window delay Percent of time	Window opening Percent of time
111	N/A	100
110	12.5	87.5
101	25	75
100	37.5	62.5
011	50	50
010	62.5	37.5
001	75	25
000	87.5	12.5

Note 1: If WDTCCS <2:0> in CONFIG3 = 111, the Reset value of WDTCS<2:0> is 000.

2: The Reset value of WINDOW<2:0> is determined by the value of WDTCWS<2:0> in the CONFIG3 register.

3: If WDTCCS<2:0> in CONFIG3 ≠ 111, these bits are read-only.

4: If WDTCWS<2:0> in CONFIG3 ≠ 111, these bits are read-only.

TABLE 14-5: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	241
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	241
LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	242
ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	242
WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	243
ODCOND	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	243
SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	244
INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	244

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

Note 1: Unimplemented, read as '1'.

22.3 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 22-1) contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- Hysteresis enable
- Timer1 output synchronization

The CMxCON1 register (see Register 22-2) contains Control bits for the following:

- Interrupt on positive/negative edge enables
- The CMxNSEL and CMxPSEL (Register 22-3 and Register 22-4) contain control bits for the following:
  - Positive input channel selection
  - Negative input channel selection

22.3.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

Note:	Setting the C2ON bit of the CM2CON0 register enables the CMP2 along with LFINTOSC. CMP2 is a clocked comparator and LFINTOSC is the clock source.

22.3.2 COMPARATOR OUTPUT

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register.

The comparator output can also be routed to an external pin through the RxyPPS register (Register 15-2). The corresponding TRIS bit must be clear to enable the pin as an output.

Note 1:	The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

22.3.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 22-2 shows the output state versus input conditions, including polarity control.

TABLE 22-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

22.13 Register Definitions: Comparator Control

REGISTER 22-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	U-0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
ON	OUT	—	POL	—	—	HYS	SYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **OUT:** Comparator Output bit
If CxPOL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If CxPOL = 0 (noninverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **Unimplemented:** Read as '0'

bit 4 **POL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **HYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **SYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous

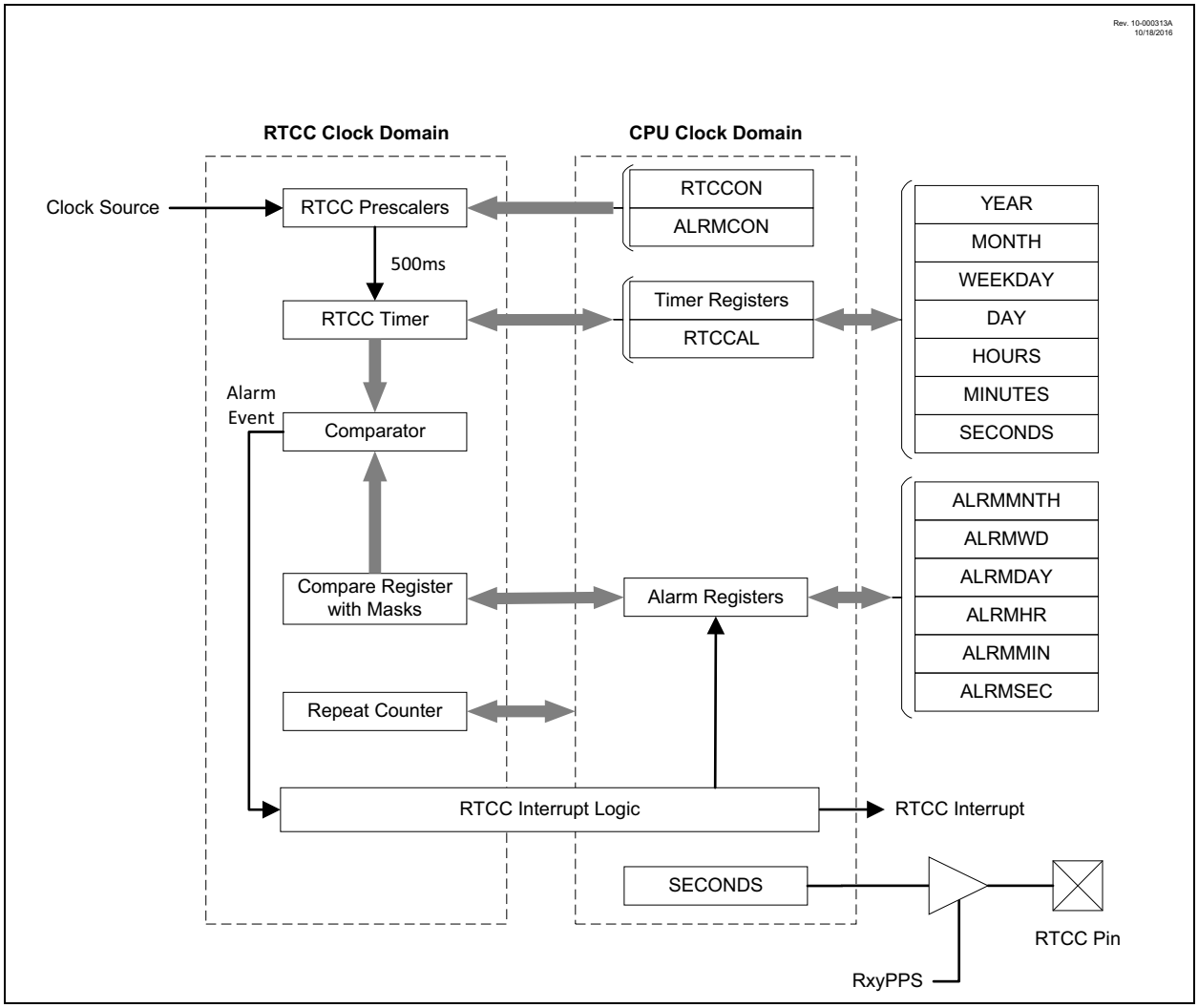
24.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

The PIC16(L)F19155/56/75/76/85/86 family of devices is equipped with a Real-Time Clock and Calendar (RTCC) module, designed to maintain accurate time measurement for extended periods, with little or no intervention from the CPU. The module is optimized for low-power operation in order to provide extended battery life. The key features include:

- Time: Hours, Minutes and Seconds
- 24-hour Format (Military Time)
- Calendar: Weekday, Date, Month and Year
- Year Range: 2000 to 2099
- Leap Year Correction
- Configurable Alarm
- BCD Format for Compact Firmware
- Half-second Synchronization and Visibility
- User Calibration with Auto-Adjust
- Multiple Clock Sources
- Low-Power Optimization

Figure 24-1 is a simplified block diagram of the RTCC module.

FIGURE 24-1: RTCC BLOCK DIAGRAM



26.0 TIMER1 MODULE WITH GATE CONTROL

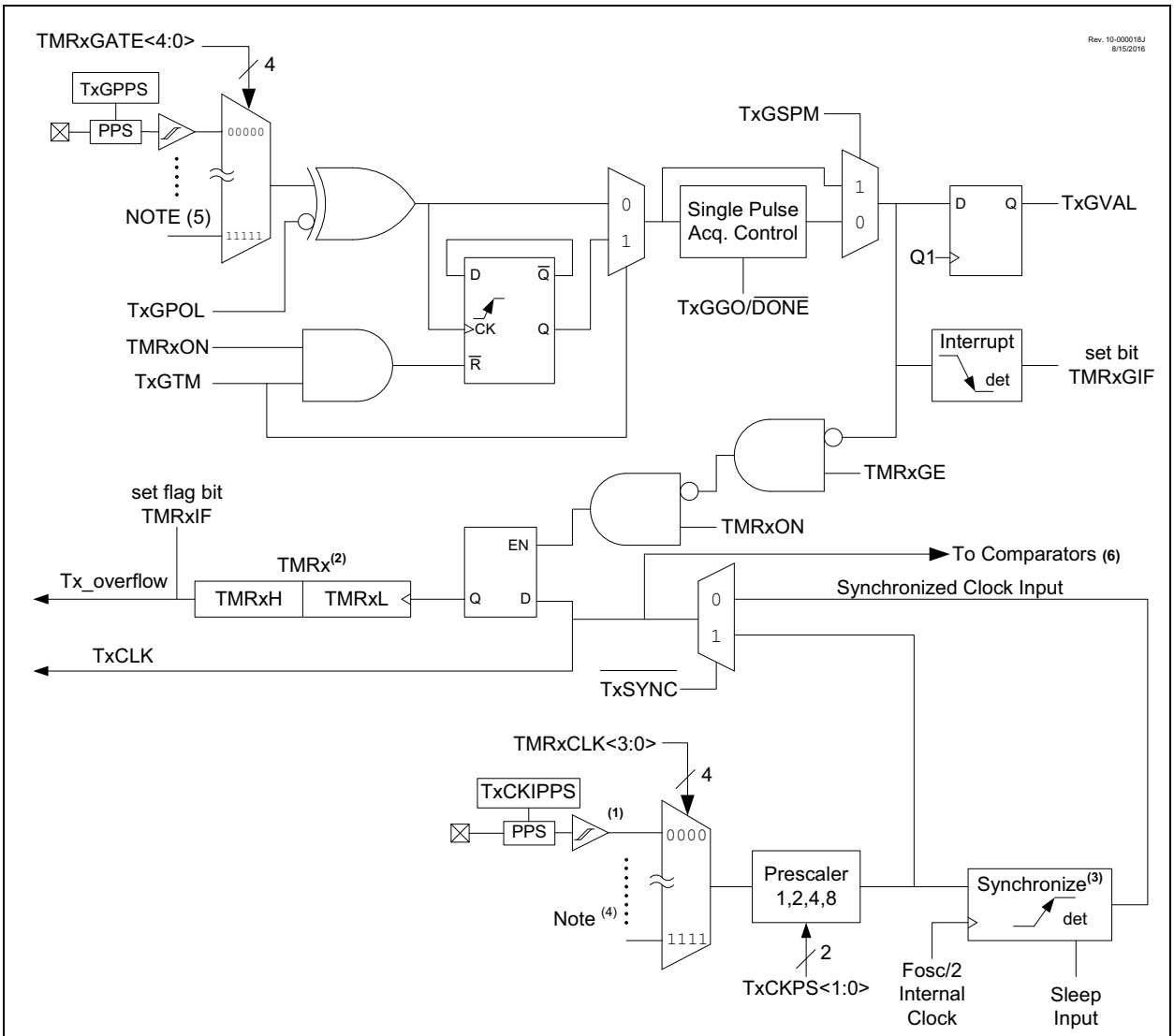
The Timer1 module is 16-bit timer/counters with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 2-bit prescaler
- Clock source for optional comparator synchronization
- Multiple Timer1 gate (count enable) sources
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Auto-conversion Trigger (with CCP)
- Selectable Gate Source Polarity
- Gate Toggle mode
- Gate Single-Pulse mode
- Gate Value Status
- Gate Event Interrupt

Figure 26-1 is a block diagram of the Timer1 module.

This device has one instance of Timer1 type modules.

FIGURE 26-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is high speed type when using TxCKIPPS.
2: TMRx register increments on rising edge.
3: Synchronize does not operate while in Sleep.
4: See Register 26-3 for Clock source selections.
5: See Register 26-4 for GATE source selections.
6: Synchronized comparator output should not be used in conjunction with synchronized input clock.

28.2 SMT Operation

The core of the module is the 24-bit counter, SMTxTMR combined with a complex data acquisition front-end. Depending on the mode of operation selected, the SMT can perform a variety of measurements summarized in Table .

28.2.1 CLOCK SOURCES

Clock sources available to the SMT include:

- FOSC
- FOSC/4
- HFINTOSC
- MFINTOSC (500 kHz and 31.25 kHz)
- LFINTOSC
- SOSC

The SMT clock source is selected by configuring the CSEL<2:0> bits in the SMTxCLK register. The clock source can also be prescaled using the PS<1:0> bits of the SMTxCON0 register. The prescaled clock source is used to clock both the counter and any synchronization logic used by the module.

28.2.2 PERIOD MATCH INTERRUPT

Similar to other timers, the SMT triggers an interrupt when SMTxTMR rolls over to '0'. This happens when SMTxTMR = SMTxPR, regardless of mode. Hence, in any mode that relies on an external signal or a window to reset the timer, proper operation requires that SMTxPR be set to a period larger than that of the expected signal or window.

28.3 Basic Timer Function Registers

The SMTxTMR time base and the SMTxCPW/SMTxPR/SMTxCPR buffer registers serve several functions and can be manually updated using software.

28.3.1 TIME BASE

The SMTxTMR is the 24-bit counter that is the center of the SMT. It is used as the basic counter/timer for measurement in each of the modes of the SMT. It can be reset to a value of 24'h00_0000 by setting the RST bit of the SMTxSTAT register. It can be written to and read from software, but it is not guarded for atomic access, therefore reads and writes to the SMTxTMR should only be made when the GO = 0, or the software should have other measures to ensure integrity of SMTxTMR reads/writes.

28.3.2 PULSE-WIDTH LATCH REGISTERS

The SMTxCPW registers are the 24-bit SMT pulse width latch. They are used to latch in the value of the SMTxTMR when triggered by various signals, which are determined by the mode the SMT is currently in.

The SMTxCPW registers can also be updated with the current value of the SMTxTMR value by setting the CPWUP bit of the SMTxSTAT register.

28.3.3 PERIOD LATCH REGISTERS

The SMTxCPR registers are the 24-bit SMT period latch. They are used to latch in values of the SMTxTMR when triggered by various other signals, which are determined by the mode the SMT is currently in.

The SMTxCPR registers can also be updated with the current value of the SMTxTMR value by setting the CPRUP bit in the SMTxSTAT register.

28.4 Halt Operation

The counter can be prevented from rolling-over using the STP bit in the SMTxCON0 register. When halting is enabled, the period match interrupt persists until the SMTxTMR is reset (either by a manual Reset, **Section 28.3.1 "Time Base"**) or by clearing the SMTxGO bit of the SMTxCON1 register and writing the SMTxTMR values in software.

28.5 Polarity Control

The three input signals for the SMT have polarity control to determine whether or not they are active high/positive edge or active low/negative edge signals.

The following bits apply to Polarity Control:

- WSEL bit (Window Polarity)
- SSEL bit (Signal Polarity)
- CSEL bit (Clock Polarity)

These bits are located in the SMTxCON0 register.

28.6 Status Information

The SMT provides input status information for the user without requiring the need to deal with the polarity of the incoming signals.

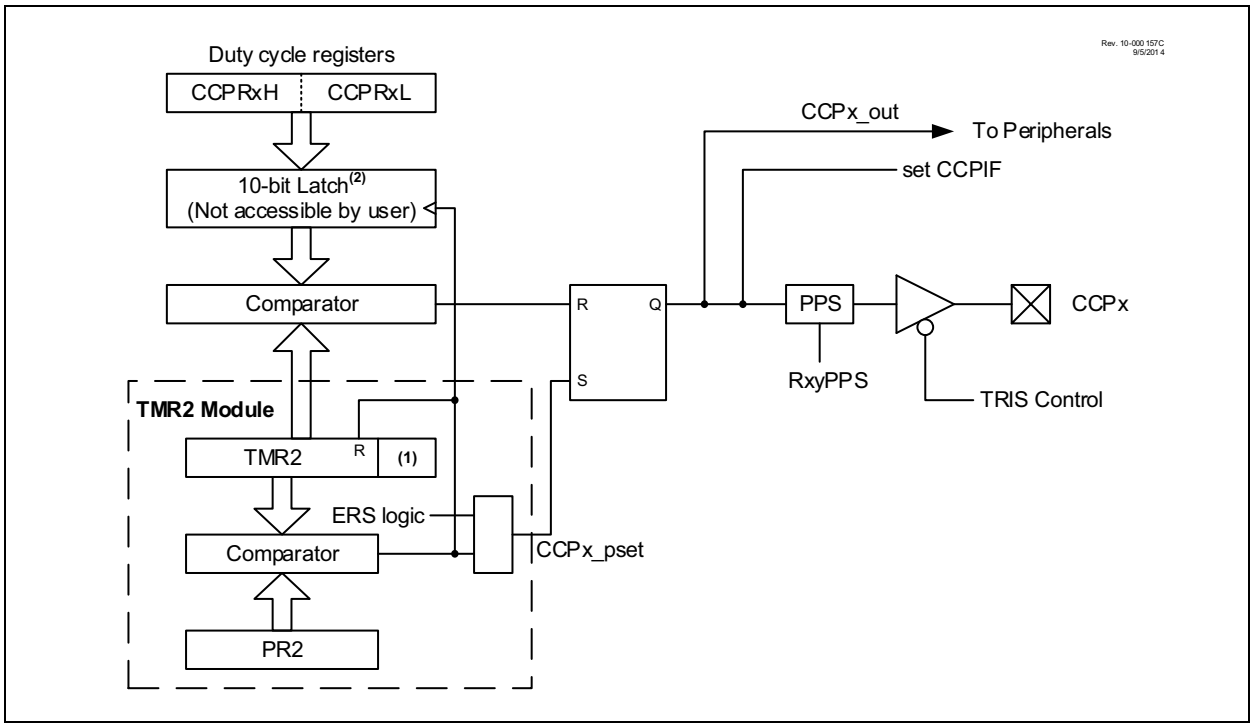
28.6.1 WINDOW STATUS

Window status is determined by the WS bit of the SMTxSTAT register. This bit is only used in Windowed Measure, Gated Counter and Gated Window Measure modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

28.6.2 SIGNAL STATUS

Signal status is determined by the AS bit of the SMTxSTAT register. This bit is used in all modes except Window Measure, Time of Flight and Capture modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

FIGURE 29-4: SIMPLIFIED PWM BLOCK DIAGRAM



29.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Use the desired output pin RxyPPS control to select CCPx as the source and disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register, and the CCPRxH register with the PWM duty cycle value and configure the CCPxFMT bit of the CCPxCON register to set the proper register alignment.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR4 register. See Note below.
   - Configure the CKPS bits of the T2CON register with the Timer prescale value.
   - Enable the Timer by setting the Timer2 ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until the Timer overflows and the TMR2IF bit of the PIR4 register is set. See Note below.
   - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note:	In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

29.3.3 CCP/PWM CLOCK SELECTION

The PIC16(L)F19155/56/75/76/85/86 allows each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

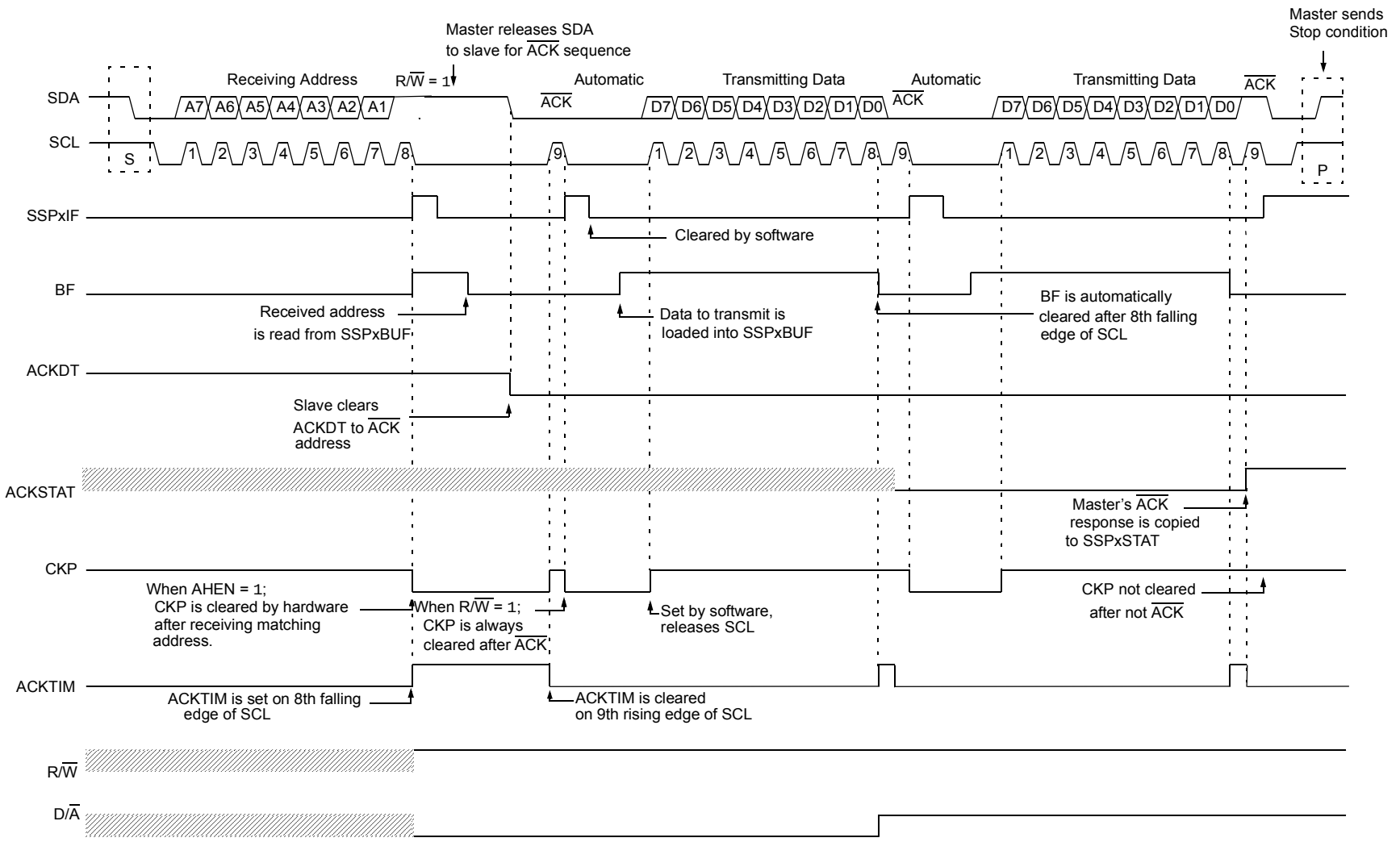
TABLE 30-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				404
T2TMR	Holding Register for the 8-bit TMR2 Register								384*
T2PR	TMR2 Period Register								384*
RxyPPS	—	—	—	RxyPPS<4:0>					265
CWG1ISM	—	—	—	—	IS<3:0>				492
CLCxSELy	—	—	LCxDyS<5:0>						503
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	222
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	235
PWM3CON	PWM3EN	—	PWM3OUT	PWM3POL	—	—	—	—	
PWM4CON	PWM4EN	—	PWM4OUT	PWM4POL	—	—	—	—	
PWM3DCL	PWM3DC1	PWM3DC0	—	—	—	—	—	—	
PWM3DCH	PWM3DC9	PWM3DC8	PWM3DC7	PWM3DC6	PWM3DC5	PWM3DC4	PWM3DC3	PWM3DC2	
PWM4DCL	PWM4DC1	PWM4DC0	—	—	—	—	—	—	
PWM4DCH	PWM4DC9	PWM4DC8	PWM4DC7	PWM4DC6	PWM4DC5	PWM4DC4	PWM4DC3	PWM4DC2	

Legend: - = Unimplemented locations, read as '0'. Shaded cells are not used by the PWMx module.

*Page provides register information.

FIGURE 33-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)



33.6.10 SLEEP OPERATION

While in Sleep mode, the I^2C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

33.6.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

33.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit of the SSPxSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCL1IF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

33.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCL1IF and reset the I^2C port to its Idle state (Figure 33-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 33-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

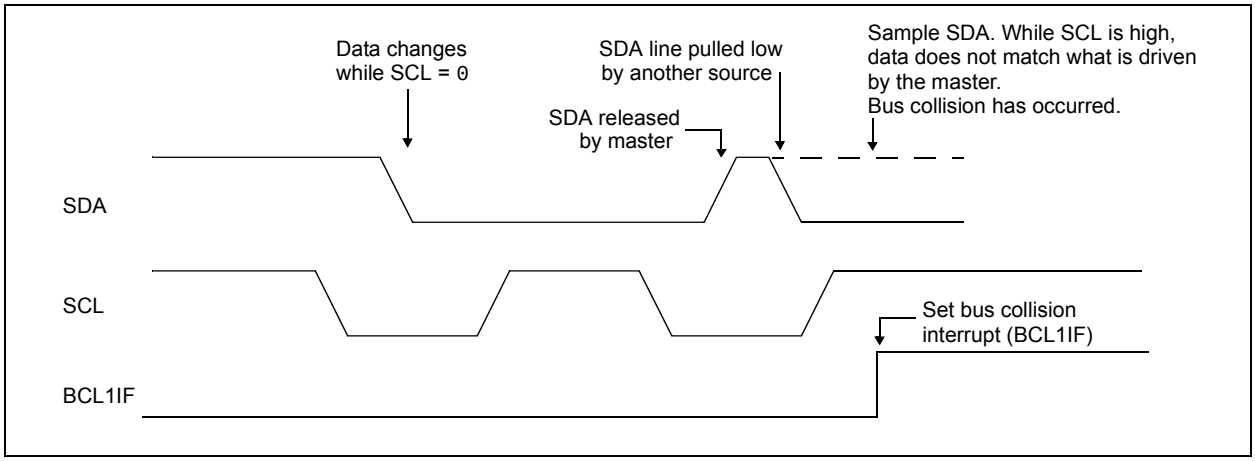


FIGURE 35-17: TYPE-A WAVEFORMS IN 1/4 MUX, 1/3 BIAS DRIVE

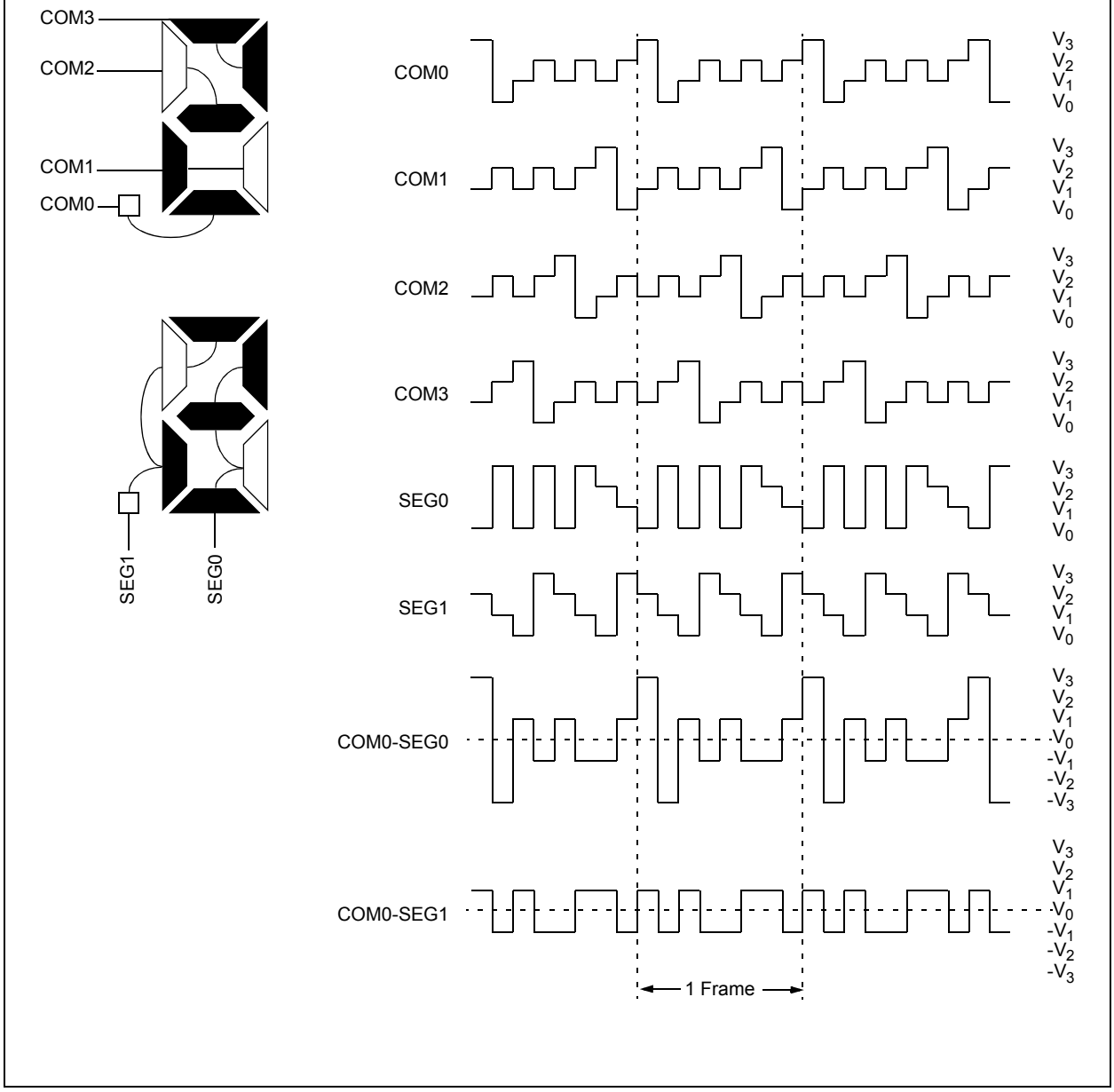
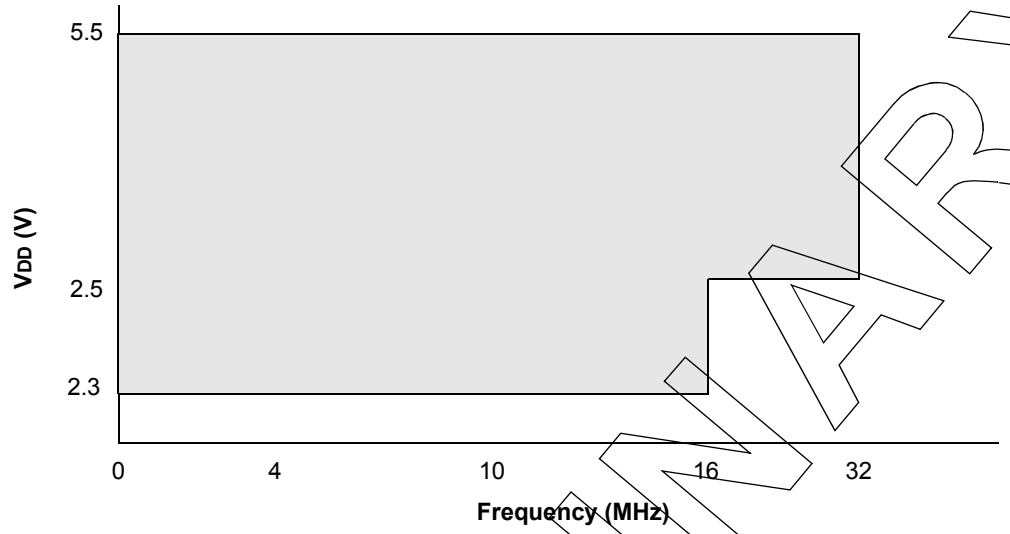


TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19155/56/75/76/85/86 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
68Dh	—	Unimplemented								
68Eh	—	Unimplemented								
68Fh	—	Unimplemented								
690h	—	Unimplemented								
691h	—	Unimplemented								
692h	—	Unimplemented								
693h	—	Unimplemented								
694h	—	Unimplemented								
695h	—	Unimplemented								
696h	—	Unimplemented								
697h	—	Unimplemented								
698h	—	Unimplemented								
699h	—	Unimplemented								
69Ah	—	Unimplemented								
69Bh	—	Unimplemented								
69Ch	—	Unimplemented								
69Dh	—	Unimplemented								
69Eh	—	Unimplemented								
69Fh	—	Unimplemented								
70Ch	PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	174
70Dh	PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
70Eh	PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	176
70Fh	PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	177
710h	PIR4	—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF	178
711h	PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	179
712h	PIR6	CRIF	—	—	—	—	—	CCP2IF	CCP1IF	180
713h	PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	181
714h	PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182
715h	—	Unimplemented								
716h	PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	165
717h	PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	166
718h	PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	167
719h	PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	168
71Ah	PIE4	—	—	—	—	TMR4IF	—	TMR2IE	TMR1IE	169
71Bh	PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	170
71Ch	PIE6	CRIE	—	—	—	—	—	CCP2IE	CCP1IE	171
71Dh	PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	172
71Eh	PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
71Fh	—	Unimplemented								

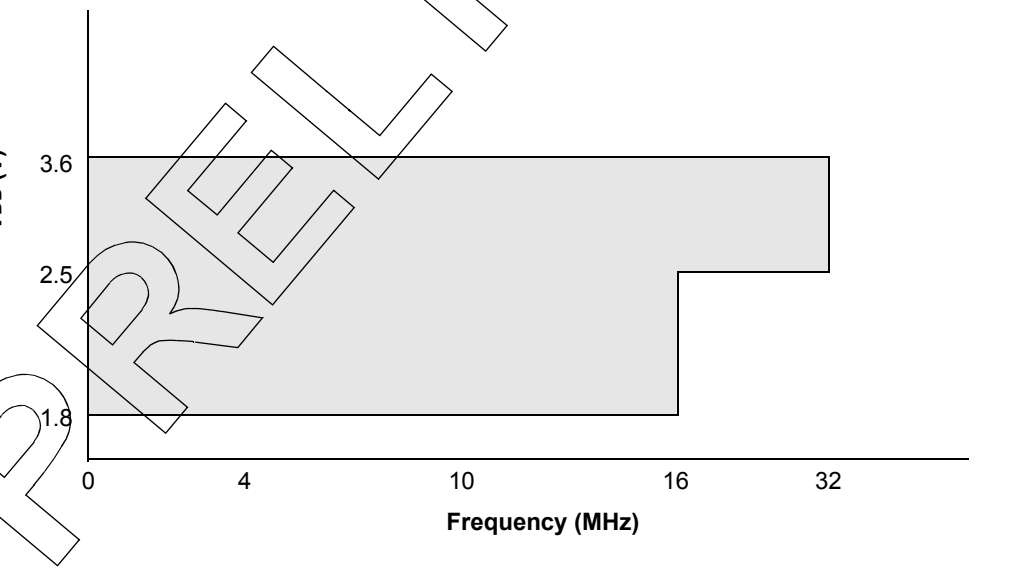
Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

FIGURE 39-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16F19155/56/75/76/85/86 ONLY



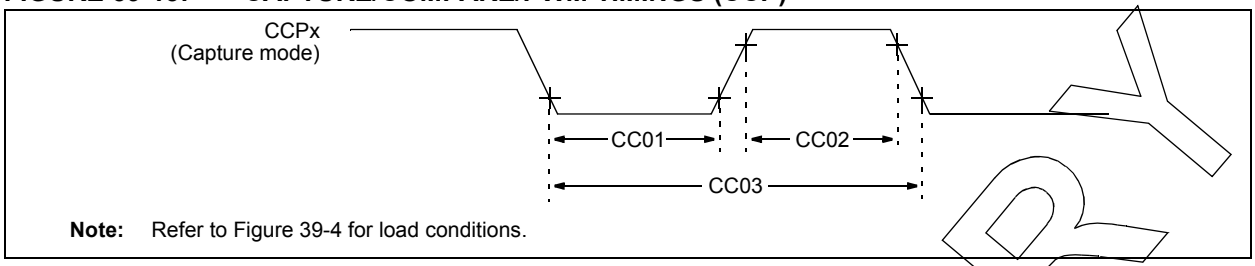
Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 39-7 for each Oscillator mode's supported frequencies.

FIGURE 39-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16(L)F19155/56/75/76/85/86 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 39-7 for each Oscillator mode's supported frequencies.

FIGURE 39-13: CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 39-4 for load conditions.

TABLE 39-20: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCPx Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCPx Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCPx Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value

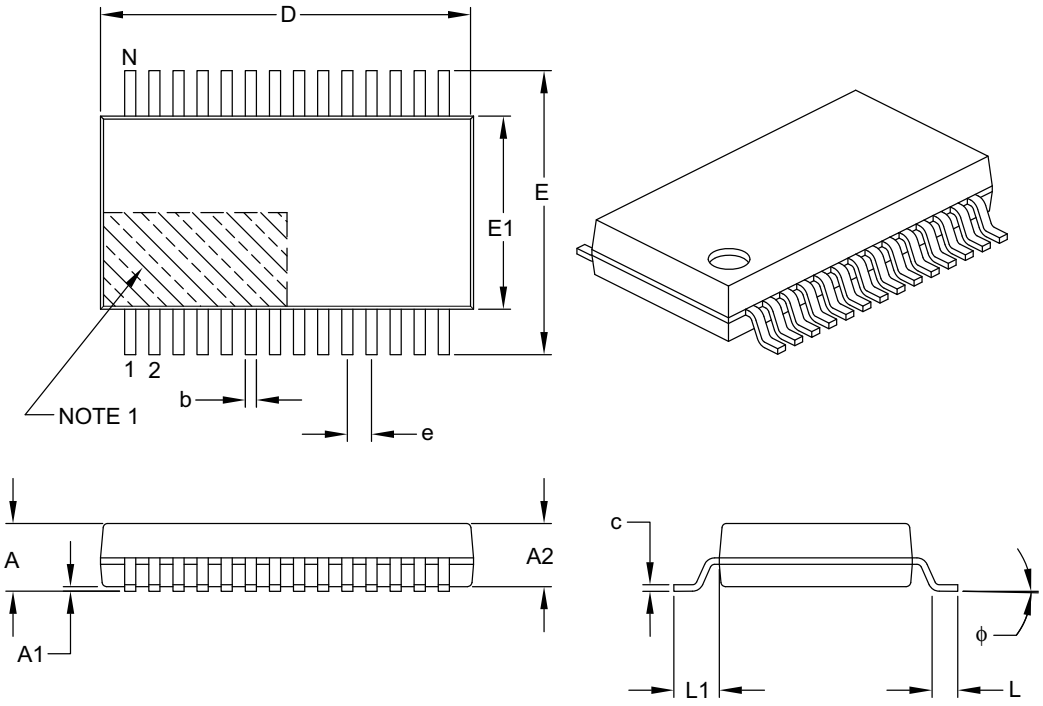
* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

The following sections give the technical details of the packages.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B