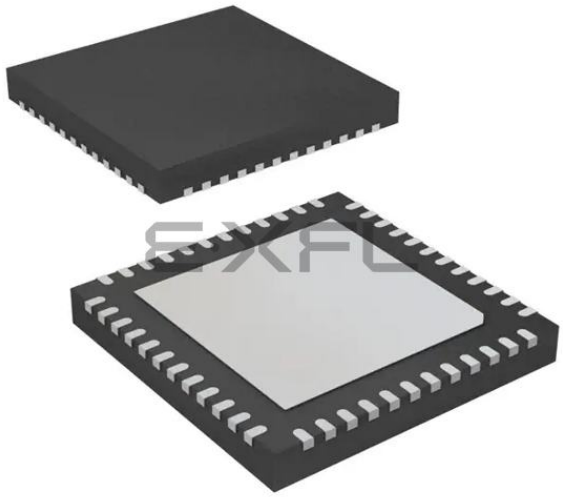

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 39x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf19186t-i-mv

TABLE 1: PIC16(L)F191XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (kW/KB)	DataEE (bytes)	Data SRAM (bytes)	I/O Pins	12-bit ADC (ch)	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer (WWDT)	CCP/10-bit PWM	CWG	CLC	Zero-Cross Detect	Temperature Indicator	Memory Access Partition	Device Information Area	EUSART/ I^2C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug(1)	LCD Segments (Max)	LCD Charge Pump/ Bias Generator
PIC16(L)F19155	**(A)**	8/14	256	1024	24	20	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	96	Y/Y
PIC16(L)F19156	**(A)**	16/28	256	2048	24	20	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	96	Y/Y
PIC16(L)F19175	**(A)**	8/14	256	1024	35	31	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	184	Y/Y
PIC16(L)F19176	**(A)**	16/28	256	2048	35	31	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	184	Y/Y
PIC16(L)F19185	**(A)**	8/14	256	1024	43	39	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	248	Y/Y
PIC16(L)F19186	**(A)**	16/28	256	2048	43	39	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	248	Y/Y
PIC16(L)F19195	**(B)**	8/14	256	1024	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y
PIC16(L)F19196	**(B)**	16/28	256	2048	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y
PIC16(L)F19197	**(B)**	32/56	256	4096	59	45	1	2	2	2	Y	2/2	1	4	Y	Y	Y	Y	2/1	Y	Y	I	360	Y/Y

Note 1: I – Debugging integrated on chip.

Data Sheet Index (Unshaded devices are described in this document):

A. Future Release PIC16(L)F19155/56/75/76/85/86 Data Sheet, 28/40/44/48-Pin

B. DS40001873 PIC16(L)F19195/6/7 Data Sheet, Full-Featured 64-Pin Microcontrollers

Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

TABLE 4-7: PIC16(L)F19155/56/75/76/85/86 MEMORY MAP, BANKS 8-15

	BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h	Core Registers (Table 4-3)	480h	Core Registers (Table 4-3)	500h	Core Registers (Table 4-3)	580h	Core Registers (Table 4-3)	600h	Core Registers (Table 4-3)	680h	Core Registers (Table 4-3)	700h	Core Registers (Table 4-3)	780h	Core Registers (Table 4-3)
40Ch	—	48Ch	SMT1TMRL	50Ch	—	58Ch	—	60Ch	CWG1CLKCON	68Ch	—	70Ch	PIR0	78Ch	—
40Dh	—	48Dh	SMT1TMRH	50Dh	—	58Dh	—	60Dh	CWG1ISM	68Dh	—	70Dh	PIR1	78Dh	—
40Eh	—	48Eh	SMT1TMRU	50Eh	—	58Eh	—	60Eh	CWG1DBR	68Eh	—	70Eh	PIR2	78Eh	—
40Fh	—	48Fh	SMT1CPRL	50Fh	—	58Fh	—	60Fh	CWG1DBF	68Fh	—	70Fh	PIR3	78Fh	—
410h	—	490h	SMT1CPRH	510h	—	590h	—	610h	CWG1CON0	690h	—	710h	PIR4	790h	—
411h	—	491h	SMT1CPRU	511h	—	591h	—	611h	CWG1CON1	691h	—	711h	PIR5	791h	—
412h	—	492h	SMT1CPWL	512h	—	592h	—	612h	CWG1AS0	692h	—	712h	PIR6	792h	—
413h	—	493h	SMT1CPWH	513h	—	593h	—	613h	CWG1AS1	693h	—	713h	PIR7	793h	—
414h	—	494h	SMT1CPWU	514h	—	594h	—	614h	CWG1STR	694h	—	714h	PIR8	794h	—
415h	—	495h	SMT1PRL	515h	—	595h	—	615h	—	695h	—	715h	—	795h	—
416h	—	496h	SMT1PRH	516h	—	596h	—	616h	—	696h	—	716h	PIE0	796h	PMD0
417h	—	497h	SMT1PRU	517h	—	597h	—	617h	—	697h	—	717h	PIE1	797h	PMD1
418h	—	498h	SMT1CON0	518h	—	598h	—	618h	—	698h	—	718h	PIE2	798h	PMD2
419h	—	499h	SMT1CON1	519h	—	599h	—	619h	—	699h	—	719h	PIE3	799h	PMD3
41Ah	—	49Ah	SMT1STAT	51Ah	—	59Ah	—	61Ah	—	69Ah	—	71Ah	PIE4	79Ah	PMD4
41Bh	—	49Bh	SMT1CLK	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	PIE5	79Bh	PMD5
41Ch	—	49Ch	SMT1SIG	51Ch	—	59Ch	TMR0L	61Ch	—	69Ch	—	71Ch	PIE6	79Ch	—
41Dh	—	49Dh	SMT1WIN	51Dh	—	59Dh	TMR0H	61Dh	—	69Dh	—	71Dh	PIE7	79Dh	—
41Eh	—	49Eh	—	51Eh	—	59Eh	T0CON0	61Eh	—	69Eh	—	71Eh	PIE8	79Eh	—
41Fh	—	49Fh	—	51Fh	—	59Fh	T0CON1	61Fh	—	69Fh	—	71Fh	—	79Fh	—
420h	General Purpose Register 80 Bytes	4A0h	General Purpose Register 80 Bytes	520h	General Purpose Register 80 Bytes	5A0h	General Purpose Register 80 Bytes	620h	General Purpose Register 48 Bytes	6A0h	General Purpose Register 80 Bytes(2)	720h	General Purpose Register 80 Bytes(2)	7A0h	General Purpose Register 80 Bytes(2)
46Fh		4EFh		56Fh		5EFh		64Fh		6EFh		76Fh		7EFh	
								650h	General Purpose Register 32 Bytes(2)						
470h	Common RAM Accesses	4F0h	Common RAM Accesses	570h	Common RAM Accesses	5F0h	Common RAM Accesses	670h	Common RAM Accesses	6F0h	Common RAM Accesses	770h	Common RAM Accesses	7F0h	Common RAM Accesses
47Fh	470h-47Fh	4FFh	4F0h-4FFh	57Fh	570h-57Fh	5FFh	5F0h-5FFh	67Fh	670h-67Fh	6FFh	6F0h-6FFh	77Fh	770h-77Fh	7FFh	7F0h-7FFh

Note 1: Unimplemented locations read as '0'.
2: Present only on PIC16(L)F19156/76/86.

4.6.1 TRADITIONAL/BANKED DATA MEMORY

The traditional or banked data memory is a region from FSR address 0x000 to FSR address 0x1FFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

FIGURE 4-10: TRADITIONAL/BANKED DATA MEMORY MAP

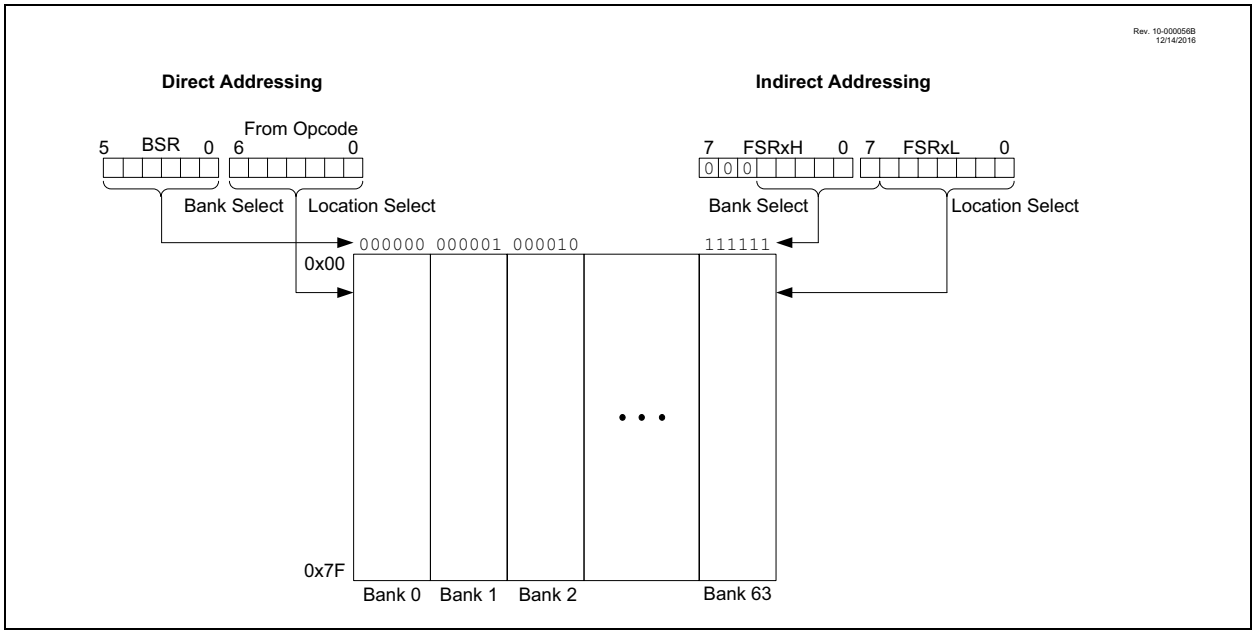


FIGURE 9-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM

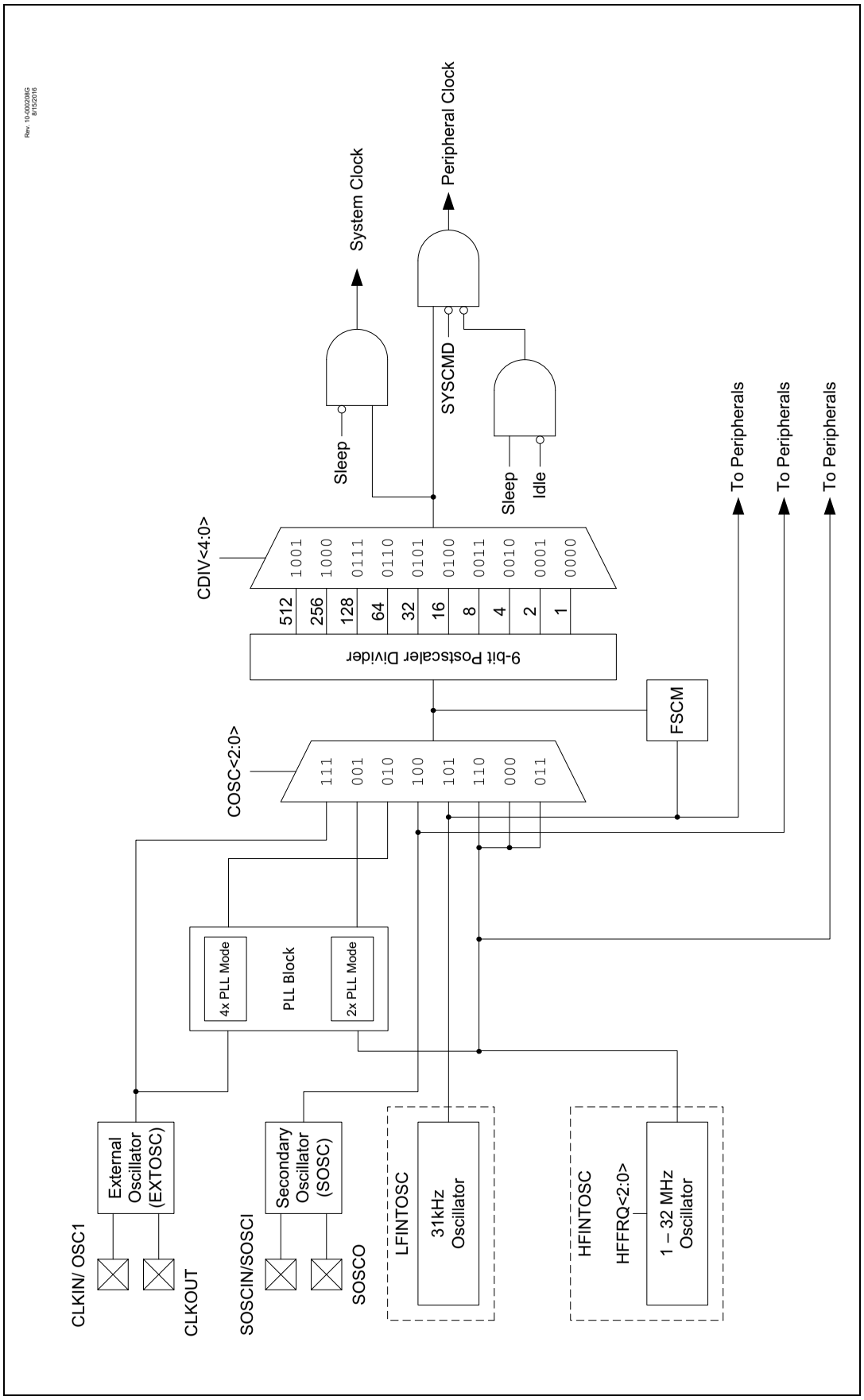
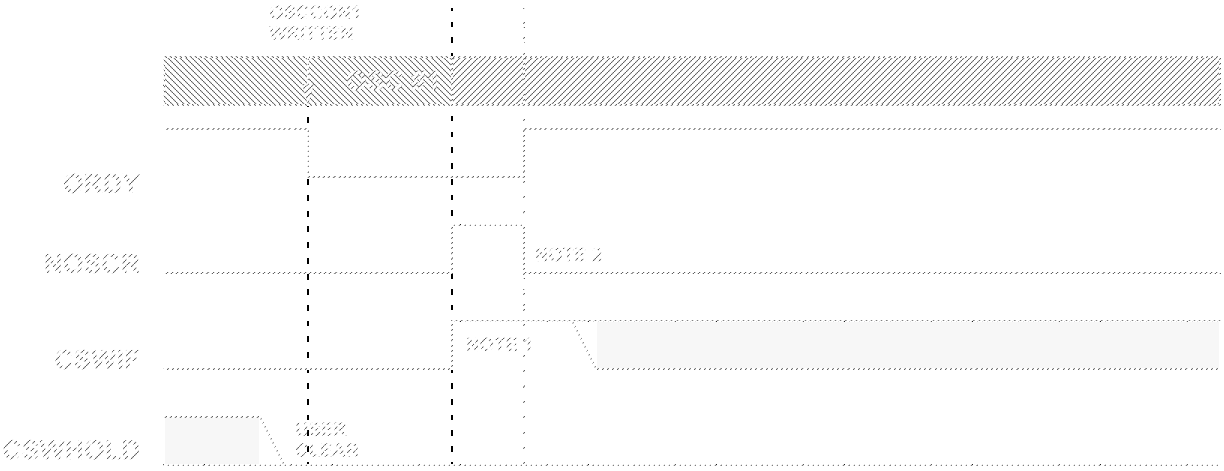
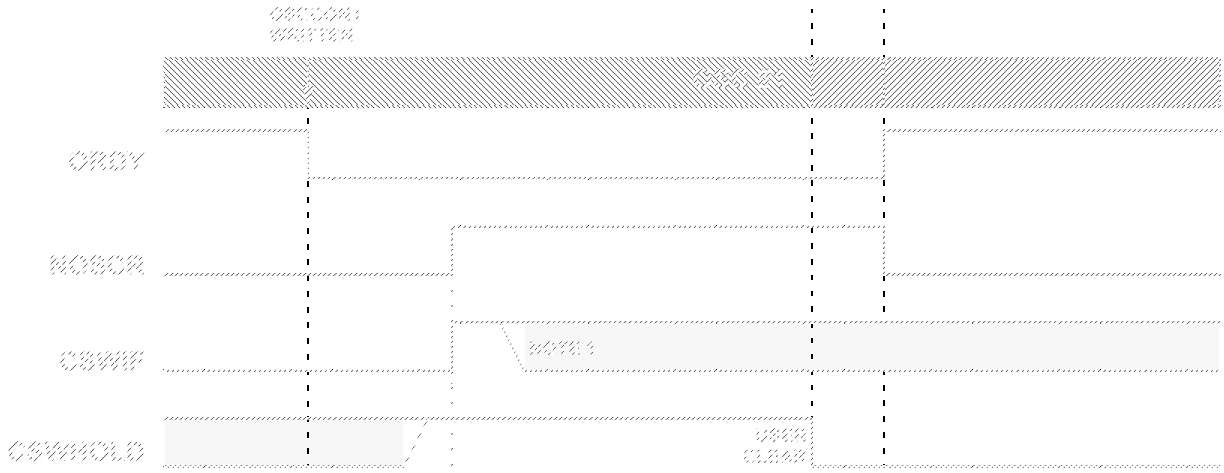


FIGURE 9-4: CLOCK SWITCH (CSWHOLD = 0)



Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 9-5: CLOCK SWITCH (CSWHOLD = 1)



Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

REGISTER 10-5: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **RC2IE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Enables the USART receive interrupt

bit 6 **TX2IE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 5 **RC1IE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Enables the USART receive interrupt

bit 4 **TX1IE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **BCL1IE:** MSSP1 Bus Collision Interrupt Enable bit
1 = MSSP bus collision interrupt enabled
0 = MSSP bus collision interrupt disabled

bit 0 **SSP1IE:** Synchronous Serial Port (MSSP1) Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by PIE1-PIE8.

REGISTER 10-11: PIR0: PERIPHERAL INTERRUPT STATUS REGISTER 0

U-0	U-0	R/W/HS-0/0	R-0	U-0	U-0	U-0	R/W/HS-0/0
—	—	TMR0IF	IOCIF	—	—	—	INTF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS= Hardware Set

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
- 1 = Timer0 register has overflowed (must be cleared in software)
- 0 = Timer0 register did not overflow

bit 4 **IOCIF:** Interrupt-on-Change Interrupt Flag bit (read-only)(2)
- 1 = One or more of the IOCAF-IOCEF register bits are currently set, indicating an enabled edge was detected by the IOC module.
- 0 = None of the IOCAF-IOCEF register bits are currently set

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **INTF:** INT External Interrupt Flag bit(1)
- 1 = The INT external interrupt occurred (must be cleared in software)
- 0 = The INT external interrupt did not occur

Note 1: The External Interrupt GPIO pin is selected by INTPPS (Register 15-1).

2: The IOCIF bit is the logical OR of all the IOCAF-IOCEF flags. Therefore, to clear the IOCIF flag, application firmware must clear all of the lower level IOCAF-IOCEF register bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	164
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	165
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	166
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	167
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	168
PIE4	—	—	—	—	TMR4IE	—	TMR2IE	TMR1IE	169
PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	170
PIE6	CRIE	—	—	—	—	—	CCP2IE	CCP1IE	171
PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	172
PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	173
PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	174
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	176
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	177
PIR4	—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF	178
PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	179
PIR6	CRIF	—	—	—	—	—	CCP2IF	CCP1IF	180
PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	181
PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	182

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

REGISTER 14-3: LATA: PORTA DATA LATCH REGISTER

R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATA7	LATA6	—	LATA4	LATA3	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **LATA<7:6>**: RA<7:6> Output Latch Value bits(1)

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **LATA<4:0>**: RA<4:0> Output Latch Value bits(1)

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 14-4: ANSELA: PORTA ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSA7	ANSA6	—	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **ANSA<7:6>**: Analog Select between Analog or Digital Function on pins RA<7:6>, respectively
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **ANSA<4:0>**: Analog Select between Analog or Digital Function on pins RA<4:0>, respectively
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 16-4: PMD3: PMD CONTROL REGISTER 3

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	PWM4MD	PWM3MD	CCP2MD	CCP1MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3 **PWM4MD:** Disable Pulse-Width Modulator PWM4 bit
1 = PWM4 module disabled
0 = PWM4 module enabled

bit 2 **PWM3MD:** Disable Pulse-Width Modulator PWM3 bit
1 = PWM3 module disabled
0 = PWM3 module enabled

bit 1 **CCP2MD:** Disable CCP2 bit
1 = CCP2 module disabled
0 = CCP2 module enabled

bit 0 **CCP1MD:** Disable CCP1 bit
1 = CCP1 module disabled
0 = CCP1 module enabled

REGISTER 19-11: ADACQL: ADC ACQUISITION TIME CONTROL REGISTER (LOW BYTE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACQ<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 ACQ<7:0>: Acquisition (charge share time) Select bits
See Table 19-6.

REGISTER 19-12: ADACQH: ADC ACQUISITION TIME CONTROL REGISTER (HIGH BYTE)

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	ACQ<12:8>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented**: Read as ‘0’

bit 4-0 ACQ<12:8>: Acquisition (charge share time) Select bits
See Table 19-6.

TABLE 19-5: ACQUISITION TIME

ADACQ	Acquisition time
1 1111 1111 1111	8191 clocks of the selected ADC clock
1 1111 1111 1110	8190 clocks of the selected ADC clock
1 1111 1111 1101	8189 clocks of the selected ADC clock
...	...
0 0000 0000 0010	2 clocks of the selected ADC clock
0 0000 0000 0001	1 clock of the selected ADC clock
0 0000 0000 0000	Not included in the data conversion cycle(1)

Note 1: If ADPRE is not equal to ‘0’, then ADACQ = b′0_0000_0000_0000 means Acquisition time is 8192 clocks of the selected ADC clock.

REGISTER 22-5: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
—	—	—	—	—	—	MC2OUT	MC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **MC2OUT:** Mirror Copy of C2OUT bit

bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

TABLE 22-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CMxCON0	ON	OUT	—	POL	—	—	HYS	SYNC	340
CMxCON1	—	—	—	—	—	—	INTP	INTN	341
CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	343
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		285
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	—	332
DAC1CON1	—	—	—	DAC1R<4:0>					332
INTCON	GIE	PEIE	—					INTEDG	164
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	167
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	176
CLCINxPPS	—	—	—	CLCIN0PPS<4:0>					264
T1GPPS	—	—	—	T1GPPS<4:0>					264

Legend: — = unimplemented location, read as ‘0’. Shaded cells are unused by the comparator module.

REGISTER 25-2: T0CON1: TIMER0 CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0CS<2:0>			T0ASYNC	T0CKPS<3:0>			
bit 7							bit 0

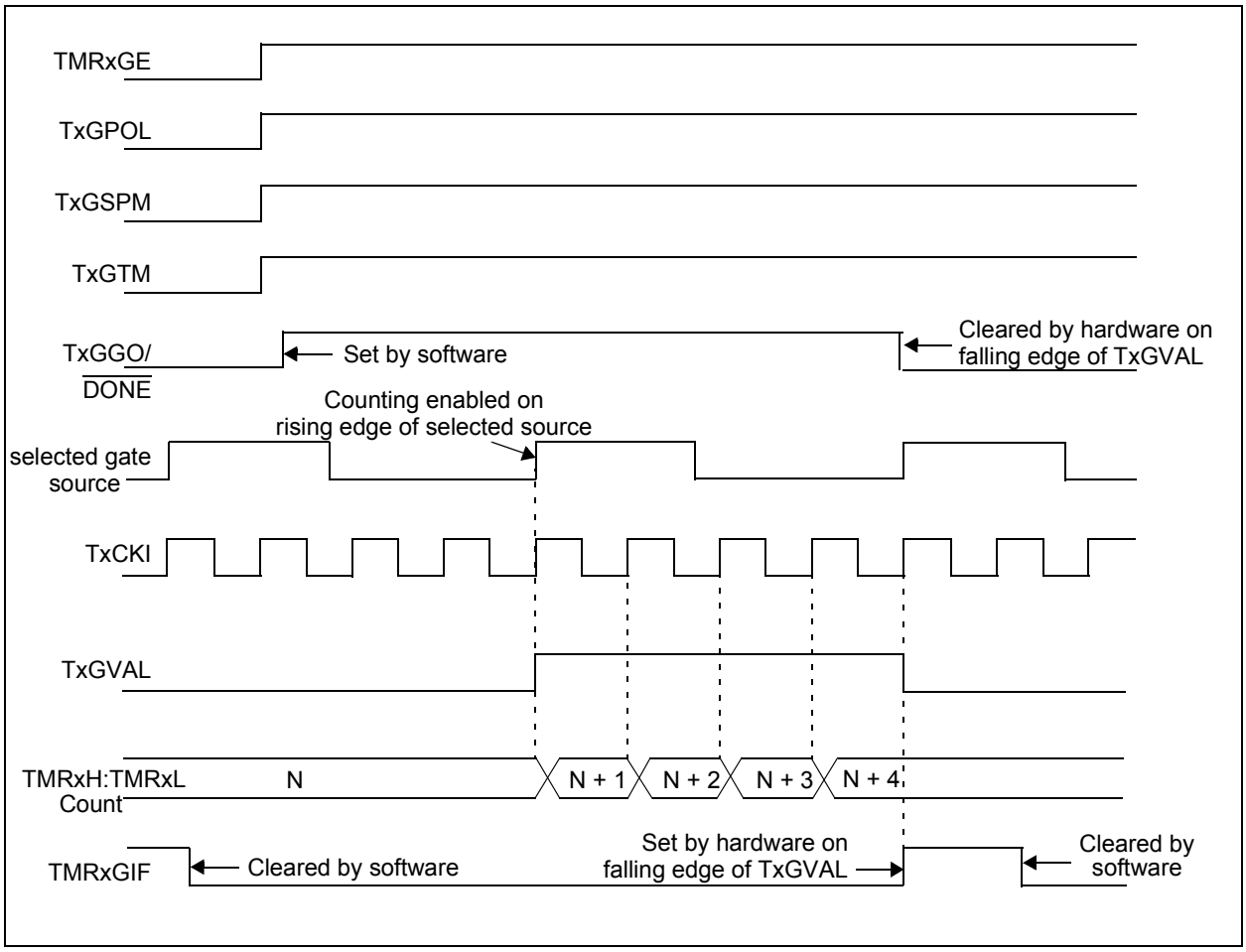
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **T0CS<2:0>:** Timer0 Clock Source select bits
111 = CLC1
110 = SOSC
101 = MFINTOSC (500 kHz)
100 = LFINTOSC
011 = HFINTOSC
010 = FOSC/4
001 = T0CKIPPS (Inverted)
000 = T0CKIPPS (True)

bit 4 **T0ASYNC:** TMR0 Input Asynchronization Enable bit
1 = The input to the TMR0 counter is not synchronized to system clocks
0 = The input to the TMR0 counter is synchronized to FOSC/4

bit 3-0 **T0CKPS<3:0>:** Prescaler Rate Select bit
1111 = 1:32768
1110 = 1:16384
1101 = 1:8192
1100 = 1:4096
1011 = 1:2048
1010 = 1:1024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

FIGURE 26-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



26.11 Peripheral Module Disable

When a peripheral module is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bit for Timer1 (TMR1MD) are in the PMD1 register. See **Section 16.0 "Peripheral Module Disable (PMD)"** for more information.

33.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 33-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPxBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPxSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPxBUF register as if a normal received byte (interrupts and Status bits appropriately set).

The clock polarity is selected by appropriately programming the CKP bit of the SSPxCON1 register and the CKE bit of the SSPxSTAT register. This then, would give waveforms for SPI communication as shown in Figure 33-6, Figure 33-8, Figure 33-9 and Figure 33-10, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 * TCY)
- FOSC/64 (or 16 * TCY)
- Timer2 output/2
- FOSC/(4 * (SSPxADD + 1))

If SMP = 0, it is necessary to select the SCK pin as an input using SCKPPS. The input and output PPS selectors must go to the same pin.

If SMP = 1 this is not required, and only the SCK output has to be routed; the input selection is ignored.

Figure 33-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPxBUF is loaded with the received data is shown.

FIGURE 33-6: SPI MODE WAVEFORM (MASTER MODE)

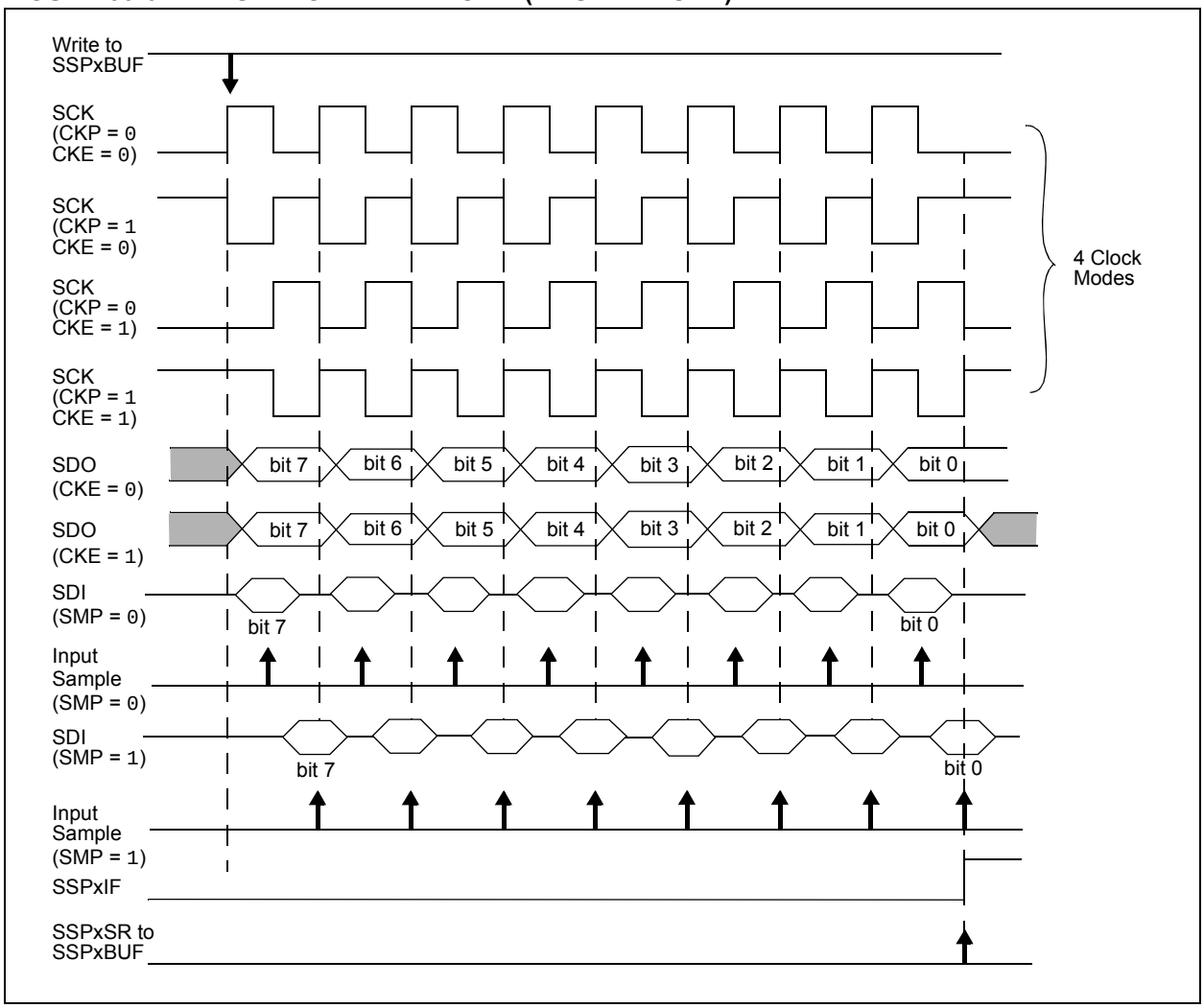


TABLE 34-3: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	FOSC/[64 (n+1)]
0	0	1	8-bit/Asynchronous	FOSC/[16 (n+1)]
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	FOSC/[4 (n+1)]
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPxBRGH, SPxBRGL register pair.

TABLE 34-4: BAUD RATE FOR ASYNCHRONOUS MODES

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	FOSC = 32.000 MHz			FOSC = 20.000 MHz			FOSC = 18.432 MHz			FOSC = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	1221	1.73	255	1200	0.00	239	1200	0.00	143
2400	2404	0.16	207	2404	0.16	129	2400	0.00	119	2400	0.00	71
9600	9615	0.16	51	9470	-1.36	32	9600	0.00	29	9600	0.00	17
10417	10417	0.00	47	10417	0.00	29	10286	-1.26	27	10165	-2.42	16
19.2k	19.23k	0.16	25	19.53k	1.73	15	19.20k	0.00	14	19.20k	0.00	8
57.6k	55.55k	-3.55	3	—	—	—	57.60k	0.00	7	57.60k	0.00	2
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	FOSC = 8.000 MHz			FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	300	0.16	207	300	0.00	191	300	0.16	51
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	—	—	—
9600	9615	0.16	12	—	—	—	9600	0.00	5	—	—	—
10417	10417	0.00	11	10417	0.00	5	—	—	—	—	—	—
19.2k	—	—	—	—	—	—	19.20k	0.00	2	—	—	—
57.6k	—	—	—	—	—	—	57.60k	0.00	0	—	—	—
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

35.8 LCD Multiplex Types

The LCD driver module can be configured into four multiplex types:

- Static (only COM0 used)
- 1/2 multiplex (COM0 and COM1 are used)
- 1/3 multiplex (COM0, COM1 and COM2 are used)
- 1/4 multiplex (COM0, COM1, COM2 and COM3 are used)
- 1/5 multiplex (COM0, COM1, COM2, COM3 and COM4 are used)
- 1/6 multiplex (COM0, COM1, COM2, COM3, COM4 and COM5 are used)
- 1/7 multiplex (COM0, COM1, COM2, COM3, COM4, COM5 and COM6 are used)
- 1/8 multiplex (COM0, COM1, COM2, COM3, COM4, COM5, COM6 and COM7 are used)

The LMUX<3:0> setting (LCDCON<3:0>) decides the function of the COM pins. (For details, see Table 35-8).

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

Note: On a Power-on Reset, the LMUX<3:0> bits are '0000'.

TABLE 35-8: COM<7:0> PIN FUNCTIONS

LMUX<3:0>	COM7 Pin	COM6 Pin	COM5 Pin	COM4 Pin	COM3 Pin	COM2 Pin	COM1 Pin	COM0 Pin
1000	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
0111	I/O Pin	COM6	COM5	COM4	COM3	COM2	COM1	COM0
0110	I/O Pin	I/O Pin	COM5	COM4	COM3	COM2	COM1	COM0
0101	I/O Pin	I/O Pin	I/O Pin	COM4	COM3	COM2	COM1	COM0
0100	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM3	COM2	COM1	COM0
0011	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM2	COM1	COM0
0010	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM1	COM0
0001	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM0
0000	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin

35.9 Segment Enables

The LCDSENx registers are used to select the pin function for each segment pin. The selection allows the designated SEG pins to be configured as LCD segment driver pins. To configure the pin as a segment pin, the corresponding bits in the LCDSENx registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSENx registers overrides any bit settings in the corresponding TRIS register.

Note:	On a Power-on Reset, these pins are configured as digital I/O.

35.10 Pixel Control

The LCDDATAx registers contain bits that define the state of each pixel. Each bit defines one unique pixel. Table 35-2 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

35.11 LCD Frame Frequency

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

TABLE 35-9: FRAME FREQUENCY FORMULAS

Multiplex	Frame Frequency =
Static ('0001')	Clock Source/(4 x 1 x (LP<3:0> + 1))
1/2 ('0010')	Clock Source/(2 x 2 x (LP<3:0> + 1))
1/3 ('0011')	Clock Source/(1 x 3 x (LP<3:0> + 1))
1/4 ('0100')	Clock Source/(1 x 4 x (LP<3:0> + 1))
1/5 ('0101')	Clock Source/(1 x 5 x (LP<3:0> + 1))
1/6 ('0110')	Clock Source/(1 x 6 x (LP<3:0> + 1))
1/7 ('0111')	Clock Source/(1 x 7 x (LP<3:0> + 1))
1/8 ('1000')	Clock Source/(1 x 8 x (LP<3:0> + 1))

Note: The clock source is SOSC/32 or LFINTOSC/32.

35.12 LCD Waveform Generation

LCD waveform generation is based on the theory that the net AC voltage across the dark pixel should be maximized and the net AC voltage across the clear pixel should be minimized. The net DC voltage across any pixel should be zero.

The COM signal represents the time slice for each common, while the SEG contains the pixel data.

The pixel signal (COM-SEG) will have no DC component and can take only one of the two rms values. The higher rms value will create a dark pixel and a lower rms value will create a clear pixel.

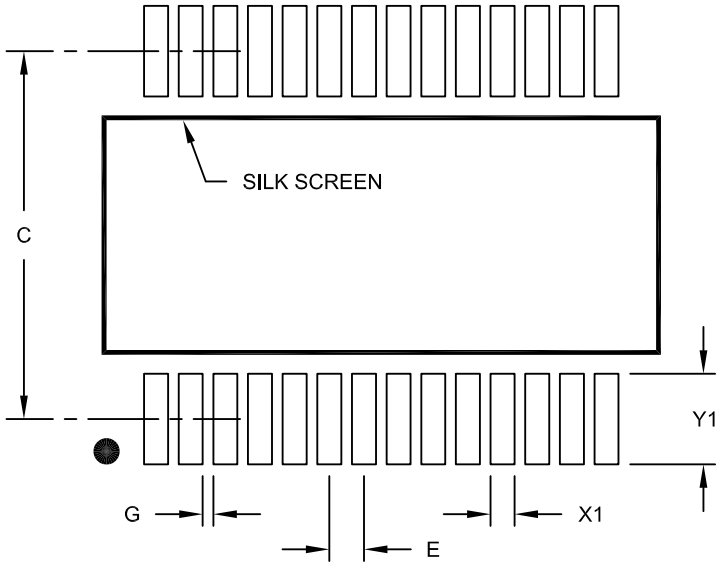
As the number of commons increases, the delta between the two rms values decreases. The delta represents the maximum contrast that the display can have.

The LCDs can be driven by two types of waveforms: Type-A and Type-B. In a Type-A waveform, the phase changes within each common type, whereas a Type-B waveform's phase changes on each frame boundary. Thus, Type-A waveforms maintain 0 VDC over a single frame, whereas Type-B waveforms take two frames.

Figure 35-8 through Figure 35-19 provide waveforms for static, half-multiplex, one-third multiplex and quarter multiplex drives for Type-A and Type-B waveforms.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

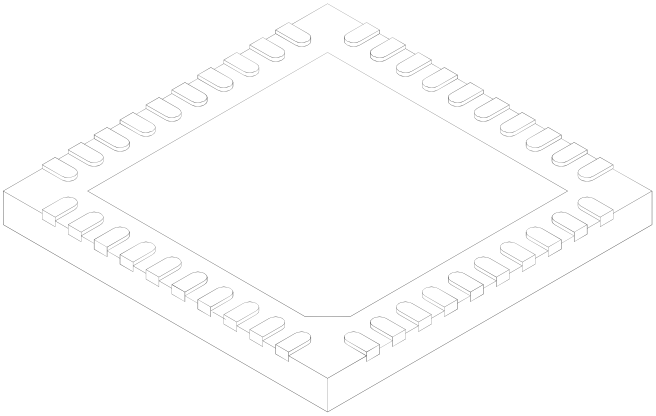
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2