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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | EBI/EMI, I²C, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 60 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e659a40fl |

## 6. Special Function Registers

The W79E659 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E659 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 6-1 Special Function Register Location Table

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| F8 | EIP | I2CON2 | I2ADDR20 | I2ADDR21 | I2DATA2 | I2STATUS2 | I2CLK2 | I2TIMER2 |
| F0 | B | | | | | | | |
| E8 | EIE | I2CON | I2ADDR10 | I2ADDR11 | I2DATA | I2STATUS | I2CLK | I2TIMER |
| E0 | ACC | | | | | | | |
| D8 | WDCON | PWMP | PWM0 | PWM1 | PWMCON1 | PWM2 | PWM3 | |
| D0 | PSW | | | | | | | WDCON2 |
| C8 | T2CON | T2MOD | RCAP2L | RCAP2H | TL2 | TH2 | PWMCON2 | PWM4 |
| C0 | ADDCON | ADCL | ADCH | PWM5 | PMR | STATUS | ADCPS | TA |
| B8 | IP | SADEN | | | | | | |
| B0 | P3 | P5 | P6 | P7 | | | | |
| A8 | IE | SADDR | | | SFRAL | SFRAH | SFRFD | SFRCN |
| A0 | P2 | XRAMAH | P4CSIN | | | P4 | | |
| 98 | SCON | SBUF | P42AL | P42AH | P43AL | P43AH | | CHPCON |
| 90 | P1 | | P4CONA | P4CONB | P40AL | P40AH | P41AL | P41AH |
| 88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | CKCON | |
| 80 | P0 | SP | DPL | DPH | | | | PCON |

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

Table 6-5 Special Function Registers, continued

| SYMBOL | DEFINITION | ADDRESS | MSB BIT_ADDRESS, SYMBOL LSB | | | | | | | | RESET |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SP | Stack Pointer | 81H | | | | | | | | | 0000 0111B |
| P0 | Port 0 | 80H | (87) | (86) | (85) | (84) | (83) | (82) | (81) | (80) | 1111 1111B |

**Note:** In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.

## PORT 0

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P0.7 | P0.6 | P0.5 | P0.4 | P0.3 | P0.2 | P0.1 | P0.0 |

Mnemonic: P0 Address: 80h

Port 0 is bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters. This port also provides a multiplexed, low-order address/data bus when the W79E659 accesses external memory.

## STACK POINTER

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SP.7 | SP.6 | SP.5 | SP.4 | SP.3 | SP.2 | SP.1 | SP.0 |

Mnemonic: SP Address: 81h

The Stack Pointer stores the address in Scratchpad RAM where the stack begins. It always points to the top of the stack.

## DATA POINTER LOW

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DPL.7 | DPL.6 | DPL.5 | DPL.4 | DPL.3 | DPL.2 | DPL.1 | DPL.0 |

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8051/52, 16-bit data pointer.

## DATA POINTER HIGH

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DPH.7 | DPH.6 | DPH.5 | DPH.4 | DPH.3 | DPH.2 | DPH.1 | DPH.0 |

Mnemonic: DPH Address: 83h

This is the low byte of the standard-8051/52, 16-bit data pointer.

## POWER CONTROL

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SMOD | SMOD0 | - | - | GF1 | GF0 | PD | IDL |

Mnemonic: PCON Address: 87h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | SMOD | 1: This bit doubles the serial-port baud rate in modes 1, 2 and 3. |
| 6 | SMOD0 | 0: Disable Framing Error Detection. SCON.7 acts as per the standard 8051/52 function.<br>1: Enable Framing Error Detection. SCON.7 indicates a Frame Error and acts as the FE flag. |
| 5-4 | - | Reserved |
| 3 | GF1 | General-purpose user flag. |
| 2 | GF0 | General-purpose user flag. |
| 1 | PD | 1: Go into POWER DOWN mode. In this mode, all clocks and program execution are stopped. |
| 0 | IDL | 1: Go into IDLE mode. In this mode, the CPU clock stops, so program execution stops too. However, the clock to the serial port, ADC, PWM timer and interrupt blocks does not stop, so these blocks continue operating. |

## TIMER CONTROL

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |

Mnemonic: TCON Address: 88h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | TF1 | Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit. |
| 6 | TR1 | Timer 1 run control: This bit turns the Timer 1 on or off by setting TR1 to 1 or 0. |
| 5 | TF0 | Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit. |
| 4 | TR0 | Timer 0 run control: This bit turns Timer 0 on or off by setting TR0 to 1 or 0. |
| 3 | IE1 | Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT1}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin. |
| 2 | IT1 | Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{INT1}$. |
| 1 | IE0 | Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT0}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin. |
| 0 | IT0 | Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{INT0}$. |

| | ALTERNATE FUNCTION1 | ALTERNATE FUNCTION2 | ALTERNATE FUNCTION3 |
|---|---|---|---|
| P1.0 | T2: External input for Timer/Counter 2 | PWM0: PWM output ch0 | - |
| P1.1 | T2EX: Timer/Counter 2 Capture/Reload Trigger | PWM1: PWM output ch1 | - |
| P1.2 | STADC: External rising edge input to start ADC | PWM2: PWM output ch2 | - |
| P1.3 | - | PWM3: PWM output ch3 | - |
| P1.4 | - | PWM4: PWM output ch4 | ADC0: Analog input0 |
| P1.5 | - | PWM5: PWM output ch5 | ADC1: Analog input1 |
| P1.6 | - | - | ADC2: Analog input2 |
| P1.7 | - | - | ADC3: Analog input3 |

### Port 4 Control Register A

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P41M1 | P41M0 | P41C1 | P41C0 | P40M1 | P40M0 | P40C1 | P40C0 |

Mnemonic: P4CONA Address: 92h

### Port 4 Control Register B

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P43M1 | P43M0 | P43C1 | P43C0 | P42M1 | P42M0 | P42C1 | P42C0 |

Mnemonic: P4CONB Address: 93h

| BIT NAME | FUNCTION |
|---|---|
| P4xM1, P4xM0 | Port 4 alternate modes.<br>=00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1.<br>=01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0.<br>=10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0.<br>=11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0 |
| P4xC1, P4xC0 | Port 4 Chip-select Mode address comparison:<br>=00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL.<br>=01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL.<br>=10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL.<br>=11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL. |

### PORT 2

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P2.7 | P2.6 | P2.5 | P2.4 | P2.3 | P2.2 | P2.1 | P2.0 |

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-up resistors. This port also provides the upper address bits for accesses to external memory.

### Port 4 Chip-select Polarity

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P43INV | P42INV | P42INV | P40INV | - | PWDNH | RMWFP | - |

Mnemonic: P4CSIN Address: A2h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7-4 | P4xINV | The Active Polarity of P4.x as P4.x is set as a chip-select strobe output.<br>1: Active High.<br>0: Active Low. |
| 3 | - | Reserved |
| 2 | PWDNH | Set ALE and $\overline{PSEN}$ state in power down mode.<br>1: ALE and $\overline{PSEN}$ output logic high in power down mode<br>0: ALE and $\overline{PSEN}$ output logic low in power down mode. |
| 1 | RMWFP | Control Read Path of Instruction “Read-Modify-Write”. When this bit is set, the read path of executing “read-modify-write” instruction is from port pin otherwise from SFR. |
| 0 | - | Reserved |

### PORT 4

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | P4.3 | P4.2 | P4.1 | P4.0 |

Mnemonic: P4 Address: A5h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

### Interrupt Enable

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | EA | EADC | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

Mnemonic: IE Address: A8h

**RS1, RS0: Register Bank select bits:**

| RS1 | RS0 | REGISTER BANK | ADDRESS |
|---|---|---|---|
| 0 | 0 | 0 | 00-07h |
| 0 | 1 | 1 | 08-0Fh |
| 1 | 0 | 2 | 10-17h |
| 1 | 1 | 3 | 18-1Fh |

## WATCHDOG CONTROL 2

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | - | - | STRLD |

Mnemonic: WDCON2 Address: D7h

STRLD Set this bit, CPU will re-start from LD Flash EPROM after watchdog reset. Clear this bit, CPU will re-start from AP Flash EPROM after watchdog reset. This register is protected by timer access (TA) register.

## WATCHDOG CONTROL

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | POR | - | - | WDIF | WTRF | EWT | RWT |

Mnemonic: WDCON Address: D8h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | - | Reserved. |
| 6 | POR | Power-on reset flag. The hardware sets this flag during power–up, and it can only be cleared by software. This flag can also be written by software. |
| 5-4 | - | Reserved. |
| 3 | WDIF | Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software. |
| 2 | WTRF | Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset. |
| 1 | EWT | Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function. |
| 0 | RWT | Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware. |

The WDCON register is affected differently by different kinds of resets. After an external reset, the WDCON register is set to 0x0x0xx0b. After a Watchdog Timer reset, WTRF is set to 1, and the other bits are unaffected. On a power-on/-down reset, WTRF and EWT are set to 0, and POR is set to 1.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT are protected bits, so programs must follow the Timed Access procedure to write them. (See the TA Register description for more information.) This is illustrated in the following example.

```
TA      EG    C7H
WDCON   REG   D8H
CKCON   REG   8EH
              MOV   TA, #AAH
              MOV   TA, #55H
              SETB  WDCON.0              ; Reset Watchdog Timer
              ORL   CKCON, #11000000B    ; Select 26 bits Watchdog Timer
              MOV   TA, #AAH
              MOV   TA, #55H
              ORL   WDCON, #00000010B    ; Enable watchdog
```

The other bits in WDCON have unrestricted write access.

### PWM Pre-scale Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | - | - | - |

Mnemonic: PWMP Address: D9h

PWMP.7-0 Adjust PWM frequency. $Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$

### PWM0

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | - | - | - |

Mnemonic: PWM0 Address: DAh

PWM0.7-0 Adjust PWM0 duty cycle. $PWMn\ high/low\ ratio\ of\ PWMn = \frac{PWMn}{255 - (PWMn)}$

### PWM1

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | - | - | - |

Mnemonic: PWM1 Address: DBh

PWM1.7-0 Adjust PWM1 duty cycle.

### PWM Control Register1

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PWM3OE | PWM2OE | ENPWM3 | ENPWM2 | PWM1OE | PWM0OE | ENPWM1 | ENPWM0 |

Mnemonic: PWMCON1 Address: DCh

### I2C Timer Counter Register Channel 1

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | ENTI | DIV4 | TIF |

Mnemonic: I2TIMER Address: EFh

ENTI Enable I2C 14-bits Time-out Counter. Setting ENTI to logic high will firstly reset the time-out counter and then start up counting. Clearing ENTI disables the 14-bit time-out counter. ENTI can be set to logic high only when SI=0.

DIV4 I2C Time-out Counter Clock Frequency Selection. DIV4 = 0 the clock frequency is coherent to the system clock Fosc. DIV4 = 1 the clock frequency is Fosc/4.

TIF I2C Time-out Flag. When the time-out counter overflows hardware will set this flag and request the I2C1 interrupt if I2C1 interrupt is enabled (EI2C1=1). This bit must be cleared by software.

### B REGISTER

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | B.7 | B.6 | B.5 | B.4 | B.3 | B.2 | B.1 | B.0 |

Mnemonic: B Address: F0h

B.7-0 The B register is the standard 8051/52 register that serves as a second accumulator

### EXTENDED INTERRUPT PRIORITY

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | PWDI | - | - | PI2C2 | PI2C1 |

Mnemonic: EIP Address: F8h

PWDI Watchdog Timer Interrupt priority.

PI2C2 I2C Channel 2 Interrupt priority.

PI2C1 I2C Channel 1 Interrupt priority.

### I2C Control Register Channel 2

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | ENS2 | STA | STO | SI | AA | - | PSEL2 |

Mnemonic: I2CON2 Address: F9h

ENS2 Enable channel 2 of I2C serial function block. When ENS2=1 the channel 2 of I2C serial function enables. The port latches of SDA2 and SCL2 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode.

SI I2C Port 2 Interrupt Flag. When a new SIO2 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C2 bits are both set, the I2C2 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is

## 7. Instruction Set

The W79E659 executes all the instructions of the standard 8051/52 family. The operations of these instructions, as well as their effect on flag and status bits, are exactly the same. However, the timing of these instructions is different in two ways. First, the W79E659 machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Second, the W79E659 can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can twice per machine cycle (i.e., six clocks per fetch).

The timing difference creates an advantage for the W79E659. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E659 reduces the number of dummy fetches and wasted cycles and improves overall efficiency, compared to the standard 8051/52.

Table 7-1 Instruction Set for W79E659

| OP-CODE | HEX CODE | BYTES | W79E659 MACHINE CYCLE | W79E659 CLOCK CYCLES | 8032 CLOCK CYCLES | W79E659 VS. 8032 SPEED RATIO |
|---|---|---|---|---|---|---|
| NOP | 00 | 1 | 1 | 4 | 12 | 3 |
| ADD A, R0 | 28 | 1 | 1 | 4 | 12 | 3 |
| ADD A, R1 | 29 | 1 | 1 | 4 | 12 | 3 |
| ADD A, R2 | 2A | 1 | 1 | 4 | 12 | 3 |
| ADD A, R3 | 2B | 1 | 1 | 4 | 12 | 3 |
| ADD A, R4 | 2C | 1 | 1 | 4 | 12 | 3 |
| ADD A, R5 | 2D | 1 | 1 | 4 | 12 | 3 |
| ADD A, R6 | 2E | 1 | 1 | 4 | 12 | 3 |
| ADD A, R7 | 2F | 1 | 1 | 4 | 12 | 3 |
| ADD A, @R0 | 26 | 1 | 1 | 4 | 12 | 3 |
| ADD A, @R1 | 27 | 1 | 1 | 4 | 12 | 3 |
| ADD A, direct | 25 | 2 | 2 | 8 | 12 | 1.5 |
| ADD A, #data | 24 | 2 | 2 | 8 | 12 | 1.5 |
| ADDC A, R0 | 38 | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R1 | 39 | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R2 | 3A | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R3 | 3B | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R4 | 3C | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R5 | 3D | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R6 | 3E | 1 | 1 | 4 | 12 | 3 |
| ADDC A, R7 | 3F | 1 | 1 | 4 | 12 | 3 |
| ADDC A, @R0 | 36 | 1 | 1 | 4 | 12 | 3 |
| ADDC A, @R1 | 37 | 1 | 1 | 4 | 12 | 3 |

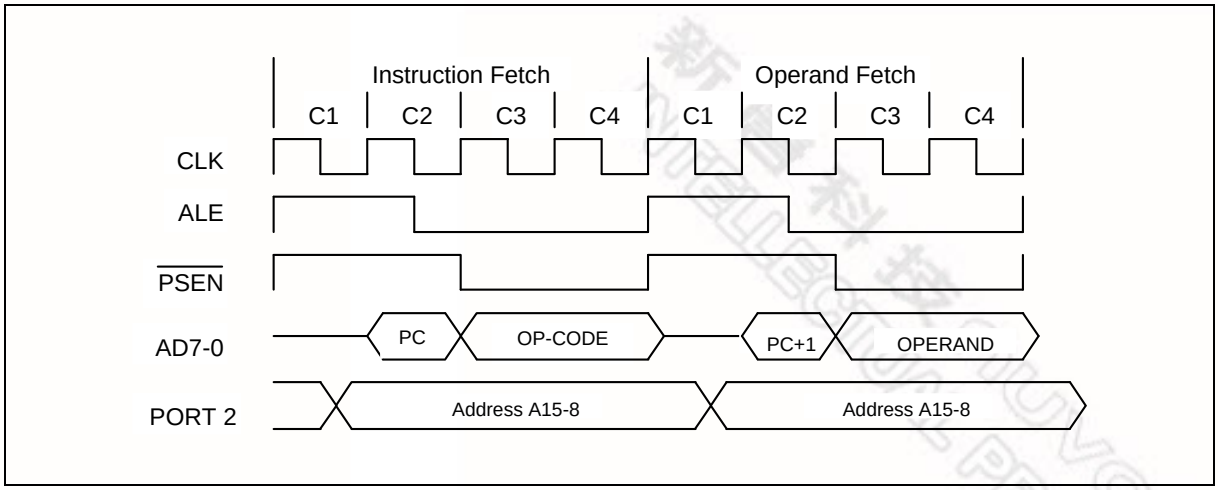



Figure 7-2 Two Cycle Instruction Timing

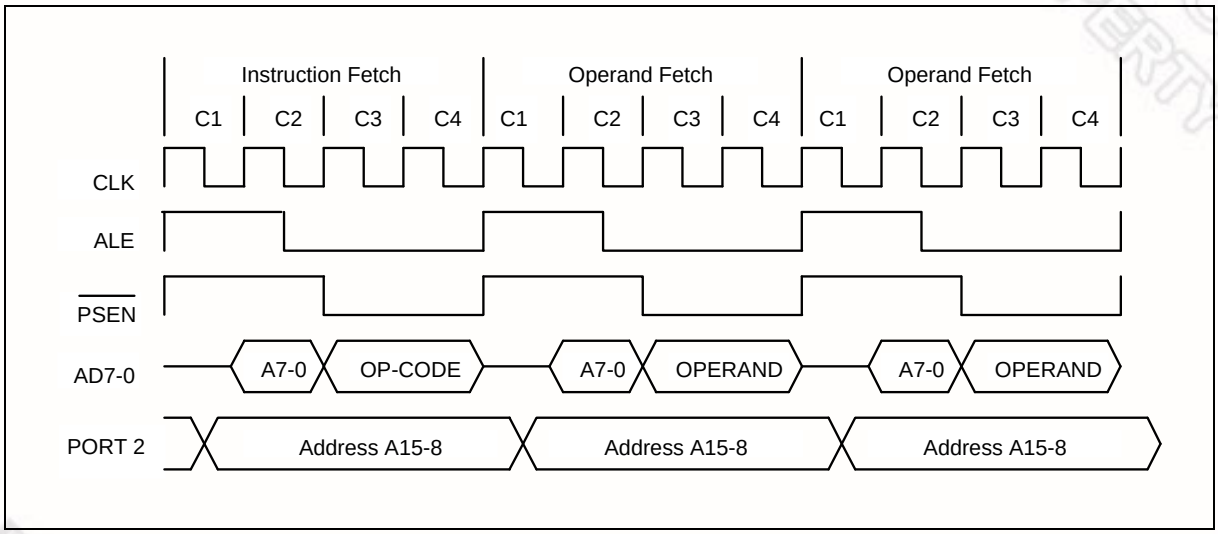



Figure 7-3 Three Cycle Instruction Timing

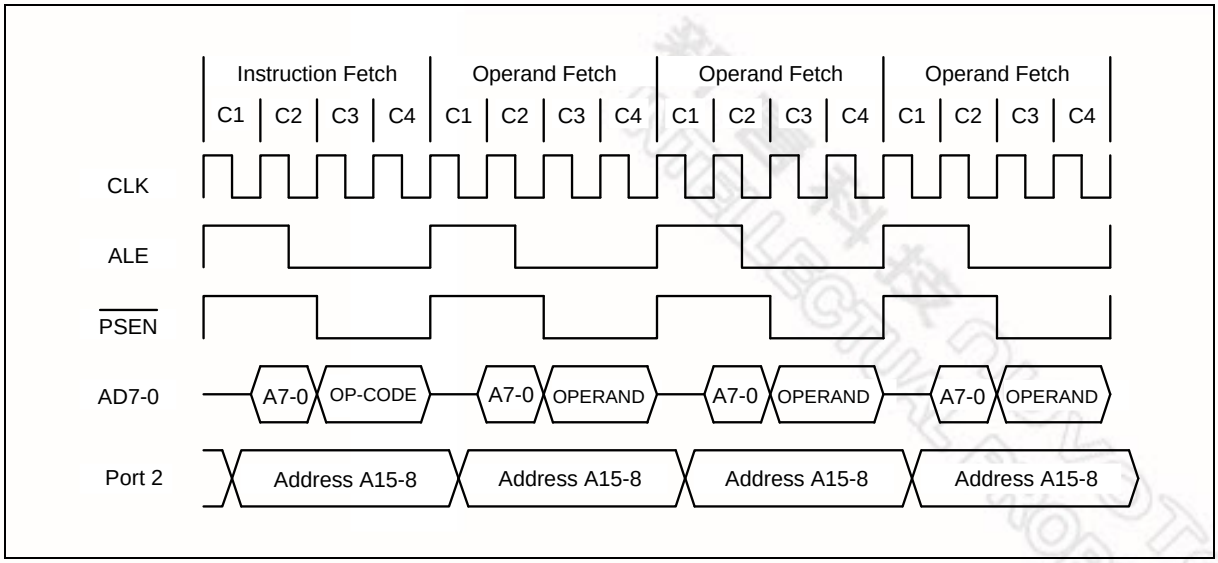



Figure 7-4 Four Cycle Instruction Timing

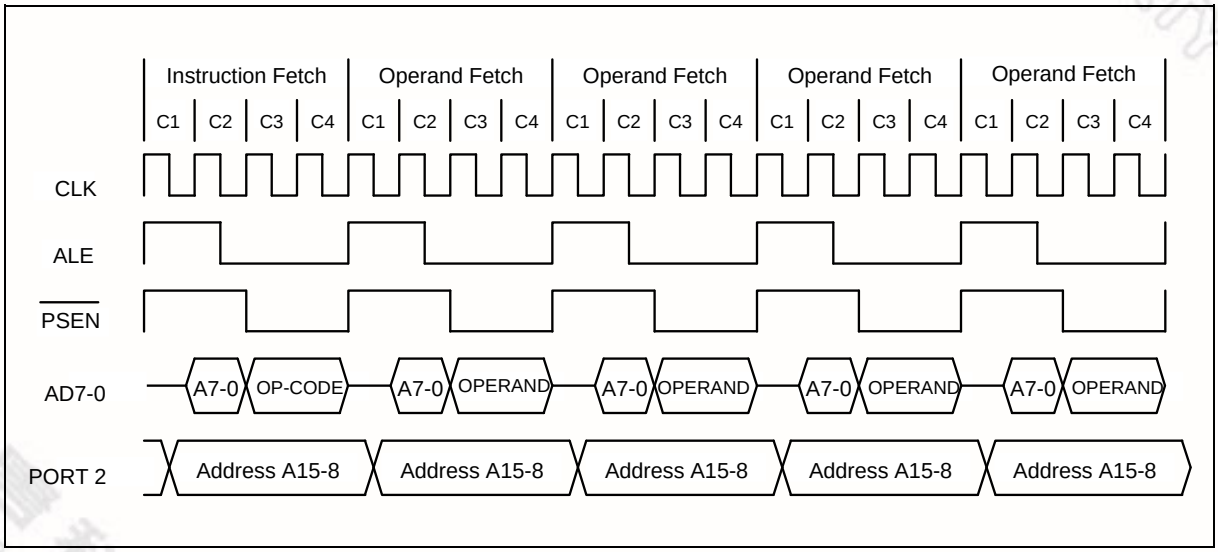



Figure 7-5 Five Cycle Instruction Timing

### 7.1.1 External Data Memory Access Timing

The timing for the MOVX instruction is another feature of the W79E659. In the standard 8051/52, the MOVX instruction has a fixed execution time of 2 machine cycles. However, in the W79E659, the duration of the access can be controlled by the user.

The instruction starts off as a normal op-code fetch that takes four clocks. In the next machine cycle, the W79E659 puts out the external memory address, and the actual access occurs. The user can control the duration of this access by setting the stretch value in CKCON, bits 2 – 0. As shown in the table below, these three bits can range from zero to seven, resulting in MOVX instructions that take

two to nine machine cycles. The default value is one, resulting in a MOVX instruction of three machine cycles.

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

Table 7-2 Data Memory Cycle Stretch Values

| M2 | M1 | M0 | MACHINE CYCLES | $\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS | $\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 25 MHZ | $\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 40 MHZ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 2 | 2 | 80 nS | 50 nS |
| 0 | 0 | 1 | 3 (default) | 4 | 160 nS | 100 nS |
| 0 | 1 | 0 | 4 | 8 | 320 nS | 200 nS |
| 0 | 1 | 1 | 5 | 12 | 480 nS | 300 nS |
| 1 | 0 | 0 | 6 | 16 | 640 nS | 400 nS |
| 1 | 0 | 1 | 7 | 20 | 800 nS | 500 nS |
| 1 | 1 | 0 | 8 | 24 | 960 nS | 600 nS |
| 1 | 1 | 1 | 9 | 28 | 1120 nS | 700 nS |

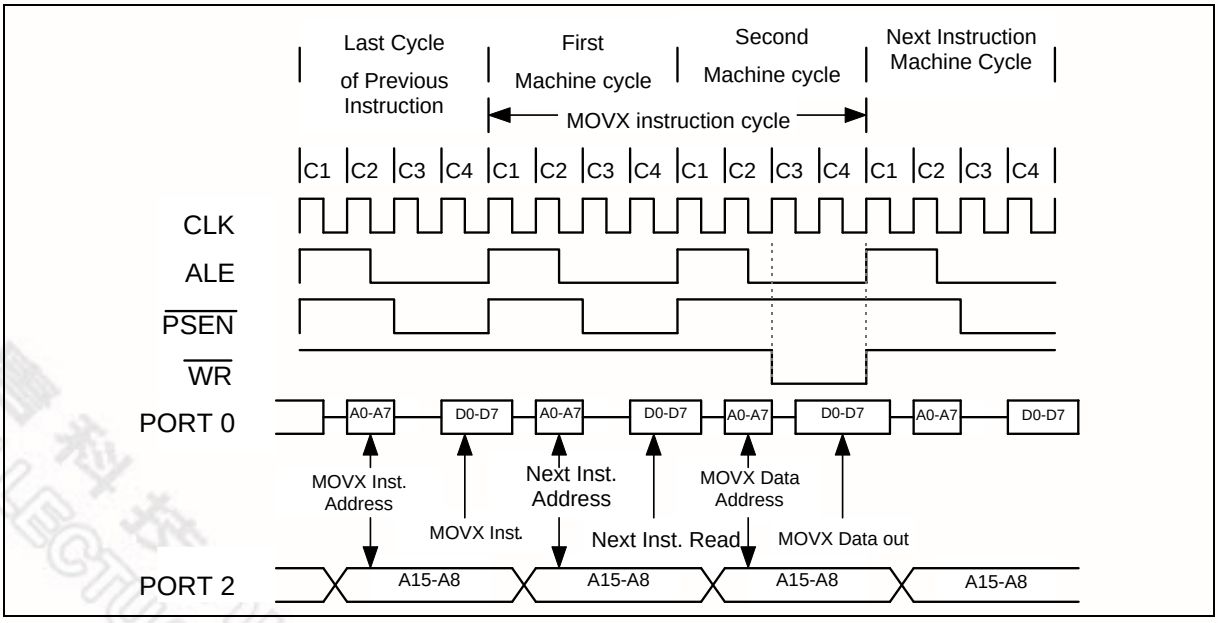



Figure 7-6 Data Memory Write with Stretch Value = 0

## 8. Power Management

The W79E659 provides idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

### 8.1 Idle Mode

Write a one to bit 0 in PCON at 87h to put the device in Idle mode. The instruction that sets the idle bit is the last instruction executed before the device goes into Idle mode. In Idle mode, the clock to the CPU is halted, but not the one to the Interrupt, Timer, Watchdog Timer, PWM, ADC, UART and I2C ports. This freezes the CPU state, including the Program Counter, Stack Pointer, Program Status Word, Accumulator and registers. The ALE and $\overline{\text{PSEN}}$ pins are held high, and port pins hold the same states they had when the device went into Idle mode. Table 8-1 below provides the values of various pins in Idle mode.

Idle mode can be terminated two ways. First, since the interrupt controller is still active, any enabled interrupt wakes up the processor. This automatically clears the Idle bit, terminates Idle mode, and executes the Interrupt Service Routine (ISR). After the ISR, the program resumes after the instruction that put the device into Idle mode.

Idle mode can also be exited by a reset, such as a high signal on the external RST pin, a power-on reset or a Watchdog Timer reset (if enabled). During reset, the program counter is reset to 0000h, so the instruction following the one that put the device into Idle mode is not executed. All the SFRs are also reset to their default values. Since the clock is already running, there is no delay, and execution starts immediately.

### 8.2 Power Down Mode

Write a one to bit 1 in PCON register at 87h to put the device in Power-Down mode. The instruction that sets the power-down bit is the last instruction executed before the device goes into Power-Down mode. In Power-Down mode, all the clocks and all activity stop completely, and power consumption is reduced to the lowest possible value. The ALE and $\overline{\text{PSEN}}$ pins are pulled low, and port pins output the values held by their respective registers. Table 8-1 provides the values of various pins in Power-Down mode.

The W79E659 can exit Power-Down mode two ways. First, it can be exited by a reset, such as a high signal on the external RST pin or a power-on reset. The Watchdog Timer cannot provide a reset to exit Power-Down mode because the clock has stopped. A reset terminates Power-Down mode, restarts the clock, and restarts program execution at 0000h.

The W79E659 can also exit Power-Down mode by an external interrupt pin, as long as the external input has been set to low level or falling edge detect, the corresponding interrupt is enabled, and the global enable (EA) bit is set. If these conditions are met, then a low-level or falling-edge signal on the external INT pin re-starts the oscillator. The device executes the interrupt service routine (ISR) for the corresponding external interrupt, and, afterwards, the program resumes execution after the one that put the device into Power-Down mode.

Table 8-1 Status of external pins during Idle and Power Down

| MODE | PROGRAM MEMORY | ALE | $\overline{\text{PSEN}}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |

### 11.2.4 Baud Rate Generator Mode

Baud rate generator mode is enabled by setting either RCLK or TCLK in T2CON. In baud rate generator mode, Timer/Counter 2 is a 16-bit counter with auto-reload when the count rolls over from FFFFh. However, rolling-over does not set TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in the T2CON register and causes an interrupt request.

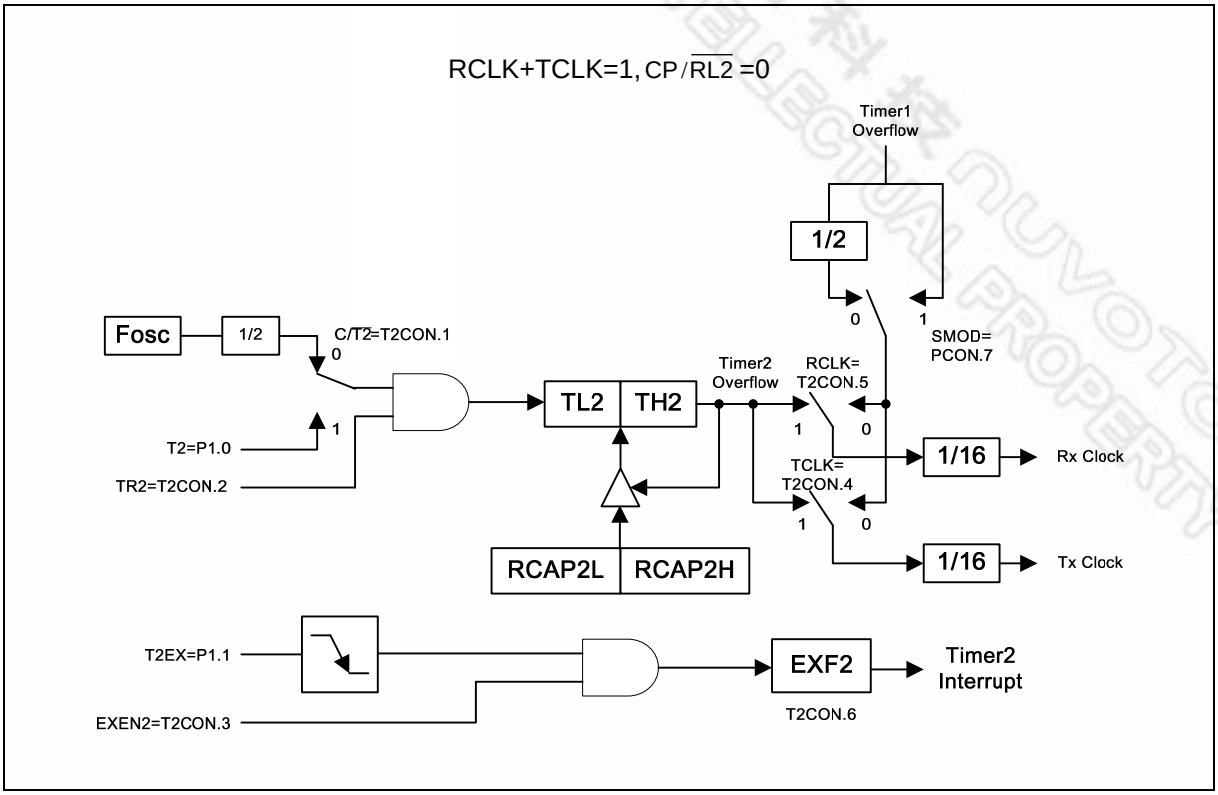



Figure 11-7 Baud Rate Generator Mode

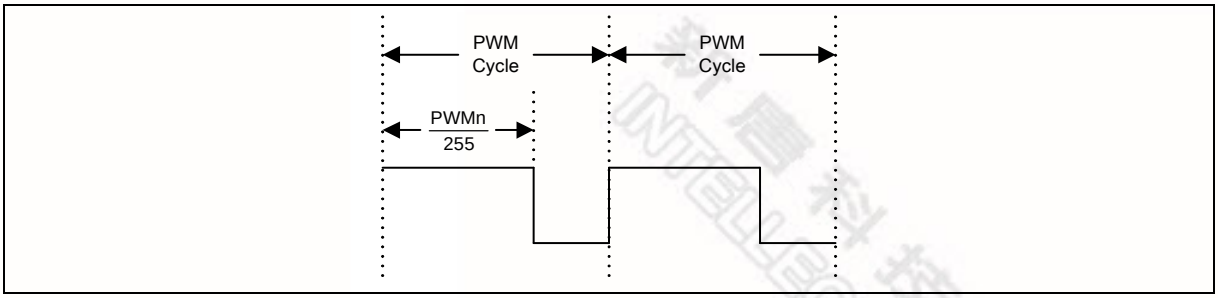



Figure 13-2 PWM Duty Ratio

If register PWM*n* is loaded with a new value, the associated output is updated immediately. By loading PWM*n* with 00H or FFH, the corresponding channel provides a constant high or low level output, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach FFh, so the output remains low all the time.

Buffered PWM outputs may be used to drive DC motors. In this case, the rotation speed of the motor is proportional to the contents of PWM*n*. The repetition frequency Fpwm for channel *n* is given by:

$$Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$$

Prescale division factor = PWM + 1

$$\text{PWMn high/low ratio of PWMn} = \frac{(PWMn)}{255 - (PWMn)}$$

This gives a repetition frequency range of 123 Hz to 31.4 KHz ( $f_{osc}$ = 16 MHz).

Please refer as below code.

```
mov    pwmcon1, #00110011b          ; enable pwm3, 2, 1, 0
mov    pwmp, #40h                   ; Fpwm = Fosc/(2*(1+PWMP)*255)
mov    pwm0, #14h                   ; duty cycle high/low = PWM0/(255-PWM0)
mov    pwm1, #18h
mov    pwm2, #20h
mov    pwm3, #b0h
mov     pwmcon1, #11111111b         ; output enable pwm3, 2, 1, 0
```

### 15.3.5 GC Mode

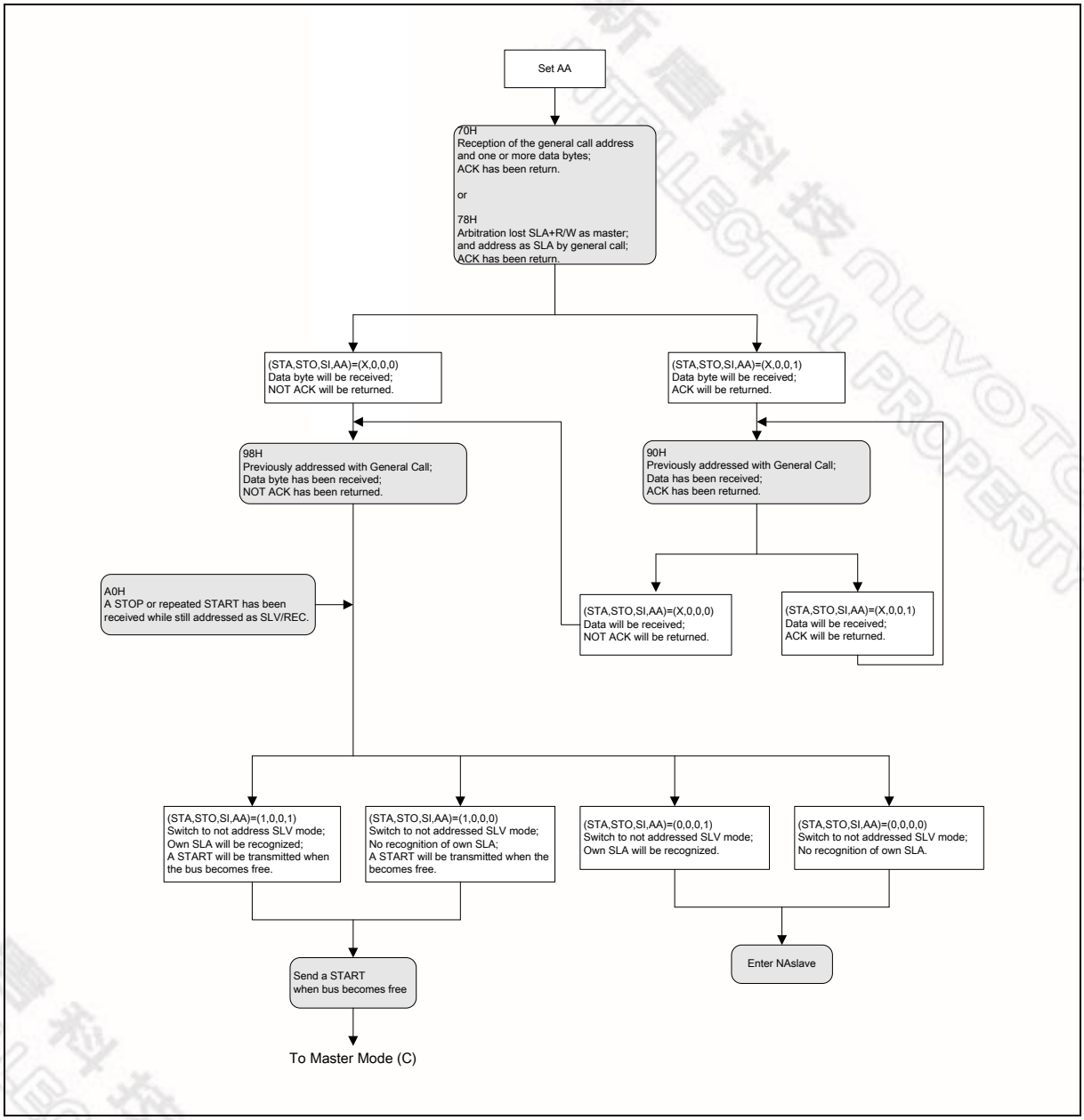



Figure 15-9 General Call Address

### ADC Converter Result High Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ADC.9 | ADC.8 | ADC.7 | ADC.6 | ADC.5 | ADC.4 | ADC.3 | ADC.2 |

Mnemonic: ADCH Address: C2h

ADC[9:2] 8 MSB of 10-bit A/D conversion result. ADCH is a read only register.

### ADC Pin Switch

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ADCPS.7 | ADCPS.6 | ADCPS.5 | ADCPS.4 | ADCPS.3 | ADCPS.2 | ADCPS.1 | ADCPS.0 |

Mnemonic: ADCPS Address: C6h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7-0 | ADCPS.7-0 | Switch I/O pins P1.4~P1.7 and P5.0~P5.3 to analog inputs. Analog inputs, ADC0-ADC3 which share the I/O pins from P1.4 to P1.7 and ADC4-ADC7 which share the I/O pins from P5.0 to P5.3.<br>1: The corresponding I/O pin functions as analog input.<br>0: The corresponding I/O pin functions as digital I/O. |

**ADCPS.3-0: Switch P1.7~P1.4 to analog input function**

| BIT | CORRESPONDING PIN | BIT | CORRESPONDING PIN |
|---|---|---|---|
| ADCPS.0 | P1.4 | ADCPS.4 | P5.0 |
| ADCPS.1 | P1.5 | ADCPS.5 | P5.1 |
| ADCPS.2 | P1.6 | ADCPS.6 | P5.2 |
| ADCPS.3 | P1.7 | ADCPS.7 | P5.3 |

| | | | | | |
|---|---|---|---|---|---|
| Input High Voltage<br>P0, P1, P2, P3, P4, P5, P6, P7, $\overline{EA}$ | $V_{IH1}$ | 2.4 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| Input High Voltage RST | $V_{IH2}$ | 3.5 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| Input High Voltage<br>XTAL1[*3] | $V_{IH3}$ | 3.5 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| Sink current<br>P1, P3, P4, P5, P6, P7 | $I_{sk1}$ | 4 | 8 | mA | $V_{DD}$ =4.5V<br>$V_s$ = 0.45V |
| Sink current<br>P0,P2, ALE, $\overline{PSEN}$ | $I_{sk2}$ | 10 | 14 | mA | $V_{DD}$ =4.5V<br>$V_{OL}$ = 0.45V |
| Source current<br>P1, P3, P4, P5, P6, P7 | $I_{sr1}$ | -180 | -360 | uA | $V_{DD}$ =4.5V<br>$V_{OL}$ = 2.4V |
| Source current<br>P0, P2, ALE, $\overline{PSEN}$ | $I_{sr2}$ | -10 | -14 | mA | $V_{DD}$ =4.5V<br>$V_{O}$L = 2.4V |
| Output Low Voltage<br>P1, P3, P4, P5, P6, P7 | $V_{OL1}$ | - | 0.45 | V | $V_{DD}$ = 4.5V<br>$I_{OL}$ = +6 mA |
| Output Low Voltage<br>P0, P2, ALE, $\overline{PSEN}$ [*2] | $V_{OL2}$ | - | 0.45 | V | $V_{DD}$ = 4.5V<br>$I_{OL}$ = +10 mA |
| Output High Voltage<br>P1, P3, P4, P5, P6, P7 | $V_{OH1}$ | 2.4 | - | V | $V_{DD}$ = 4.5V<br>$I_{OH}$ = -180 μA |
| Output High Voltage<br>P0, P2, ALE, $\overline{PSEN}$ [*2] | $V_{OH2}$ | 2.4 | - | V | $V_{DD}$ = 4.5V<br>$I_{OH}$ = -10mA |

**Notes:**

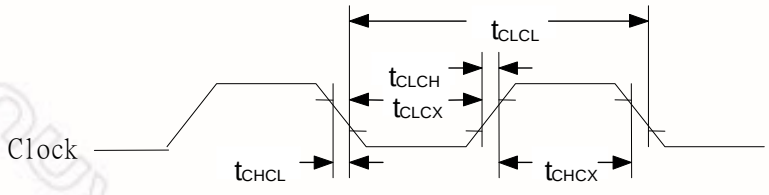
*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

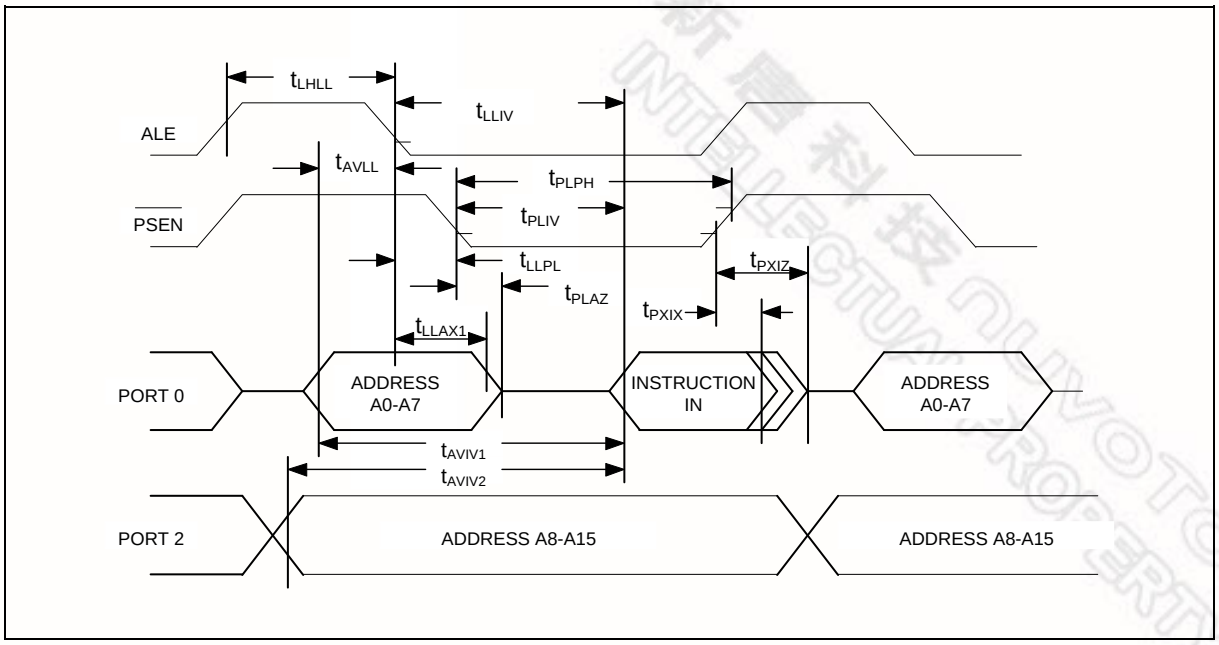
*4. Pins of P0, P1, P2, P3, P4, P5, P6, P7 can source a transition current when they are being externally driven from 1 to 0. The transition
current reaches its maximum value when VIN approximates to 2V.

## 23.3 AC Characteristics




**Note**: Duty cycle is 50%.

## 23.5 Program Memory Read Cycle




## 23.6 Data Memory Read Cycle