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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 4.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79l659a25fl

1. General Description

The W79E659 is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E659 executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E659 can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E659 provides 256 bytes of on-chip RAM; 1-KB of auxiliary RAM; seven 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; an UART serial port, 2 channels of I2C with master/slave capability and 8 channels of 10-bit ADC. These peripherals are all supported by ten interrupt sources with 2 levels of priority.

The W79E659 contains a 32-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

Note: If the applied V_{DD} is not stable, especially with long transition time of power on/off, it's recommended to apply an external RESET IC to the RST pin for improving the stability of system.

2. Features

- Fully-static-design 8-bit Turbo 51 CMOS microcontroller up to 40MHz
- 32-KB of in-system-programmable Flash EPROM (AP Flash EPROM with ISP)
- 4-KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM)
- 1-KB auxiliary RAM, software-selectable, accessed by MOVX instruction
- 256 bytes of scratch-pad RAM
- Seven 8-bit bi-directional ports
- All pins with Schmitt trigger inputs
- One 4-bit multipurpose I/O port4 with Chips select(CS) and boot function
- Three 16-bit timers
- 6 channels of 8-bit PWM
- One enhanced full-duplex UART with framing-error detection and automatic address recognition
- 2-channels of I2C with master/slave capability
- 10-bit ADC with 8-channel inputs
- Software programmable access cycle to external RAM/peripherals
- 10 interrupt sources with two levels of priority
- Software reset function
- Optional H/L state of ALE/PSEN during power down mode
- Built-in power management
- Code protection
- Development tool
  - JTAG ICE(In Circuit Emulator) tool
- Packages:
  - Lead Free(RoHS) QFP 100: W79E659A40FL, W79L659A25FL

4. PIN DESCRIPTION

SYMBOL	TYPE[1]	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	**RESET:** Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	**CRYSTAL 1:** Crystal oscillator input or external clock input.
XTAL2	O	**CRYSTAL 2:** Crystal oscillator output.
V_{SS}	I	**GROUND**: ground potential.
V_{DD}	I	**POWER SUPPLY:** Supply voltage for operation.
AV_{SS}	I	**Analog GROUND:** for ADC
AV_{DD}	I	**Analog Power Supply:** for ADC
P0.0–P0.7	I/O D S H	**PORT 0:** 8-bit, bi-directional I/O port with internal pull-up resisters. This port also provides a multiplexed, low-order address / data bus during accesses to external memory.
P1.0–P1.7	I/O S H	**PORT 1:** 8-bit, bi-directional I/O port with internal pull-up resistors. This port also provides alternate functions as below. P1.0 ~ P1.5 provide PWM0 ~ PWM5. P1.4 ~ P1.7 provide ADC0 ~ ADC3. P1.0 alternately provides Timer2 external count input.(T2) P1.1 alternately provides Timer2 Reload/Capture/Direction control.(T2Ex)
P2.0–P2.7	I/O S H	**PORT 2:** 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory. P2.4 to P2.7 can be software configured as I2C serial ports
P3.0–P3.7	I/O S H	**PORT 3:** 8-bit, bi-directional I/O port with internal pull-up resistors. All bits have alternate functions, which are described below: RXD (P3.0): Serial Port 0 input TXD (P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0 (P3.4):Timer 0 External Input T1 (P3.5):Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe

PWM Control Register2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4

Mnemonic: PWMCON2 Address: CEh

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	PWM5OE	Output enable for PWM5 0: Disable PWM5 Output. 1: Enable PWM5 Output.
2	PWM4OE	Output enable for PWM4 0: Disable PWM4 Output. 1: Enable PWM4 Output.
1	ENPWM5	Enable PWM5 0: Disable PWM5. 1: Enable PWM5.
0	ENPWM4	Enable PWM4 0: Disable PWM4. 1: Enable PWM4.

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high-order nibble.
5	F0	User flag 0: A general-purpose flag that can be set or cleared by the user.
4	RS1	Register Bank select bits. See table below.
3	RS0	Register Bank select bits. See table below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit, or vice versa, as a result of the previous operation.
1	F1	User flag 1: A general-purpose flag that can be set or cleared by the user.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number of 1's in the accumulator.

```
TA      EG    C7H
WDCON   REG   D8H
CKCON   REG   8EH
              MOV   TA, #AAH
              MOV   TA, #55H
              SETB  WDCON.0              ; Reset Watchdog Timer
              ORL   CKCON, #11000000B    ; Select 26 bits Watchdog Timer
              MOV   TA, #AAH
              MOV   TA, #55H
              ORL   WDCON, #00000010B    ; Enable watchdog
```

The other bits in WDCON have unrestricted write access.

PWM Pre-scale Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWMP Address: D9h

PWMP.7-0 Adjust PWM frequency. $Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$

PWM0

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM0 Address: DAh

PWM0.7-0 Adjust PWM0 duty cycle. $PWMn\ high/low\ ratio\ of\ PWMn = \frac{PWMn}{255 - (PWMn)}$

PWM1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM1 Address: DBh

PWM1.7-0 Adjust PWM1 duty cycle.

PWM Control Register1

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0

Mnemonic: PWMCON1 Address: DCh

Instruction Set for W79E659, continued

OP-CODE	HEX CODE	BYTES	W79E659 MACHINE CYCLE	W79E659 CLOCK CYCLES	8032 CLOCK CYCLES	W79E659 VS. 8032 SPEED RATIO
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5

Instruction Set for W79E659, continued

OP-CODE	HEX CODE	BYTES	W79E659 MACHINE CYCLE	W79E659 CLOCK CYCLES	8032 CLOCK CYCLES	W79E659 VS. 8032 SPEED RATIO
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

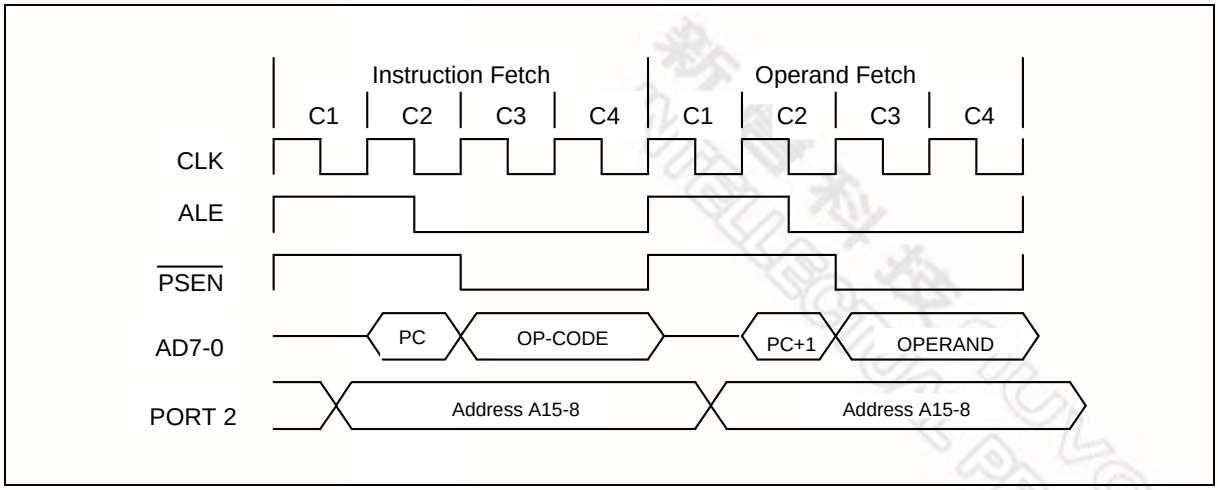


Figure 7-2 Two Cycle Instruction Timing

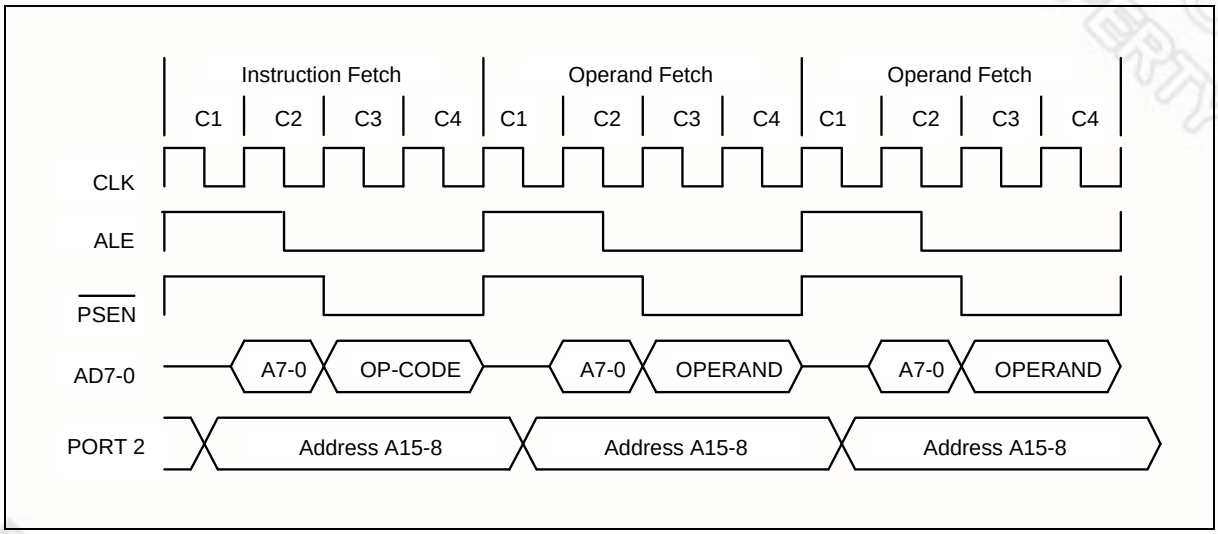


Figure 7-3 Three Cycle Instruction Timing

9.5 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state and makes Port 0 float (as it does not have on-chip pull-up resistors). The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2 V, the minimum operating voltage for the RAM. If VDD falls below 2 V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depends on the source of the reset. The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is cleared to 0 on a Power-on reset and unaffected by other resets. All the bits in this SFR have unrestricted read access. The bits of POR, WDIF, EWT and RWT require Timed Access (TA) procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

Table 9-1 lists the different reset values.

Table 9-1 The WDCON reset values in three reset conditions

WDCON	Watch-Dog Control	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	0x0x 0xx0B External reset 0x0x 01x0B Watchdog reset 0100 0000B Power on reset

10. Interrupts

The W79E659 has a two priority level interrupt structure with 10 interrupt sources. Each interrupt source has a separate priority bit, interrupt flag, interrupt enable bit, and interrupt vector. In addition, all the interrupts can be globally disabled.

10.1 Interrupt Sources

External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be edge-triggered or level-triggered, depending on bits IT0 and IT1. In edge-triggered mode, the INTx input is sampled every machine cycle. If the sample is high in one cycle and low in the next, then a high-to-low transition is detected, and the interrupt request flag IEx in TCON is set. This flag requests the interrupt, and it is automatically cleared when the interrupt service routine is called. Since external interrupts are sampled every machine cycle, the input has to be held high or low for at least one complete machine cycle. In level-triggered mode, the requesting source has to hold the pin low until the interrupt is serviced. The IEx flag is not cleared automatically when the service routine is called, and, if the input continues to be held low after the service routine is completed, the signal may generate another interrupt request.

Timer 0 and 1 interrupts are generated by the TF0 and TF1 flags. These flags are set by a timer overflow, and they are cleared automatically when the interrupt service routine is called. The Timer 2 interrupt is generated by a logical-OR of the TF2 (overflow) and the EXF2 (capture / reload events) flags. The hardware does not clear these flags when the interrupt service routine is called, so the software has to resolve the cause of the interrupt and clear the appropriate flag(s).

When ADC conversion is completed hardware will set flag ADCI to logic high to request ADC interrupt if bit EADC (IE.6) is in high state. ADCI is cleared by software only. W79E659 provides 2 identically independent I2C serial ports, I2C1 and I2C2. When a new SIO1 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C2 bits are both set, the I2C2 interrupt is requested. **SI must be cleared by software**.

The Watchdog Timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by bit EIE.4, then an interrupt is generated.

All of the interrupt flags can be set or reset by software, as well as hardware, by setting or clearing the appropriate bit in the IE register. This register also has the global disable bit EA, which can be cleared to disable all interrupts.

11.1.3 Mode 1

Mode 1 is the same as Mode 0, except that the timer/counter is 16 bits, instead of 13 bits.

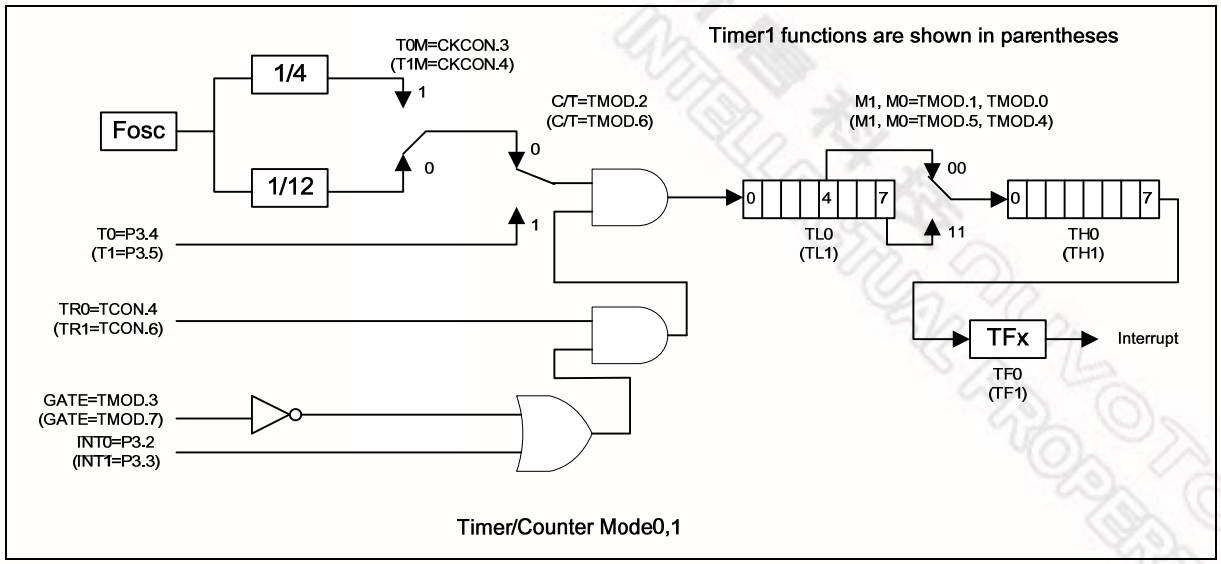


Figure 11-1 Timer/Counters 0/1 in Mode 0 & Mode 1

11.1.4 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

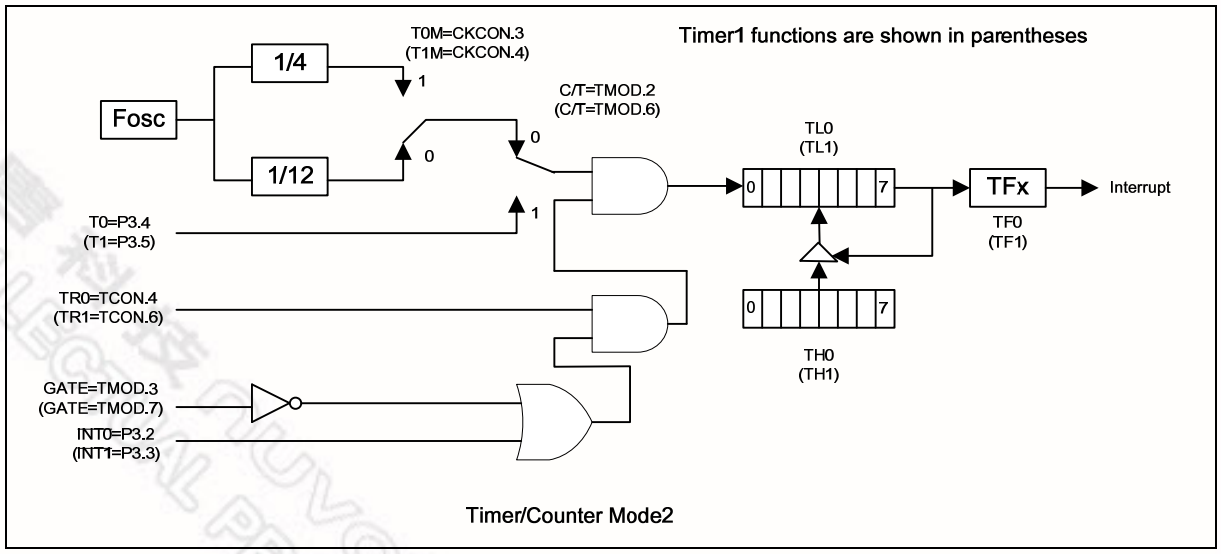


Figure 11-2 Timer/Counter 0/1 in Mode 2

```
start:
        mov     ckcon,#01h              ; select 2 ^ 17 timer
;       mov     ckcon,#61h              ; select 2 ^ 20 timer
;       mov     ckcon,#81h              ; select 2 ^ 23 timer
;       mov     ckcon,#c1h              ; select 2 ^ 26 timer
        mov     TA,#aah
        mov     TA,#55h
        mov     WDCON,#00000011B
        setb    EWDI
        setb    ea
        jmp     $                       ; wait time out
```

Clock Control

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the Watchdog Timer. The reset interval is 512 clocks longer than the selected interval. The default time-out is 2^{17} clocks, the shortest time-out period.

Table 15-1 Control Registers of I2C Ports

SYMBOL	DEFINITION	ADDRESS	MSB		BIT_ADDRESS, SYMBOL				LSB		RESET
I2TIMER2	I2C2 Timer Counter Register	FFH	-	-	-	-	-	ENTI2	DIV42	TIF2	0000 0000B
I2CLK2	I2C2 Clock Rate	FEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS2	I2C2 Status Register	FDH						-	-	-	0000 0000B
I2DAT2	I2C2 Data	FCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR21	I2C2 Slave Address1	FBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR20	I2C2 Slave Address0	FAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON2	I2C2 Control Register	F9H	-	ENS2	STA	STO	SI	AA	-	PSEL2	x000 00x0B
I2TIMER	I2C1 Timer Counter Register	EFH	-	-	-	-	-	ENTI	DIV4	TIF	0000 0000B
I2CLK	I2C1 Clock Rate	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C1 Status Register	EDH						-	-	-	0000 0000B
I2DAT	I2C1 Data	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR11	I2C1 Slave Address1	EBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR10	I2C1 Slave Address0	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON	I2C1 Control Register	E9H	-	ENS1	STA	STO	SI	AA	-	PSEL1	x000 00x0B

15.1.1 Slave Address Registers, I2ADDRxx

Each I2C port is equipped with two slave address registers. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDRxx are matched with the received slave address.

The I2C ports support the "General Call" function. If the GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

15.1.2 Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. Data in I2DAT remains stable as long as SI is set. The MSB is shifted out first. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus.

I2DAT and the acknowledge bit form a 9-bit shift register which shifts in or out an 8-bit byte, followed by an acknowledge bit. The acknowledge bit is controlled by the hardware and cannot be accessed by the CPU. Serial data is shifted into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses.

15.3.4 Slave/Receiver Mode

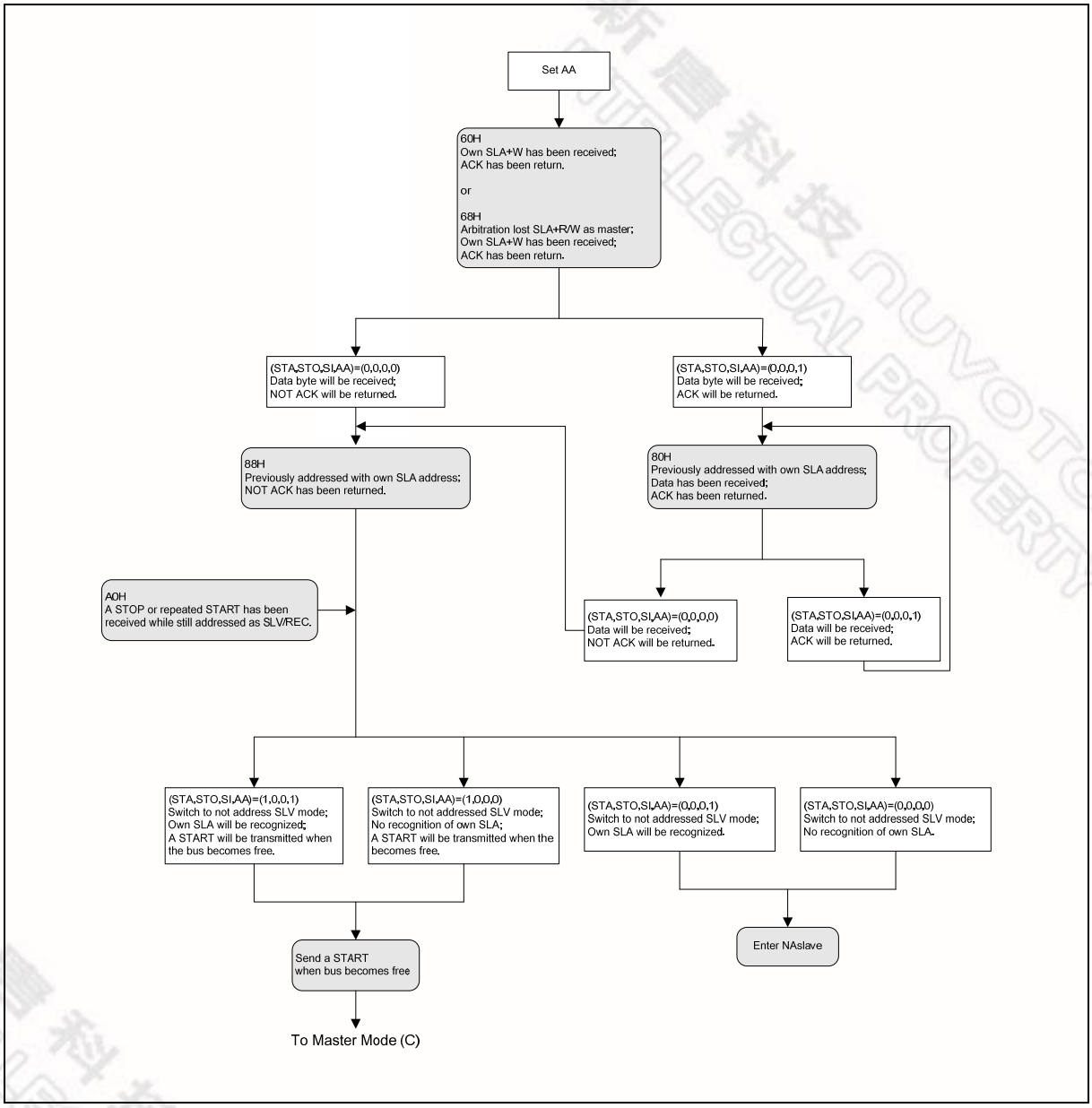


Figure 15-8 Slave Receiver Mode

20. In-System Programming

20.1 The Loader Program Locates at LDFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LDFlash memory and execute a reset action. H/W reboot mode will switch to LDFlash memory, too. Set SFRCN register where it locates at user's loader program to update APFlash memory. Set a SWRESET (CHPCON.7) to switch back APFlash after CPU has updated APFlash program. CPU will restart to run program from reset state.

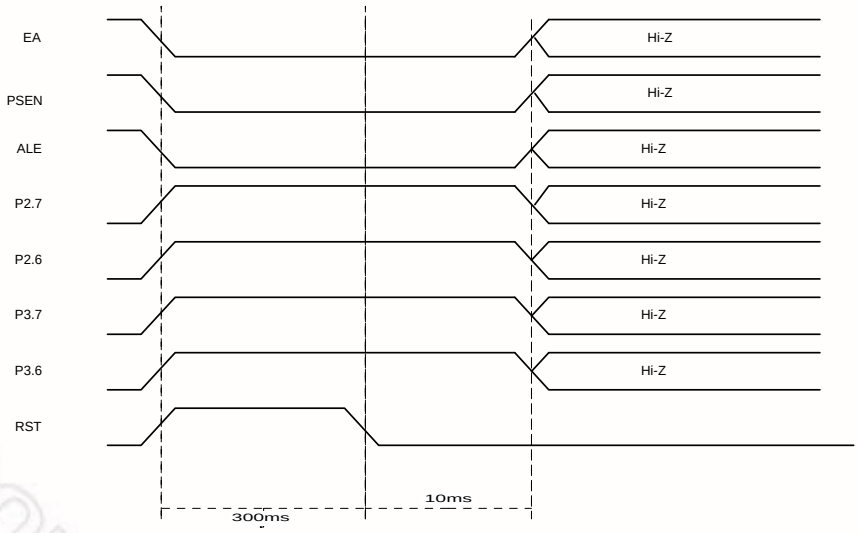
20.2 The Loader Program Locates at APFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LDFlash. CPU will continue to run user's APFlash program after CPU has updated program. Please refer demonstrative code to understand other detail description.

21. H/W Writer Mode

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.

The Timing For Entering Flash EPROM Mode on the Programmer



22. Security Bits

During the on-chip FLASH EPROM programming mode, the FLASH EPROM can be programmed and verified repeatedly. And the program code can be protected by setting security bits. The protection of FLASH EPROM and those operations on it are described below.

The W79E659 has several Special Setting Registers, including the Security Register and Company/Device ID Registers, which can not be accessed in programming mode. Those bits of the Security bits can not be changed once they have been programmed from high to low. They can only be reset to the default value FFh through “Erase-All” operation. The contents of the Company ID and Device ID registers have been set in factory.

If user doesn’t need ISP function, do not fill “FFh” code in LD Flash memory. The writer always writes both AP and LD flash in a completed program procedure.

Table 22-1 Security Bits

BIT	DESCRIPTION
B0	=0: Lock data out
B1	=0: MOVC Inhibited
B2	Reserved
B3	Reserved
B4	=1: Disable H/W reboot by P2.6 and P2.7 =0: Enable H/W reboot by P2.6 and P2.7
B5	=1: Disable H/W reboot by P4.3 =0: Enable H/W reboot by P4.3
B6	Reserved
B7	=1: Crystal > 24MHz =0: Crystal < 24MHz

B0: Lock bit

This bit is used to protect the customer's program code in the W79E659. After the programmer finishes the programming and verifies sequence B0 can be cleared to logic 0 to protect code from reading by any access path. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

B1: MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

23. Electrical Characteristics

23.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	+70	°C
Storage Temperature	T_{st}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

23.2 DC Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, TA = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5 3.0	5.5 4.5	V	For W79E659 version For W79L659 version
Operating Current	I_{DD}	-	30	mA	No load V_{DD} = RST = 5.5V
Idle Current	I_{IDLE}	-	24	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	10	µA	Power-down mode V_{DD} = 5.5V
Input Current P0, P1, P2, P3,P4, P5, P6, P7	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or VDD
Input Current RST[*1]	I_{IN2}	-	100	µA	V_{DD} = 5.5V 0<V_{IN}<VDD
Input Leakage Current $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5, P6, P7	I_{TL}[*4]	-500	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, P5, P6, P7, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V

23.3.1 External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12	-	-	nS	
Clock Low Time	t_{CLCX}	12	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

23.3.2 AC Specification

($V_{DD} - V_{SS}$ = 5V ±10%, TA = 25°C, Fosc = 20 MHz, unless otherwise specified.

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	40[1]	MHz
Oscillator Frequency	$1/t_{CLCL}$	0	33[2]	MHz
ALE Pulse Width	t_{LHLL}	$1.5t_{CLCL}$ - 5		nS
Address Valid to ALE Low	t_{AVLL}	$0.5t_{CLCL}$ - 5		nS
Address Hold After ALE Low	t_{LLAX1}	$0.5t_{CLCL}$ - 5		nS
Address Hold After ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$ - 5		nS
ALE Low to Valid Instruction In	t_{LLIV}		$2.5t_{CLCL}$ - 20	nS
ALE Low to PSEN Low	t_{LLPL}	$0.5t_{CLCL}$ - 5		nS
$\overline{PSEN}$ Pulse Width	t_{PLPH}	$2.0t_{CLCL}$ - 5		nS
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		$2.0t_{CLCL}$ - 20	nS
Input Instruction Hold After PSEN	t_{PXIX}	0		nS
Input Instruction Float After PSEN	t_{PXIZ}		t_{CLCL} - 5	nS
Port 0 Address to Valid Instr. In	t_{AVIV1}		$3.0t_{CLCL}$ - 20	nS
Port 2 Address to Valid Instr. In	t_{AVIV2}		$3.5t_{CLCL}$ - 20	nS
$\overline{PSEN}$ Low to Address Float	t_{PLAZ}	0		nS
Data Hold After Read	t_{RHDX}	0		nS
Data Float After Read	t_{RHDZ}		t_{CLCL} - 5	nS
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL}$ - 5	nS

Note: 1. CPU executes the program stored in the internal APFlash at V_{DD}=5.0V
2. CPU executes the program stored in the external memory at V_{DD}=5.0V

M2	M1	M0	MOVX CYCLES	T_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Explanation of Logics Symbols

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{PSEN}$
Q	Output Data	R	$\overline{RD}$ signal
V	Valid	W	$\overline{WR}$ signal
X	No longer a valid state	Z	Tri-state

23.4 The ADC Converter DC ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V±10%, T_A = -40~85°C, Fosc = 20MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Analog input	AVin	V_{SS}-0.2	V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	5MHz	Hz	ADC circuit input clock
Conversion time	t_C	$52t_{ADC}$[1]		us	
Differential non-linearity	DNL	-1	+1	LSB	
Integral non-linearity	INL	-2	+2	LSB	Fosc=20MHz
		-5	+5	LSB	Fosc=40MHz
Offset error	Ofe	-1.5	+1.5	LSB	Fosc=20MHz
		-2.5	+2.5	LSB	Fosc=40MHz
Gain error	Ge	-1	+1	%	
Absolute voltage error	Ae	-5	+5	LSB	Fosc=20MHz
		-11	+11	LSB	Fosc=40MHz

Notes: 1. t_{ADC} : The period time of ADC input clock.

```
MAIN_APFlash:
        MOV  A,P1               ; SCAN P1.0
        ANL  A,#01H
        CJNE  A,#01H,PROGRAM_APFlash     ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING
                                         ; MODE
        JMP  NORMAL_MODE

PROGRAM_64:
        MOV  TA, #AAH           ; CHPCON register is written protect by TA register.
        MOV  TA, #55H
        MOV  CHPCON, #03H       ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV  SFRCN, #0H
        MOV  TCON, #00H         ; TR = 0 TIMER0 STOP
        MOV  IP, #00H           ; IP = 00H
        MOV  IE, #82H           ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV  R6, #F0H           ; TL0 = F0H
        MOV  R7, #FFH           ; TH0 = FFH
        MOV  TL0, R6
        MOV  TH0, R7
        MOV  TMOD, #01H         ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV  TCON, #10H         ; TCON = 10H, TR0 = 1,GO
        MOV  PCON, #01H         ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                ; PROGRAMMING
;************** ********************************************************************
;* Normal mode APFlash program: depending user's application
;*****************************************************************************
NORMAL_MODE:
                                .
                                ; User's application program
                                .
                                .
                                .
```

EXAMPLE 2:

```
;*************************************************************************************************************
;* Example of 4KB LDFlash program: This loader program will erase the APFlash first, then reads the
new ;* code from external SRAM and program them into APFlash bank. XTAL = 24 MHz
;*************************************************************************************************************
.chip 8052
.RAMCHK OFF
.symbols

CHPCON          EQU             9FH
```

```
                                ; DEPENDING ON USER'S SYSTEM CLOCK RATE.
MOV  R7,#8AH
MOV  TL0,R6
MOV  TH0,R7

ERASE_P_4K:
MOV  SFRCN,#22H     ; SFRCN = 22H, ERASE APFlash0
                    ; SFRCN = A2H, ERASE APFlash1
MOV  TCON,#10H      ; TCON = 10H, TR0 = 1,GO
MOV  PCON,#01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
MOV  SFRCN,#0H      ; SFRCN = 00H, READ APFlash0
                    ; SFRCN = 80H, READ APFlash1
MOV  SFRAH,#0H      ; START ADDRESS = 0H
MOV  SFRAL,#0H
MOV  R6,#FDH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
MOV  R7,#FFH
MOV  TL0,R6
MOV  TH0,R7

blank_check_loop:
        SETB  TR0               ; enable TIMER 0
        MOV  PCON,#01H          ; enter idle mode
        MOV  A,SFRFD            ; read one byte
        CJNE  A,#FFH,blank_check_error
        INC  SFRAL              ; next address
        MOV  A,SFRAL
        JNZ   blank_check_loop
        INC  SFRAH
        MOV  A,SFRAH
        CJNE  A,#0H,blank_check_loop   ; end address = FFFFH
        JMP  PROGRAM_APFlashROM

blank_check_error:
        JMP  $

;*****************************************************************************
;* RE-PROGRAMMING APFlash BANK
;*****************************************************************************
PROGRAM_APFlashROM:
```