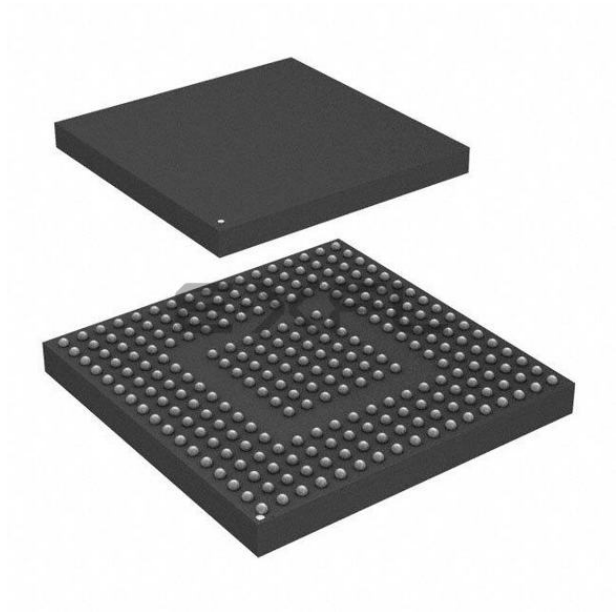

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kf0mmm2

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

1.6.4 Enhanced Direct Memory Access (eDMA) controller

- 32 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

1.6.5 Interrupt Controller (INTC)

- 208 peripheral interrupt requests
- 8 software settable sources
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

1.6.6 Frequency-Modulated Phase-Locked Loop (FMPLL)

Two FMPLLs are available on each device.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor and output clock divider ratio are software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 2 modes of operation
  - Normal PLL mode with crystal reference (default)
  - Normal PLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers as well as jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows running motor control periphery at different (precisely lower, equal, or higher, as required) frequency than the system to ensure higher resolution

1.6.11 DRAM controller

The DRAM controller (available only on 473-pin devices) is a multi-port controller that monitors incoming requests on the three AHB slave ports and decides (at each rising clock edge) what command needs to be sent to the external DRAM.

The DRAM controller on this device supports the following types of memories:

- Mobile DDR (mDDR)
- DDR 1
- DDR 2 (optional)
- SDR

The controller has the following features:

- Optimized timing for 32-byte bursts and single read accesses on the AHB interface
- Optimized timing for 8-byte and 16-byte bursts on the DRAMC interface
- Supports priority elevation on the slave ports for single accesses
- 16-bit wide DRAM interface
- One chip select (CS)
- mDDR memory controller
  - 16-bit external interface
  - Address range up to 8 MB

1.6.12 Boot Assist Module (BAM)

- Enables booting via serial mode (FlexCAN, LINFlex)
- Handles static mode in case of an erroneous boot procedure
- Implemented in 8 KB ROM
- Supports Lock Step Mode (LSM) and Decoupled Parallel Mode (DPM)

1.6.13 Parallel Data Interface (PDI)

- Support for external ADC and CMOS image sensors
- Parallel interface operation up to MCU system bus frequency
- Selectable data capture from rising or falling edge
- Receive FIFO with adjustable trigger thresholds
- Data width for 8, 10, 12, 14, and 16 bits
- Data Packing Unit to pack input data on 64-bit words — data packed on 8- or 16- bit boundary, depending on input data width
- Binary increasing channel select that allows as many as eight channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK

1.6.14 Deserial Serial Peripheral Interface (DSPI) modules

- Three serial peripheral interfaces
  - Full duplex communication ports with interrupt and eDMA request support
  - Support for all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
AA21	VSS_HV_IO	VSS_HV	M15	VSS_LV_COR	VSS_LV
AB1	VSS_HV_IO	VSS_HV	M16	VSS_LV_COR	VSS_LV
AB23	VSS_HV_IO	VSS_HV	M17	VSS_LV_COR	VSS_LV
AC1	VSS_HV_IO	VSS_HV	N7	VSS_LV_COR	VSS_LV
AC2	VSS_HV_IO	VSS_HV	N8	VSS_LV_COR	VSS_LV
AC22	VSS_HV_IO	VSS_HV	N9	VSS_LV_COR	VSS_LV
AC23	VSS_HV_IO	VSS_HV	N10	VSS_LV_COR	VSS_LV
AC13	VSS_HV_ADR_0	VSS_HV_A	N11	VSS_LV_COR	VSS_LV
AC16	VSS_HV_ADR_1	VSS_HV_A	N12	VSS_LV_COR	VSS_LV
AC8	VSS_HV_ADR_23	VSS_HV_A	N13	VSS_LV_COR	VSS_LV
AA10	VSS_HV_ADV	VSS_HV_A	N14	VSS_LV_COR	VSS_LV
H23	VSS_HV_DRAM	VSS_HV	N15	VSS_LV_COR	VSS_LV
L22	VSS_HV_DRAM	VSS_HV	N16	VSS_LV_COR	VSS_LV
P22	VSS_HV_DRAM	VSS_HV	N17	VSS_LV_COR	VSS_LV
V22	VSS_HV_DRAM	VSS_HV	P7	VSS_LV_COR	VSS_LV
D12	VSS_HV_FLA	VSS_HV	P8	VSS_LV_COR	VSS_LV
Y1	VSS_HV_OSC	VSS_HV	P9	VSS_LV_COR	VSS_LV
C21	VSS_HV_PDI	VSS_HV	P10	VSS_LV_COR	VSS_LV
D17	VSS_HV_PDI	VSS_HV	P11	VSS_LV_COR	VSS_LV
G7	VSS_LV_COR	VSS_LV	P12	VSS_LV_COR	VSS_LV
G8	VSS_LV_COR	VSS_LV	P13	VSS_LV_COR	VSS_LV
G9	VSS_LV_COR	VSS_LV	P14	VSS_LV_COR	VSS_LV
G10	VSS_LV_COR	VSS_LV	P15	VSS_LV_COR	VSS_LV
G11	VSS_LV_COR	VSS_LV	P16	VSS_LV_COR	VSS_LV
G12	VSS_LV_COR	VSS_LV	P17	VSS_LV_COR	VSS_LV
G13	VSS_LV_COR	VSS_LV	R7	VSS_LV_COR	VSS_LV
G14	VSS_LV_COR	VSS_LV	R8	VSS_LV_COR	VSS_LV
G15	VSS_LV_COR	VSS_LV	R9	VSS_LV_COR	VSS_LV
G16	VSS_LV_COR	VSS_LV	R10	VSS_LV_COR	VSS_LV
G17	VSS_LV_COR	VSS_LV	R11	VSS_LV_COR	VSS_LV
H7	VSS_LV_COR	VSS_LV	R12	VSS_LV_COR	VSS_LV
H8	VSS_LV_COR	VSS_LV	R13	VSS_LV_COR	VSS_LV
H9	VSS_LV_COR	VSS_LV	R14	VSS_LV_COR	VSS_LV
H10	VSS_LV_COR	VSS_LV	R15	VSS_LV_COR	VSS_LV

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
B13	GPIO	fec TX_ER	A0: siul_GPIO[205] A1: fec_TX_ER A2: dspi2_CS3 A3: _	I: flexpwm1_FAULT[3] I: lin0_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B16	GPIO	pdi DATA[4]	A0: siul_GPIO[135] A1: flexpwm2_A[2] A2: _ A3: etimer1_ETC[4]	I: pdi_DATA[4] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B17	GPIO	pdi DATA[0]	A0: siul_GPIO[131] A1: _ A2: lin3_TXD A3: _	I: pdi_DATA[0] I: _ I: flexpwm2_FAULT[2]	—	disabled	PDI Medium	VDD_HV_PDI
B18	GPIO	pdi LINE_V	A0: siul_GPIO[129] A1: _ A2: lin2_TXD A3: _	I: pdi_LINE_V I: _ I: flexpwm2_FAULT[0]	—	disabled	PDI Medium	VDD_HV_PDI
B19	GPIO	pdi DATA[9]	A0: siul_GPIO[140] A1: flexpwm2_X[2] A2: _ A3: _	I: pdi_DATA[9] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B20	GPIO	pdi DATA[14]	A0: siul_GPIO[145] A1: pdi_SENS_SEL[1] A2: i2c2_clock A3: _	I: pdi_DATA[14] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B21	GPIO	can0 TXD	A0: siul_GPIO[16] A1: can0_TXD A2: _ A3: sscm_DEBUG[0]	I: _ I: _ I: siul_EIRQ[15]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C2	GPIO	nexus MDO[15][1]	A0: siul_GPIO[220] A1: _ A2: npc_wrapper_MDO[15] A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
C5	GPIO	flexray CB_RX	A0: siul_GPIO[50] A1: _ A2: ctu1_EXT_TGR A3: _	I: flexray_CB_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C6	GPIO	etimer0 ETC[4]	A0: siul_GPIO[43] A1: etimer0_ETC[4] A2: _ A3: _	I: _ I: mc_rgm_ABS[0] I: _	—	pulldown	GP Slow/ Medium	VDD_HV_IO
C7	GPIO	etimer0 ETC[1]	A0: siul_GPIO[1] A1: etimer0_ETC[1] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[1]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C8	GPIO	etimer0 ETC[2]	A0: siul_GPIO[2] A1: etimer0_ETC[2] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[2]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C9	GPIO	etimer0 ETC[3]	A0: siul_GPIO[3] A1: etimer0_ETC[3] A2: _ A3: _	I: _ I: mc_rgm_ABS[2] I: siul_EIRQ[3]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
C10	GPIO	fec TXD[2]	A0: siul_GPIO[203] A1: fec_TXD[2] A2: _ A3: _	I: flexpwm1_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C11	GPIO	fec TXD[1]	A0: siul_GPIO[202] A1: fec_TXD[1] A2: _ A3: dspi2_SCK	I: flexpwm1_FAULT[0] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C12	GPIO	fec CRS	A0: siul_GPIO[208] A1: flexray_DBG1 A2: etimer2_ETC[3] A3: dspi0_CS5	I: fec_CRS I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C13	GPIO	fec RX_CLK	A0: siul_GPIO[209] A1: flexray_DBG2 A2: etimer2_ETC[2] A3: dspi0_CS6	I: fec_RX_CLK I: _ I: siul_EIRQ[25]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
E23	GPIO	dramc BA[2]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F1	GPIO	nexus MDO[10][1]	A0: siul_GPIO[109] A1: _ A2: npc_wrapper_MDO[10] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F4	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F20	GPIO	dramc RAS	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F21	GPIO	siul GPIO[194]	A0: siul_GPIO[194] A1: flexpwm0_X[0] A2: ebi_AD28 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F22	GPIO	siul GPIO[148]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F23	GPIO	dramc D[5]	A0: siul_GPIO[179] A1: dramc_D[5] A2: ebi_AD13 A3: ebi_ADD29	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
G1	GPIO	nexus MCKO	A0: siul_GPIO[87] A1: _ A2: npc_wrapper_MCKO A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G3	GPIO	nexus MDO[8][1]	A0: siul_GPIO[111] A1: _ A2: npc_wrapper_MDO[8] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G4	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G20	GPIO	siul GPIO[196]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_AD30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
G21	GPIO	dramc DQS[0]	A0: siul_GPIO[190] A1: dramc_DQS[0] A2: ebi_AD24 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G22	GPIO	dramc DM[0]	A0: siul_GPIO[192] A1: dramc_DM[0] A2: ebi_AD26 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G23	GPIO	dramc D[7]	A0: siul_GPIO[181] A1: dramc_D[7] A2: ebi_AD15 A3: ebi_ADD31	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
H1	GPIO	nexus EVTO_B	A0: siul_GPIO[90] A1: _ A2: npc_wrapper_EVTO_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
H3	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
L2	GPIO	dspi2 CS2	A0: siul_GPIO[42] A1: dspi2_CS2 A2: lin3_TXD A3: can2_TXD	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
L3	GPIO	dspi2 CS0	A0: siul_GPIO[10] A1: dspi2_CS0 A2: _ A3: can3_TXD	I: _ I: _ I: siul_EIRQ[9]	—	disabled	GP Slow/ Medium	VDD_HV_IO
M1	GPIO	flexpwm0 X[0]	A0: siul_GPIO[57] A1: flexpwm0_X[0] A2: lin2_TXD A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M3	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M20	GPIO	dramc ODT	A0: siul_GPIO[157] A1: dramc_ODT A2: ebi_CS1 A3: flexpwm1_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
M21	GPIO	dramc WEB	A0: siul_GPIO[153] A1: dramc_WEB A2: ebi_WE_BE_2 A3: flexpwm0_A[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
M22	GPIO	dramc D[11]	A0: siul_GPIO[185] A1: dramc_D[11] A2: ebi_AD19 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
M23	GPIO	dramc D[10]	A0: siul_GPIO[184] A1: dramc_D[10] A2: ebi_AD18 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N1	GPIO	flexpwm0 A[0]	A0: siul_GPIO[58] A1: flexpwm0_A[0] A2: _ A3: _	I: _ I: etimer0_ETC[0] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
N3	GPIO	flexpwm0 X[1]	A0: siul_GPIO[60] A1: flexpwm0_X[1] A2: _ A3: _	I: lin2_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N4	GPIO	flexpwm0 B[2]	A0: siul_GPIO[100] A1: flexpwm0_B[2] A2: _ A3: _	I: _ I: etimer0_ETC[5] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N20	GPIO	dramc DQS[1]	A0: siul_GPIO[191] A1: dramc_DQS[1] A2: ebi_AD25 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N21	GPIO	dramc DM[1]	A0: siul_GPIO[193] A1: dramc_DM[1] A2: ebi_AD27 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N22	GPIO	dramc D[13]	A0: siul_GPIO[187] A1: dramc_D[13] A2: ebi_AD21 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N23	GPIO	dramc D[12]	A0: siul_GPIO[186] A1: dramc_D[12] A2: ebi_AD20 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
P1	GPIO	flexpwm0 B[0]	A0: siul_GPIO[59] A1: flexpwm0_B[0] A2: _ A3: _	I: _ I: etimer0_ETC[1] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P2	GPIO	flexpwm0 B[1]	A0: siul_GPIO[62] A1: flexpwm0_B[1] A2: _ A3: _	I: _ I: etimer0_ETC[3] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P3	GPIO	flexpwm0 A[2]	A0: siul_GPIO[99] A1: flexpwm0_A[2] A2: _ A3: _	I: _ I: etimer0_ETC[4] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
U20	GPIO	dramc ADD[6]	A0: siul_GPIO[164] A1: dramc_ADD[6] A2: ebi_ADD14 A3: flexpwm1_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U21	GPIO	dramc ADD[12]	A0: siul_GPIO[170] A1: dramc_ADD[12] A2: ebi_AD4 A3: ebi_ADD20	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U23	GPIO	dramc ADD[0]	A0: siul_GPIO[158] A1: dramc_ADD[0] A2: ebi_ADD8 A3: ebi_CS2	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V3	GPIO	flexpwm1 B[2]	A0: siul_GPIO[124] A1: flexpwm1_B[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V4	GPIO	dspi1 CS2	A0: siul_GPIO[56] A1: dspi1_CS2 A2: _ A3: dspi0_CS5	I: flexpwm0_FAULT[3] I: lin2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V20	GPIO	lin0 TXD	A0: siul_GPIO[18] A1: lin0_TXD A2: i2c0_clock A3: sscm_DEBUG[2]	I: _ I: _ I: siul_EIRQ[17]	—	disabled	GP Slow/ Medium	VDD_HV_IO
V21	GPIO	dramc ADD[13]	A0: siul_GPIO[171] A1: dramc_ADD[13] A2: ebi_AD5 A3: ebi_ADD21	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V23	GPIO	dramc ADD[2]	A0: siul_GPIO[160] A1: dramc_ADD[2] A2: ebi_ADD10 A3: ebi_TA	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
W3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AB4	GPIO	flexpwm1 X[2]	A0: siul_GPIO[122] A1: flexpwm1_X[2] A2: etimer2_ETC[2] A3: dspi0_CS5	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AB5	GPIO	flexpwm1 X[3]	A0: siul_GPIO[125] A1: flexpwm1_X[3] A2: etimer2_ETC[3] A3: dspi0_CS6	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AB6	ANA	adc3 AN[2]	—	siul_GPI[231]	AN: adc3_AN[2]	—	Analog	VDD_HV_ADR23
AB7	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR23
AB8	ANA	adc2 AN[1]	—	siul_GPI[222]	AN: adc2_AN[1]	—	Analog	VDD_HV_ADR23
AB9	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR23
AB10	ANA	adc0 AN[0]	—	siul_GPI[23] lin0_RXD	AN: adc0_AN[0]	—	Analog	VDD_HV_ADR0
AB11	ANA	adc0 AN[4]	—	siul_GPI[70]	AN: adc0_AN[4]	—	Analog	VDD_HV_ADR0
AB12	ANA	adc0 AN[6]	—	siul_GPI[71]	AN: adc0_AN[6]	—	Analog	VDD_HV_ADR0
AB13	ANA	adc0 AN[7]	—	siul_GPI[68]	AN: adc0_AN[7]	—	Analog	VDD_HV_ADR0
AB14	ANA	adc0_adc1 AN[13]	—	siul_GPI[27]	AN: adc0_adc1_AN[13]	—	Analog Shared	VDD_HV_ADR0

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

The “Symbol” column of the electrical parameter and timings tables may contain an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the *input* voltage of a voltage regulator.
- “CC” identifies specifications that define normal device operation. Where available, the letters “P”, “C”, “T”, or “D” replace the letter “CC” and apply to these controller characteristics. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 11. Absolute maximum ratings[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	–0.3	5.5[2]	V
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	–0.1	0.1	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	–0.3	3.63[3,4]	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	–0.1	0.1	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	–0.3	3.63[,4]	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	–0.1	0.1	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	–0.3	3.63[,4]	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	–0.1	0.1	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	–0.3	3.63[,4]	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	–0.1	0.1	V
11	$V_{DD\_HV\_DRAM}$[5]	SR	DRAM interface supply voltage	—	–0.3	3.63[,4]	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	–0.1	0.1	V
13	$V_{DD\_HV\_ADRx}$[6]	SR	ADC*x* high reference voltage	—	–0.3	6.0	V
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	–0.1	0.1	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	–0.3	3.63[3,4]	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	–0.1	0.1	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic	—	–0.3	1.32[7]	V

Table 21. Main oscillator electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
1	F_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
2a	$T_{XOSCHSSU}$	CC	Oscillator start-up time	f_{OSC} < 16 MHz	—	6	10	ms
2b				f_{OSC} = 16 MHz to 40 MHz	—	2	4	
3	V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
4	V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1 V_{DD} = 3.0 V to 3.6 V, T_J = –40 to 150 °C, unless otherwise specified.

3.12 FMPLL electrical characteristics

Table 22. FMPLL electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range[1, 2]	Crystal reference	4	—	120	MHz
2	f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
3	$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	See the FMPLL chapter in the chip reference manual for more details on PLL configuration.	16	—	256	MHz
4	f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	19	—	60	MHz
5	f_{sys}	D	On-chip FMPLL frequency[2]	—	—	—	180	MHz
6	t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
7a	f_{LORL} f_{LORH}	D	Loss of reference frequency window[3]	Lower limit	1.6	—	3.7	MHz
7b				Upper limit	24	—	56	
8	f_{SCM}	D	Self-clocked mode frequency[4,5]	—	20	—	150	MHz
9	t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
10	t_{lpll}	D	FMPLL lock time [6, 7]	—	—	—	200	µs
11	t_{dc}	D	Duty cycle of reference	—	20	—	80	%
12a	C_{JITTER}	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge), $f_{FMPLLOUT}$ maximum[12]	—	—	160	ps
12b				Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	—	—	6	ns
13	Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±500	ps

Table 52. Output drive current @ V_{DDE} = 1.8 V (±100 mV)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
2	DRAM DQ	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
3	DRAM CLK	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 53. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	
2	DRAM DQ	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	

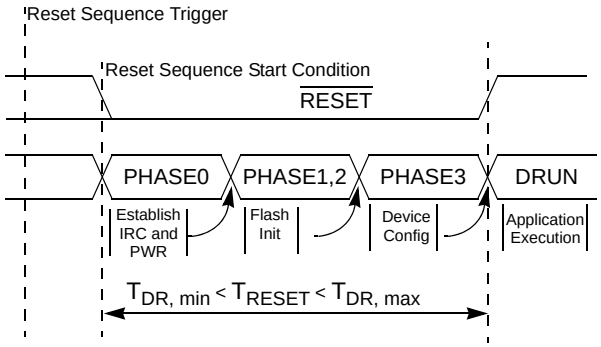

Figure 13. Destructive reset sequence, BIST disabled

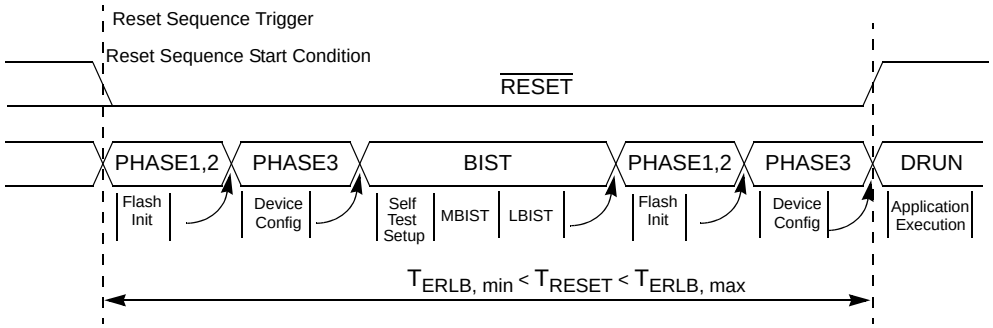

Figure 14. External reset sequence long, BIST enabled

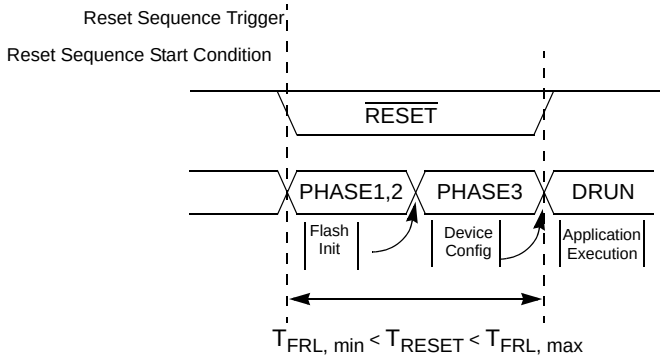

Figure 15. Functional reset sequence long

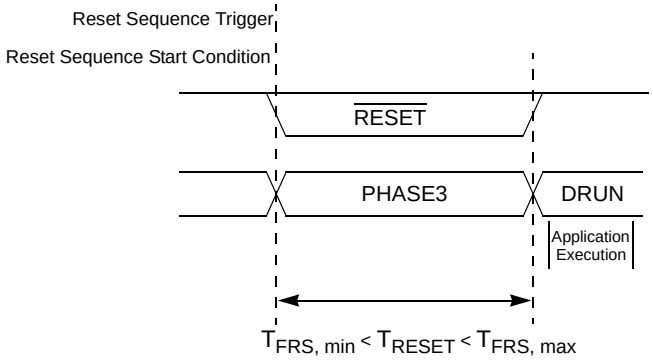

Figure 16. Functional reset sequence short

The reset sequences shown in Figure 15 and Figure 16 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence. See the RGM_FBRE register in the *MPC5675K Reference Manual* for more information.

3.21.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences, depending on the VREG mode (external or internal). It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 58.

JEDEC standards define the minimum set of requirements for compliant memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, MAY 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The MPC5675K supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strength (intended for lighter loads or point-to-point environments)

The MPC5675K memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the Section 3.19, DRAM pad specifications.

3.22.1.1 DDR and DDR2 SDRAM AC timing specifications

Table 61. DDR and DDR2 (DDR2-400) SDRAM timing specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

No.	Symbol		Parameter	Min	Max	Unit
1	t_{CK}	CC	Clock cycle time, CL = *x*	—	90	MHz
2	$V_{IX\text{-}AC}$	CC	MCK AC differential crosspoint voltage[1]	$V_{DD\_MEM\_IO}$ × 0.5 – 0.1	$V_{DD\_MEM\_IO}$ × 0.5 + 0.1	V
3	t_{CH}	CC	CK HIGH pulse width[1, 2]	0.47	0.53	t_{CK}
4	t_{CL}	CC	CK LOW pulse width[1, 2]	0.47	0.53	t_{CK}
5	t_{DQSS}	CC	Skew between MCK and DQS transitions[2, 3]	–0.25	0.25	t_{CK}
6	$t_{OS(base)}$	CC	Address and control output setup time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)		ps
7	$t_{OH(base)}$	CC	Address and control output hold time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)	—	ps
8	$t_{DS1(base)}$	CC	DQ and DM output setup time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
9	$t_{DH1(base)}$	CC	DQ and DM output hold time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
10	t_{DQSQ}	CC	DQS-DQ skew for DQS and associated DQ inputs[2]	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps

1 Measured with clock pin loaded with differential 100 Ω termination resistor.

2 All transitions measured at mid-supply ($V_{DD\_MEM\_IO}$/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

Figure 22 shows the DDR SDRAM write timing.

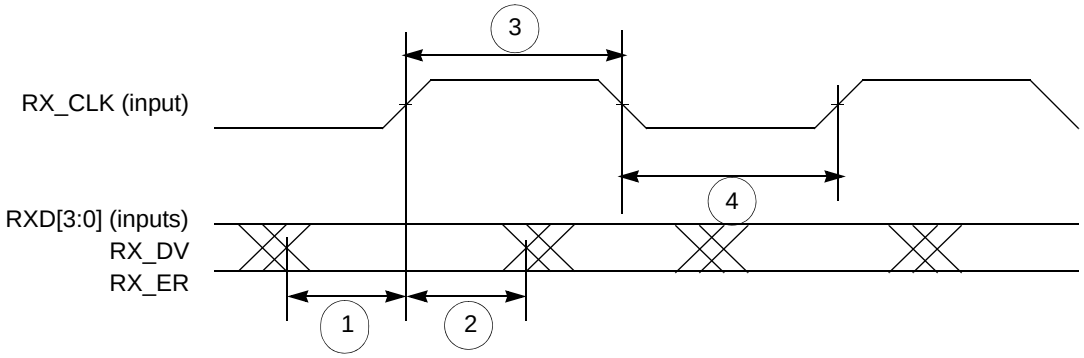

Figure 45. MII receive signal timing diagram

3.22.8.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed two times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 73. MII transmit signal timing[1]

No.	Parameter	Min	Max	Unit
5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
7	TX_CLK pulse width high	40%	60%	TX_CLK period
8	TX_CLK pulse width low	40%	60%	TX_CLK period

1 Output pads configured with SRC = 0b11.

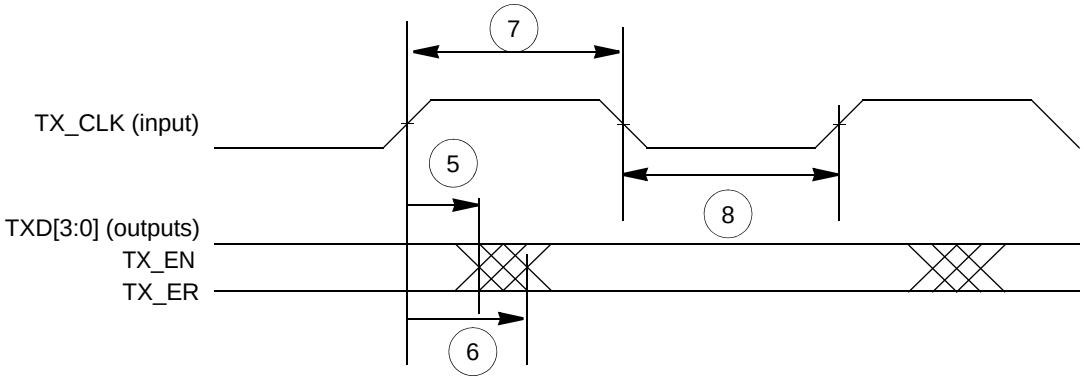

Figure 46. MII transmit signal timing diagram

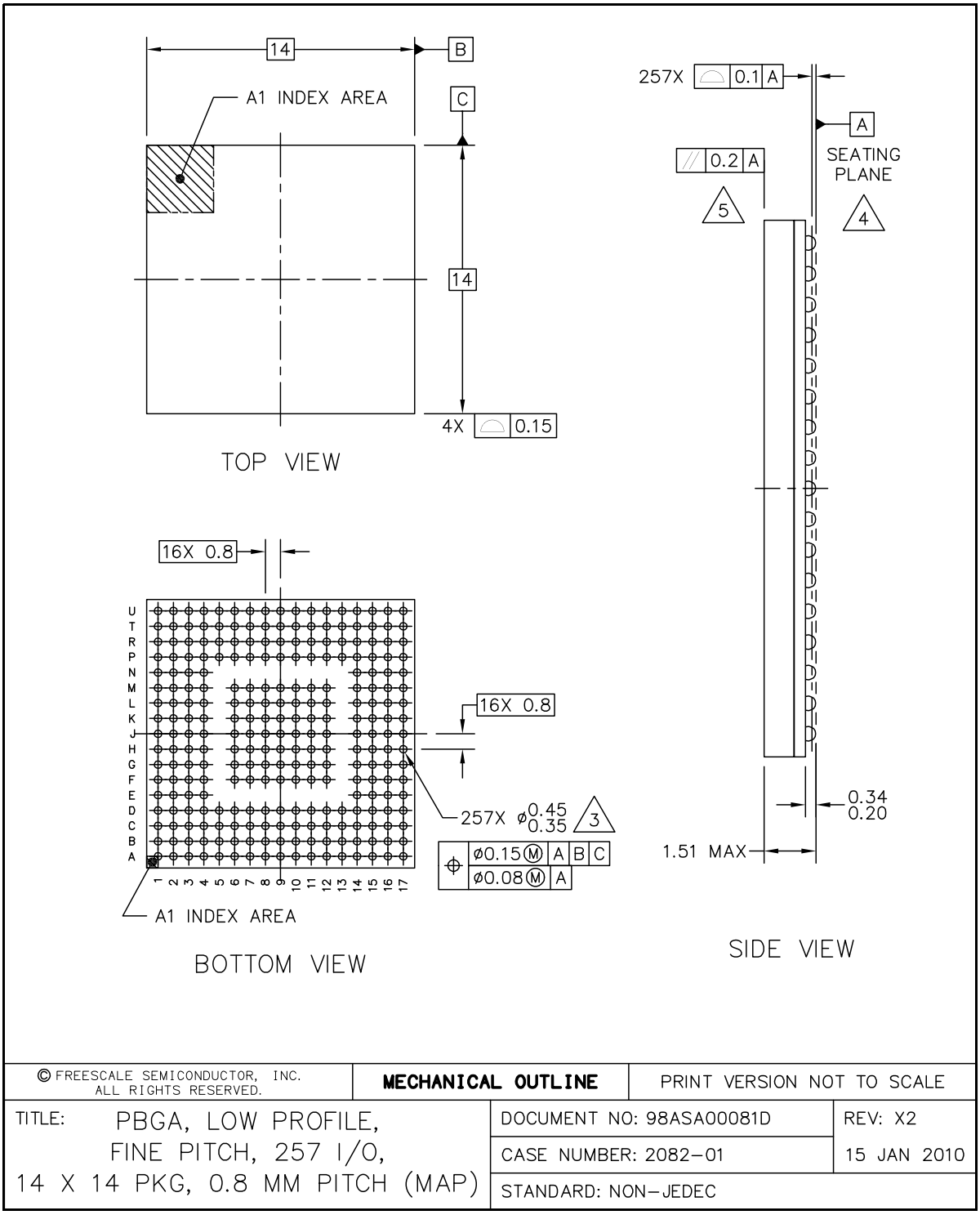

Figure 54. 257 MAPBGA mechanical data (1 of 2)

Table 79. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.2, Absolute maximum ratings, Table 11 (Absolute maximum ratings), • Deleted footnote to the Max value "Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined." • Added footnote to $V_{DD\_HV\_DRAM}$: "As the $V_{DD\_HV\_DRAM\_VREF}$ supply should always be constrained by the $V_{DD\_HV\_DRAM}$ supply for example through a voltage divider network per the JEDEC specification, the maximum ratings for the $V_{DD\_HV\_DRAM}$ supply should be used for the $V_{DD\_HV\_DRAM\_VREF}$ reference as well." • Changed absolute max rating for $V_{DD\_LV\_PLL}$ from 1.4 to 1.32. • Added footnote to Min value of T_{STG}: "If the ambient temperature is at or above the minimum storage temperature and below the recommended minimum operating temperature, power may be applied to the device safely. However, functionality is not guaranteed and a power cycle must be administered if in internal regulation mode or an assertion of RESET_SUP_B must be administered if in external regulation mode once device enters into the recommended operating temperature range." In Section 3.3, Recommended operating conditions, Table 12 (Recommended operating conditions), • For T_A and T_J, added footnote "When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition." • For T_A, changed the Max temperature spec for the 257 package from 105 to 125 and deleted footnote: "Preliminary data." In Section 3.8.1, PMC electrical specifications, Table 17 (PMC electrical specifications), • No. 4 LvdC and No. 5 HvdC threshold were specified as rising edge and hysteresis. The specification is changed to rising edge / falling edge. • Removed No. 6, VddStepC, and renumbered subsequent lines. In Section 3.9, Supply current characteristics, Table 19 (Current consumption characteristics), added a footnote to No. 3. Idd_HV_FLA. "The current specified for Idd_HV_FLA includes current consumed during programming and erase operations." In Section 3.12, FMPLL electrical characteristics, Table 22 (FMPLL electrical characteristics), replaced "f_{sys}" with "$f_{FMPLLOUT}$" in rows for C_{JITTER}, f_{LCK}, f_{UL}, f_{CS}/f_{DS}, and footnote 9. In Section 3.14.1, Input impedance and ADC accuracy: • Changed "C_S being substantially a switched capacitance..." to "C_S and C_{P2} being substantially a switched capacitance..." • Changed "and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, ..." to "and the sum of $R_S + R_F$, ..." • Changed the equation $$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ to $$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ • Added new spec after line 3 for $t_{ADC\_S\_PMC}$, C: Parameter: Sample time of internal PMC channels. Conditions: - , Min : 717, Typ : - , Max : - , Unit : nS. In Section 3.17.1, GP pads DC specifications, Table 33 (GP pads DC electrical characteristics), added new spec for "Input pad capacitance", No. 21.