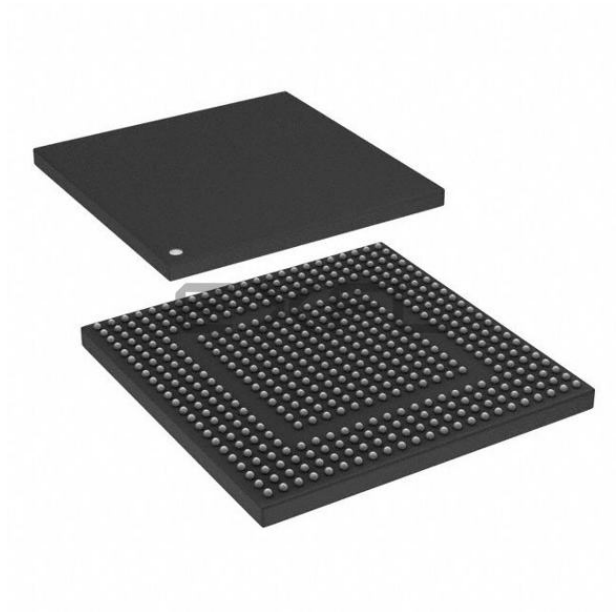

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kf0mms2

1.3 Device comparison

Table 1. MPC5675K family device comparison

Features		MPC5673K	MPC5674K	MPC5675K
CPU	Type	2 × e200z7d (SoR[1]) in lock-step or decoupled operation		
	Architecture	Harvard		
	Execution speed	0–150 MHz (+2% FM)	0–180 MHz (+2% FM)	0–180 MHz (+2% FM)
	Nominal platform frequency (in 1:1, 1:2, and 1:3 modes)	0–75 MHz (+2% FM)	0–90 MHz (+2% FM)	0–90 MHz (+2% FM)
	MMU	64 entries (SoR)		
	Instruction set PPC	Yes		
	Instruction set VLE	Yes		
	Instruction cache	16 KB, 4-way with EDC (SoR)		
	Data cache	16 KB, 4-way with Parity (SoR)		
	MPU	Yes (SoR)		
Buses	Core bus	32-bit address, 64-bit data		
	Internal periphery bus	32-bit address, 32-bit data		
XBAR	Master × slave ports	Yes (SoR)		
Memory	Static RAM (SRAM)	256 KB (ECC)	384 KB (ECC)	512 KB (ECC)
	Code flash memory	1 MB[2] (ECC)	1.5 MB[2] (ECC)	2 MB[2] (ECC)
	Data flash memory	64 KB[2] (ECC)		
Modules	Analog-to-Digital Converter (ADC)	257 pin pkg: 4 × 12 bit (22 external channels) 473 pin pkg: 4 × 12 bit (up to 34 external channels)		
	CRC unit	2 (3 contexts each)		
	Cross Triggering Unit (CTU)	2 modules		
	Deserial Serial Peripheral Interface (DSPI)	2 modules (3 chip selects)[3]	3 modules[4]	
	Digital I/Os	≥ 16		
	DRAM Controller (DRAMC)	No	Yes[5]	
	Enhanced Direct Memory Access (eDMA)	2 modules, 32 channels each		
	eTimer	3 modules, 6 channels each		

Table 1. MPC5675K family device comparison (continued)

Features		MPC5673K	MPC5674K	MPC5675K
Modules (cont.)	External Bus Interface (EBI)	1 module[5] 16-bit Data + Address or 32-bit Data with Address bus muxed[8]		
	Fast Ethernet Controller (FEC)	1 module		
	Fault Collection and Control Unit (FCCU)	1 module		
	FlexCAN	4 modules (32 message buffers each)		
	FlexPWM	3 modules (each 4 × 3 channels)		
	FlexRay	Optional		
	I^2C	2 modules[6]	3 modules	
	Interrupt Controller (INTC)	Yes (SoR)		
	LINFlex	3 modules[7]	4 modules	
	Parallel Data Interface (PDI)	1 module[8]		
	Periodic Interrupt Timer (PIT)	1 module, 4 channels		
	Software Watchdog Timer (SWT)	Yes (SoR)		
	System Timer Module (STM)	Yes (SoR)		
	Temperature sensor	1 module		
	Wakeup Unit (WKPU)	Yes		
	Crossbar switch (XBAR)	3 modules, 2 are user-configurable		
Clocking	Clock monitor unit (CMU)	3 modules		
	Frequency-modulated phase-locked loop (FMPLL)	2 modules (system and auxiliary)		
	IRCOSC – 16 MHz	1		
	XOSC 4–40 MHz	1		
Supply	Power management unit (PMU)	Yes		
	1.2 V low-voltage detector (LVD12)	1		
	1.2 V high-voltage detector (HVD12)	1		
	2.7 V low-voltage detector (LVD27)	4		
Debug	Nexus	Class 3+ (for cores and SRAM ports)		

1.5 Feature list

- High-performance e200z7d dual core
  - 32-bit Power Architecture® technology CPU
  - Up to 180 MHz core frequency
  - Dual-issue core
  - Variable length encoding (VLE)
  - Memory management unit (MMU) with 64 entries
  - 16 KB instruction cache and 16 KB data cache
- Memory available
  - Up to 2 MB code flash memory with ECC
  - 64 KB data flash memory with ECC
  - Up to 512 KB on-chip SRAM with ECC
- SIL3/ASILD innovative safety concept: LockStep mode and fail-safe protection
  - Sphere of replication (SoR) for key components
  - Redundancy checking units on outputs of the SoR connected to FCCU
  - Fault collection and control unit (FCCU)
  - Boot-time built-in self-test for memory (MBIST) and logic (LBIST) triggered by hardware
  - Boot-time built-in self-test for ADC and flash memory
  - Replicated safety-enhanced watchdog timer
  - Silicon substrate (die) temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) units
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority interrupt controller
- GPIOs individually programmable as input, output, or special function
- 3 general-purpose eTimer units (6 channels each)
- 3 FlexPWM units with four 16-bit channels per module
- Communications interfaces
  - 4 LINFlex modules
  - 3 DSPI modules with automatic chip select generation
  - 4 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1) with dual channel, up to 128 message objects and up to 10 Mbit/s
  - Fast Ethernet Controller (FEC)
  - 3 I^2C modules
- Four 12-bit analog-to-digital converters (ADCs)
  - 22 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADC conversion with timer and PWM
- External bus interface
- 16-bit external DDR memory controller
- Parallel digital interface (PDI)

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
D13	VDD_HV_FLA	VDD_HV	V6	VDD_LV_COR	VDD_LV
V1	VDD_HV_OSC	VDD_HV	V7	VDD_LV_COR	VDD_LV
D16	VDD_HV_PDI	VDD_HV	V8	VDD_LV_COR	VDD_LV
D20	VDD_HV_PDI	VDD_HV	V9	VDD_LV_COR	VDD_LV
AC17	VDD_HV_PMU	VDD_HV	V10	VDD_LV_COR	VDD_LV
F6	VDD_LV_COR	VDD_LV	V11	VDD_LV_COR	VDD_LV
F7	VDD_LV_COR	VDD_LV	V12	VDD_LV_COR	VDD_LV
F8	VDD_LV_COR	VDD_LV	V13	VDD_LV_COR	VDD_LV
F9	VDD_LV_COR	VDD_LV	V14	VDD_LV_COR	VDD_LV
F10	VDD_LV_COR	VDD_LV	V15	VDD_LV_COR	VDD_LV
F11	VDD_LV_COR	VDD_LV	V16	VDD_LV_COR	VDD_LV
F12	VDD_LV_COR	VDD_LV	V17	VDD_LV_COR	VDD_LV
F13	VDD_LV_COR	VDD_LV	V18	VDD_LV_COR	VDD_LV
F14	VDD_LV_COR	VDD_LV	Y4	VDD_LV_PLL	VDD_LV
V_{SS}					
A2	VSS_HV_IO	VSS_HV	L7	VSS_LV_COR	VSS_LV
A22	VSS_HV_IO	VSS_HV	L8	VSS_LV_COR	VSS_LV
A23	VSS_HV_IO	VSS_HV	L9	VSS_LV_COR	VSS_LV
B1	VSS_HV_IO	VSS_HV	L10	VSS_LV_COR	VSS_LV
B2	VSS_HV_IO	VSS_HV	L11	VSS_LV_COR	VSS_LV
B14	VSS_HV_IO	VSS_HV	L12	VSS_LV_COR	VSS_LV
B23	VSS_HV_IO	VSS_HV	L13	VSS_LV_COR	VSS_LV
C3	VSS_HV_IO	VSS_HV	L14	VSS_LV_COR	VSS_LV
D9	VSS_HV_IO	VSS_HV	L15	VSS_LV_COR	VSS_LV
D11	VSS_HV_IO	VSS_HV	L16	VSS_LV_COR	VSS_LV
H2	VSS_HV_IO	VSS_HV	L17	VSS_LV_COR	VSS_LV
K20	VSS_HV_IO	VSS_HV	M7	VSS_LV_COR	VSS_LV
L4	VSS_HV_IO	VSS_HV	M8	VSS_LV_COR	VSS_LV
N2	VSS_HV_IO	VSS_HV	M9	VSS_LV_COR	VSS_LV
A1	VSS_HV_IO	VSS_HV	M10	VSS_LV_COR	VSS_LV
R4	VSS_HV_IO	VSS_HV	M11	VSS_LV_COR	VSS_LV
W2	VSS_HV_IO	VSS_HV	M12	VSS_LV_COR	VSS_LV
Y12	VSS_HV_IO	VSS_HV	M13	VSS_LV_COR	VSS_LV
AA3	VSS_HV_IO	VSS_HV	M14	VSS_LV_COR	VSS_LV

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
R4	GPIO	dspi1 CS3	A0: siul_GPIO[55] A1: dspi1_CS3 A2: lin2_TXD A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R5	ANA	adc2 AN[0]	—	siul_GPI[221]	AN: adc2_AN[0]	—	Analog	VDD_HV_ADR02
R6	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR02
R8	ANA	adc2_adc3 AN[14]	—	siul_GPI[228]	AN: adc2_adc3_AN[14]	—	Analog Shared	VDD_HV_ADR13
R10	ANA	adc0 AN[2]	—	siul_GPI[33]	AN: adc0_AN[2]	—	Analog	VDD_HV_ADR02
R11	ANA	adc0_adc1 AN[13]	—	siul_GPI[27]	AN: adc0_adc1_AN[13]	—	Analog Shared	VDD_HV_ADR02
R12	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR13
R14	GPIO	lin0 TXD	A0: siul_GPIO[18] A1: lin0_TXD A2: i2c0_clock A3: sscm_DEBUG[2]	I: _ I: _ I: siul_EIRQ[17]	—	disabled	GP Slow/ Medium	VDD_HV_IO
R16	GPIO	flexpwm1 A[2]	A0: siul_GPIO[164] A1: dramc_ADD[6] A2: ebi_ADD14 A3: flexpwm1_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
R17	GPIO	flexpwm1 B[2]	A0: siul_GPIO[165] A1: dramc_ADD[7] A2: ebi_ADD15 A3: flexpwm1_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
T3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO
T4	ANA	adc3 AN[0]	—	siul_GPI[229]	AN: adc3_AN[0]	—	Analog	VDD_HV_ADR13
T5	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	Analog	VDD_HV_ADR13
T6	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR02
T8	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR02
T10	ANA	adc0 AN[1]	—	siul_GPI[24] etimer0_ETC[5]	AN: adc0_AN[1]	—	Analog	VDD_HV_ADR02
T11	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR02
T12	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR13
T13	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR13
T14	GPIO	lin0 RXD	A0: siul_GPIO[19] A1: _ A2: i2c0_data A3: sscm_DEBUG[3]	I: lin0_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
G1	GPIO	nexus MCKO	A0: siul_GPIO[87] A1: _ A2: npc_wrapper_MCKO A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G3	GPIO	nexus MDO[8][1]	A0: siul_GPIO[111] A1: _ A2: npc_wrapper_MDO[8] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G4	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G20	GPIO	siul GPIO[196]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_AD30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
G21	GPIO	dramc DQS[0]	A0: siul_GPIO[190] A1: dramc_DQS[0] A2: ebi_AD24 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G22	GPIO	dramc DM[0]	A0: siul_GPIO[192] A1: dramc_DM[0] A2: ebi_AD26 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G23	GPIO	dramc D[7]	A0: siul_GPIO[181] A1: dramc_D[7] A2: ebi_AD15 A3: ebi_ADD31	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
H1	GPIO	nexus EVTO_B	A0: siul_GPIO[90] A1: _ A2: npc_wrapper_EVTO_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
H3	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
Y22	GPIO	dramc ADD[11]	A0: siul_GPIO[169] A1: dramc_ADD[11] A2: ebi_AD3 A3: ebi_ADD19	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
Y23	GPIO	dramc ADD[5]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AA4	GPIO	dspi1 CS3	A0: siul_GPIO[55] A1: dspi1_CS3 A2: lin2_TXD A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA5	GPIO	flexpwm1 X[1]	A0: siul_GPIO[119] A1: flexpwm1_X[1] A2: etimer2_ETC[1] A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA6	ANA	adc3 AN[1]	—	siul_GPI[230]	AN: adc3_AN[1]	—	Analog	VDD_HV_ADR23
AA7	ANA	adc2_adc3 AN[12]	—	siul_GPI[226]	AN: adc2_adc3_AN[12]	—	Analog Shared	VDD_HV_ADR23
AA8	ANA	adc2 AN[0]	—	siul_GPI[221]	AN: adc2_AN[0]	—	Analog	VDD_HV_ADR23
AA11	ANA	adc0 AN[2]	—	siul_GPI[33]	AN: adc0_AN[2]	—	Analog	VDD_HV_ADR0
AA12	ANA	adc0 AN[5]	—	siul_GPI[66]	AN: adc0_AN[5]	—	Analog	VDD_HV_ADR0
AA13	ANA	adc0 AN[8]	—	siul_GPI[69]	AN: adc0_AN[8]	—	Analog	VDD_HV_ADR0

Table 12. Recommended operating conditions (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	0	0	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	3.0	3.63	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	0	0	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	3.0	3.63	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	0	0	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	3.0	3.63	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	0	0	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	1.62	3.63	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	0	0	V
11	$V_{DD\_HV\_DRAM}$	SR	DRAM interface supply voltage	—	1.62	3.63	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	0	0	V
13	$V_{DD\_HV\_ADRx}$	SR	ADC*x* high reference voltage[1]	—	3.0	3.63	V
				Alternate input voltage	4.5	5.5	
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	0	0	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	3.0	3.63	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	0	0	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic[2]	External VREG mode	1.14	1.32	V
17a		CC		Internal VREG Mode	1.14	1.32	V
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	0	0	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage[2]	External VREG mode	1.14	1.32	V
19a		CC		Internal VREG Mode	1.14	1.32	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	0	0	V
21	T_A	SR	Ambient temperature under bias[3,4]	257 MAPBGA	–40	125	°C
				473 MAPBGA	–40	125	°C
22	T_J	SR	Junction temperature under bias[4]	257 MAPBGA	–40	150	°C
				473 MAPBGA	–40	150	

1 If this supply is not above its absolute minimum recommended operating level, LBIST operations can fail.

2 The jitter specifications for both PLLs holds true only up to 50 mV noise (peak to peak) on $V_{DD\_LV\_COR}$ and $V_{DD\_LV\_PLL}$.

3 See Table 1 for available frequency and package options.

4 When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition.

Table 23. RC oscillator electrical characteristics (continued)

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
3	$\Delta_{IRCTRIM}$	CC	Internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1 PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature.

3.14 ADC electrical characteristics

The MPC5675K provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

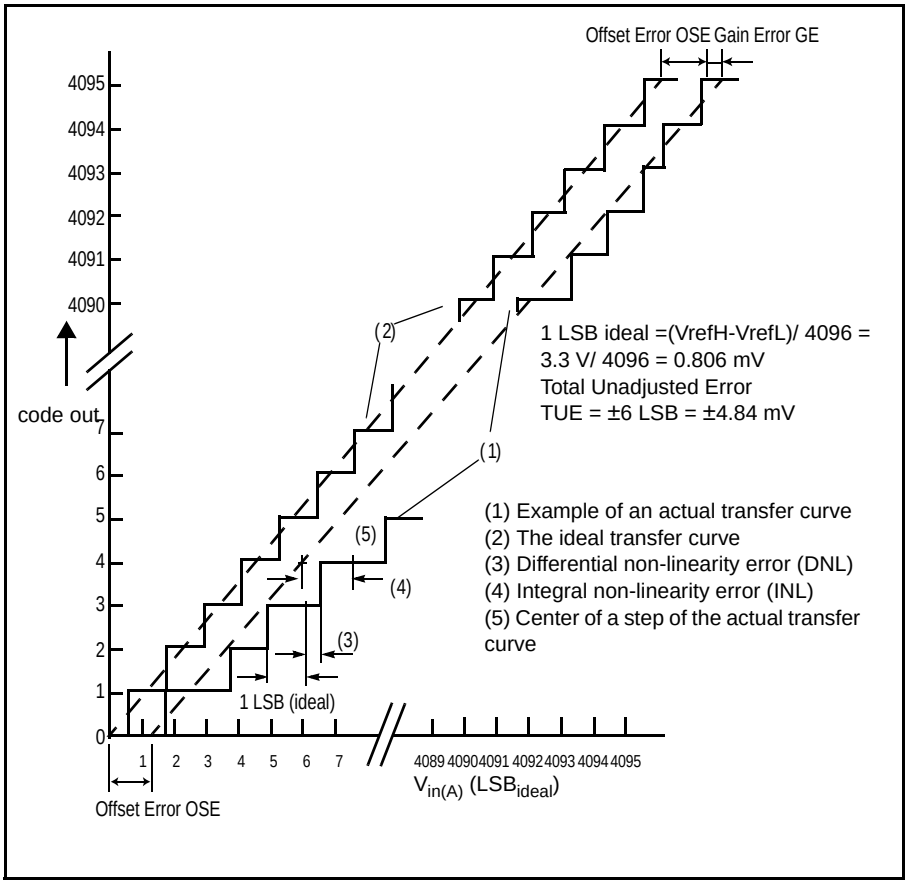

Figure 8. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

Table 33. GP pads DC electrical characteristics[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
12	I_{PU}	CC	Equivalent pullup current	$V_{IN} = V_{IL}$	–130	—	—	µA
				$V_{IN} = V_{IH}$	—	—	–10	
13	I_{PD}	CC	Equivalent pulldown current	$V_{IN} = V_{IL}$	10	—	—	µA
				$V_{IN} = V_{IH}$	—	—	130	
14	I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 150 °C	-1	—	1	µA
		P	Input leakage current (All single ADC channels)[3]	T_A = –40 to 150 °C	-0.25	—	0.25	µA
		P	Input leakage current (All shared ADC channels)	T_A = –40 to 150 °C	-0.3	—	0.3	µA
16	V_{ILR}	SR	$\overline{\text{RESET}}$, low level input voltage	—	–0.4[2]	—	0.35 $V_{DD\_HV\_IO}$	V
17	V_{IHR}	SR	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$+0.4[2]	V
18	V_{HYSR}	CC	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	—	V
19	V_{OLR}	CC	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
20	I_{PD}	CC	$\overline{\text{RESET}}$, equivalent pulldown current	$V_{IN} = V_{IL}$	10	—	—	µA
				$V_{IN} = V_{IH}$	—	—	130	
21	C_{IN}	D	Input pad capacitance	—	—	—	3	pF
22	V_{ILRSB}	SR	Reset Sup B, Low level input voltage	—	-0.1[2]	—	0.30 VDD_HV_IO	V
23	V_{IHRSB}	SR	Reset Sup B, High level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.1[2]	V

1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.

2 "SR" parameter values must not exceed the absolute maximum ratings shown in Table 11.

3 Specified values are applicable to all modes of the pad, i.e., IBE = 0/1 and/or APC = 0/1.

3.17.2 GP pads AC specifications

Table 34. GP pads AC electrical characteristics[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200

Table 34. GP pads AC electrical characteristics[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	7	—	40	50
		1	—	6	3	—	12	—	—	40	7	—	40	100
		1	—	6	5	—	18	—	—	25	7	—	40	200
4	Symmetric	1	—	8	1	—	5	—	—	50	3	—	25	25
5	Pullup/down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

3.17.3 I/O pad current specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated based on the voltage, frequency, and load on the pin.

Table 35. I/O pad current specifications

Pad Type	Load (pF)	Frequency (MHz)	VDD_HV_IO (V)	Current (mA)
GP Slow/Medium	20	4	3.6	0.30
GP Slow/Symmetric	20	10	3.6	0.76
GP Slow/Fast	20	45	3.6	3.40
GP Slow	20	0.5	3.6	0.04

3.17.4 Power Sequence Pin States for GPIO Pads

Table 36. Power sequence pin states for GPIO pads

VDD_LV_COR	VDD_HV_IO	Pad Function
Low	Low	Outputs Disabled
Low	High	Outputs Disabled
High	Low	Outputs Disabled

Table 52. Output drive current @ V_{DDE} = 1.8 V (±100 mV)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
2	DRAM DQ	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
3	DRAM CLK	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 53. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	
2	DRAM DQ	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	

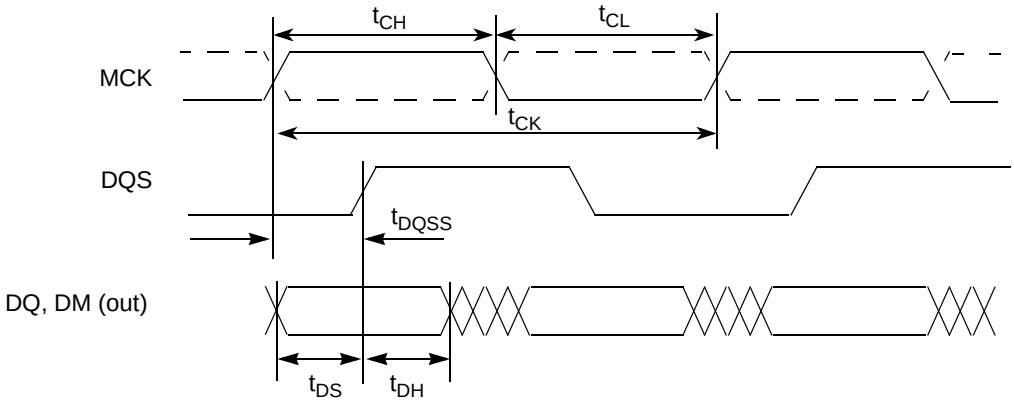

Figure 22. DDR write timing

Figure 23 and Figure 24 show the DDR SDRAM read timing.

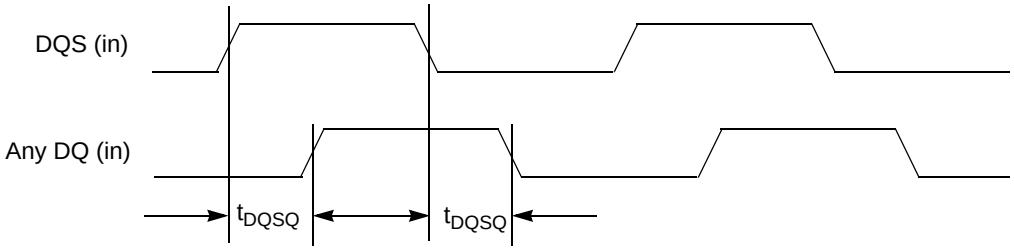

Figure 23. DDR read timing, DQ vs. DQS

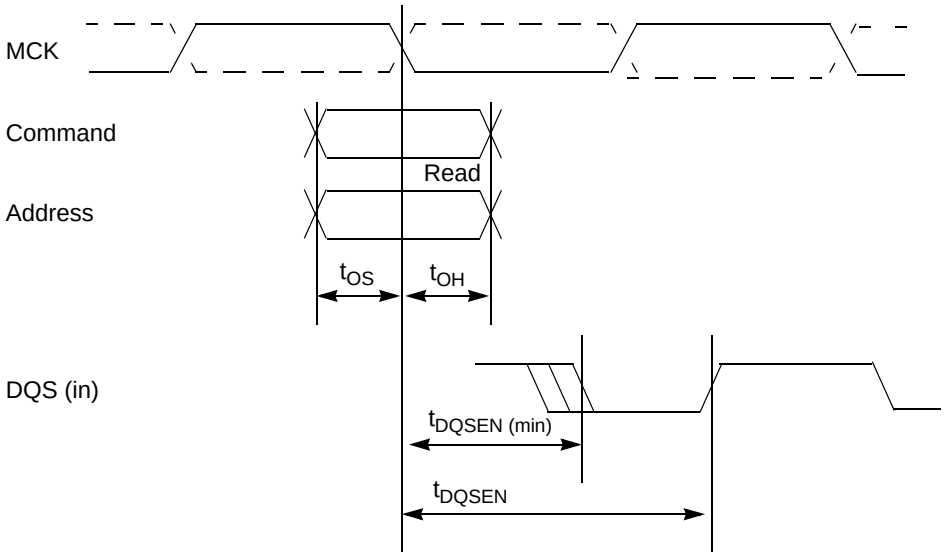

Figure 24. DDR read timing, DQSEN

Figure 25 provides the AC test load for the DDR bus.

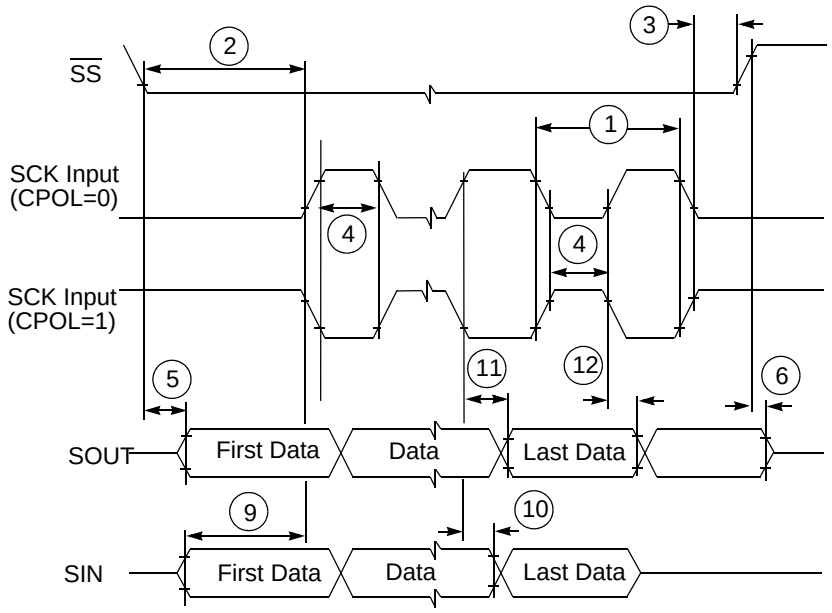

Figure 39. DSPI modified transfer format timing—slave, CPHA = 0

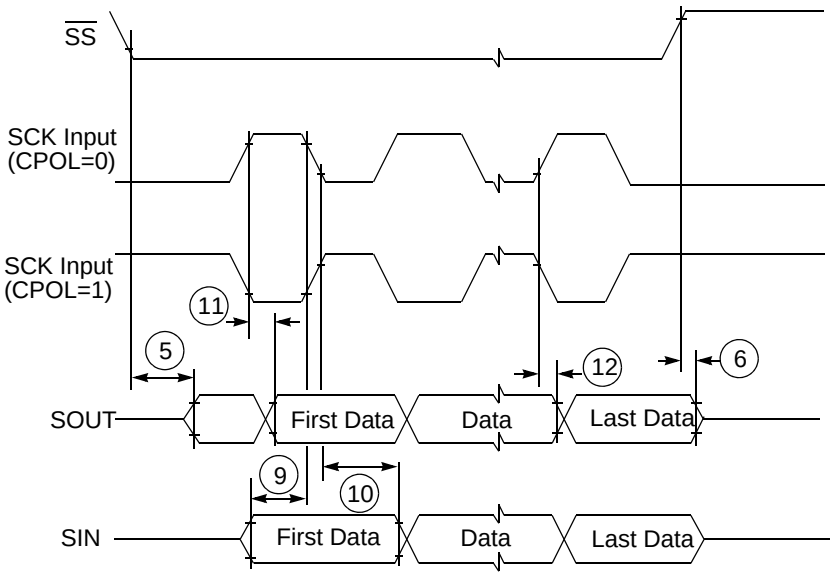

Figure 40. DSPI modified transfer format timing—slave, CPHA = 1

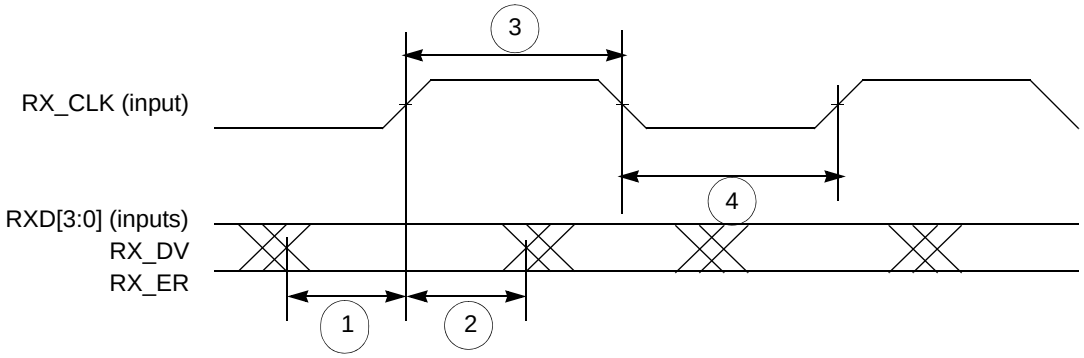

Figure 45. MII receive signal timing diagram

3.22.8.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed two times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 73. MII transmit signal timing[1]

No.	Parameter	Min	Max	Unit
5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
7	TX_CLK pulse width high	40%	60%	TX_CLK period
8	TX_CLK pulse width low	40%	60%	TX_CLK period

1 Output pads configured with SRC = 0b11.

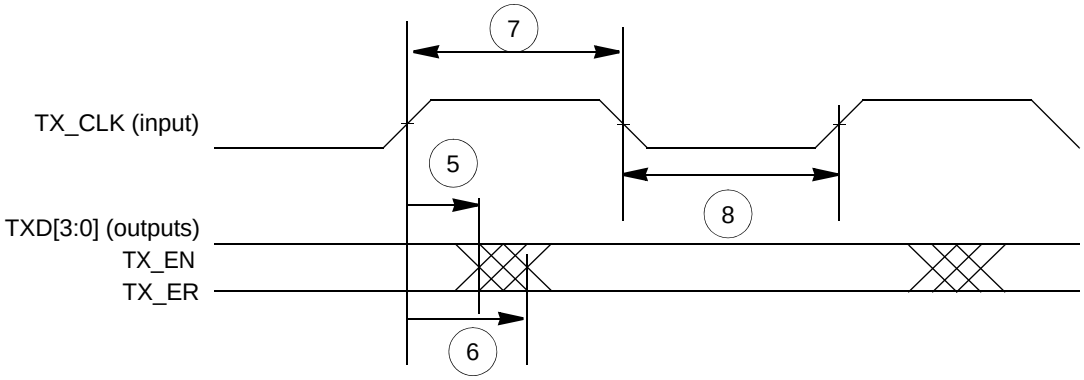

Figure 46. MII transmit signal timing diagram

3.22.10 I²C timing

Table 77. I²C SCL and SDA input timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	D	Start condition hold time	2	—	IP bus cycle[1]
2	—	D	Clock low time	8	—	IP bus cycle[1]
3	—	D	Data hold time	0.0	—	ns
4	—	D	Clock high time	4	—	IP bus cycle[1]
5	—	D	Data setup time	0.0	—	ns
6	—	D	Start condition setup time (for repeated start condition only)	2	—	IP bus cycle[1]
7	—	D	Stop condition setup time	2	—	IP bus cycle[1]

1 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

Table 78. I²C SCL and SDA output timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1[1]	—	D	Start condition hold time	6	—	IP bus cycle[2]
2[1]	—	D	Clock low time	10	—	IP bus cycle[1]
3[3]	—	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	D	Data hold time	7	—	IP bus cycle[1]
5[1]	—	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	D	Clock high time	10	—	IP bus cycle[1]
7[1]	—	D	Data setup time	2	—	IP bus cycle[1]
8[1]	—	D	Start condition setup time (for repeated start condition only)	20	—	IP bus cycle[1]
9[1]	—	D	Stop condition setup time	10	—	IP bus cycle[1]

1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

3 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values.

4.1.2 473 MAPBGA

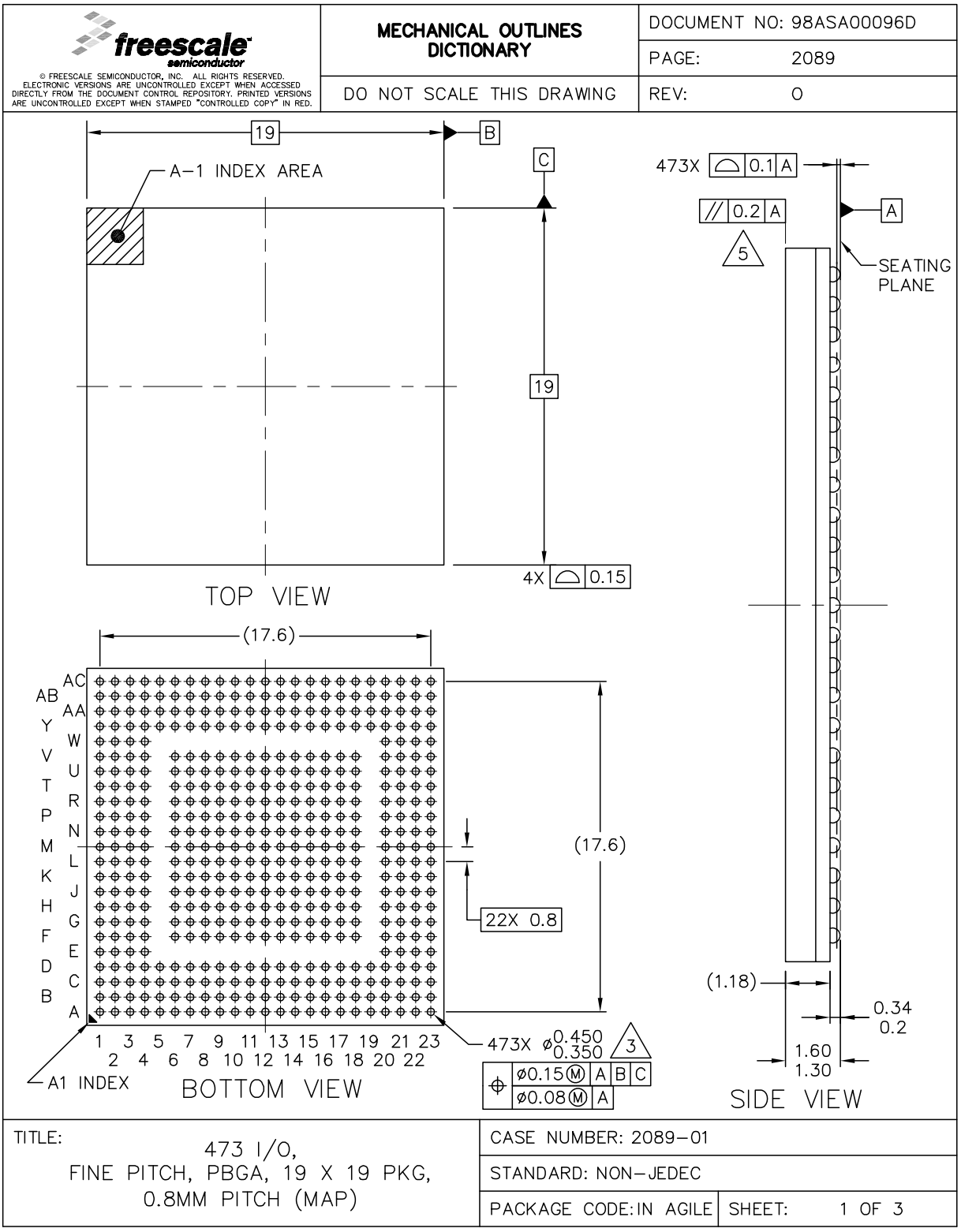

Figure 56. 473 MAPBGA package mechanical data (1 of 3)

Table 79. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.2, Absolute maximum ratings, Table 11 (Absolute maximum ratings), • Deleted footnote to the Max value "Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined." • Added footnote to $V_{DD\_HV\_DRAM}$: "As the $V_{DD\_HV\_DRAM\_VREF}$ supply should always be constrained by the $V_{DD\_HV\_DRAM}$ supply for example through a voltage divider network per the JEDEC specification, the maximum ratings for the $V_{DD\_HV\_DRAM}$ supply should be used for the $V_{DD\_HV\_DRAM\_VREF}$ reference as well." • Changed absolute max rating for $V_{DD\_LV\_PLL}$ from 1.4 to 1.32. • Added footnote to Min value of T_{STG}: "If the ambient temperature is at or above the minimum storage temperature and below the recommended minimum operating temperature, power may be applied to the device safely. However, functionality is not guaranteed and a power cycle must be administered if in internal regulation mode or an assertion of RESET_SUP_B must be administered if in external regulation mode once device enters into the recommended operating temperature range." In Section 3.3, Recommended operating conditions, Table 12 (Recommended operating conditions), • For T_A and T_J, added footnote "When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition." • For T_A, changed the Max temperature spec for the 257 package from 105 to 125 and deleted footnote: "Preliminary data." In Section 3.8.1, PMC electrical specifications, Table 17 (PMC electrical specifications), • No. 4 LvdC and No. 5 HvdC threshold were specified as rising edge and hysteresis. The specification is changed to rising edge / falling edge. • Removed No. 6, VddStepC, and renumbered subsequent lines. In Section 3.9, Supply current characteristics, Table 19 (Current consumption characteristics), added a footnote to No. 3. Idd_HV_FLA. "The current specified for Idd_HV_FLA includes current consumed during programming and erase operations." In Section 3.12, FMPLL electrical characteristics, Table 22 (FMPLL electrical characteristics), replaced "f_{sys}" with "$f_{FMPLLOUT}$" in rows for C_{JITTER}, f_{LCK}, f_{UL}, f_{CS}/f_{DS}, and footnote 9. In Section 3.14.1, Input impedance and ADC accuracy: • Changed "C_S being substantially a switched capacitance..." to "C_S and C_{P2} being substantially a switched capacitance..." • Changed "and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, ..." to "and the sum of $R_S + R_F$, ..." • Changed the equation $$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ to $$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ • Added new spec after line 3 for $t_{ADC\_S\_PMC}$, C: Parameter: Sample time of internal PMC channels. Conditions: - , Min : 717, Typ : - , Max : - , Unit : nS. In Section 3.17.1, GP pads DC specifications, Table 33 (GP pads DC electrical characteristics), added new spec for "Input pad capacitance", No. 21.

Revision	Date	Description of Changes
8 (Contd..)	29 October 2013	In Table 58 (RESET sequences), changed min values of T_{DRB} and T_{ERLB} from 60 to 50 ms and typ values from 65 to 60 ms. In Table 62 (JTAG pin AC electrical characteristics), updated the footnote to - "$f_{TCK} = 1/t_{TCK}$. f_{TCK} must not exceed 1/4 the frequency of the system clock (SYS_CLK)." Reverted the first term of Equation 11.