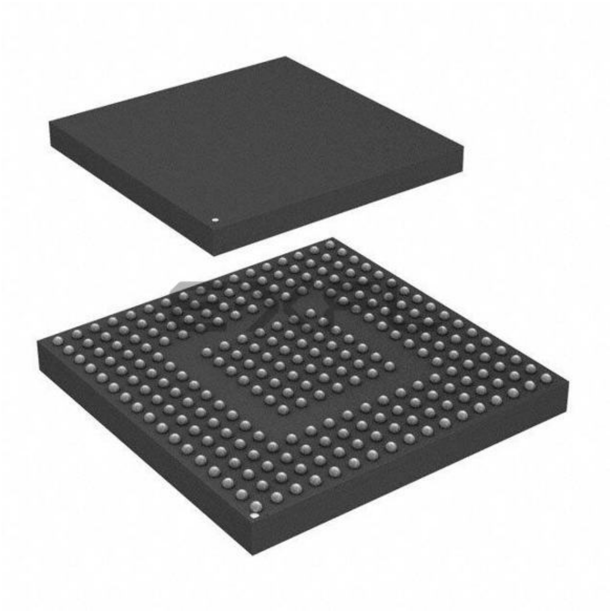
NXP USA Inc. - SPC5675KFAVMM2 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kfavmm2

N	flexpwm0 A[0]	VSS_HV_IO	flexpwm0 X[1]	flexpwm0 B[2]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR
P	flexpwm0 B[0]	flexpwm0 B[1]	flexpwm0 A[2]	flexpwm0 A[3]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR
R	flexpwm0 X[2]	flexpwm0 X[3]	flexpwm0 A[1]	VSS_HV_IO		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR
T	flexpwm0 B[3]	flexpwm1 A[0]	flexpwm1 A[1]	VDD_HV_IO		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR
U	flexpwm1 B[0]	flexpwm1 B[1]	flexpwm1 A[2]	dspi2 SCK		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR
V	VDD_HV_OSC	VDD_HV_IO	flexpwm1 B[2]	dspi1 CS2		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR
W	XTALIN	VSS_HV_IO	dspi0 CS3	VSS_LV_PLL								
Y	VSS_HV_OSC	$\overline{\text{RESET}}$	dspi0 CS2	VDD_LV_PLL	flexpwm1 X[0]	adc3 AN[0]	adc2_adc3 AN[11]	adc2_adc3 AN[14]	etimer1 ETC[1]	etimer1 ETC[2]	etimer1 ETC[3]	VSS_HV_IO
AA	XTALOUT	FCCU_F[0]	VSS_HV_IO	dspi1 CS3	flexpwm1 X[1]	adc3 AN[1]	adc2_adc3 AN[12]	adc2 AN[0]	VDD_HV_ADV	VSS_HV_ADV	adc0 AN[2]	adc0 AN[5]
AB	VSS_HV_IO	VDD_HV_IO	dspi2 SOUT	flexpwm1 X[2]	flexpwm1 X[3]	adc3 AN[2]	adc2_adc3 AN[13]	adc2 AN[1]	adc2 AN[2]	adc0 AN[0]	adc0 AN[4]	adc0 AN[6]
AC	VSS_HV_IO	VSS_HV_IO	dspi2 SIN	flexpwm1 A[3]	flexpwm1 B[3]	adc3 AN[3]	VDD_HV_ADR_23	VSS_HV_ADR_23	adc2 AN[3]	adc0 AN[1]	adc0 AN[3]	VDD_HV_ADR_0
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 4. MPC5675K 473 MAPBGA pinout (southwest, viewed from above)

13	14	15	16	17	18	19	20	21	22	23	
fec TXD[3]	VDD_HV_IO	pdi DATA[3]	pdi DATA[1]	pdi CLOCK	pdi DATA[7]	pdi DATA[10]	pdi DATA[13]	pdi DATA[15]	VSS_HV_IO	VSS_HV_IO	A
fec TX_ER	VSS_HV_IO	pdi DATA[6]	pdi DATA[4]	pdi DATA[0]	pdi LINE_V	pdi DATA[9]	pdi DATA[14]	can0 TXD	VDD_HV_IO	VSS_HV_IO	B
fec RX_CLK	fec RXD[1]	fec COL	pdi DATA[5]	pdi DATA[2]	pdi DATA[8]	pdi DATA[12]	can0 RXD	VSS_HV_PDI	siul GPIO[197]	dramc CAS	C
VDD_HV_FLA	fec RXD[2]	fec MDC	VDD_HV_PDI	VSS_HV_PDI	pdi DATA[11]	pdi FRAME_V	VDD_HV_PDI	dramc BA[1]	siul GPIO[195]	dramc BA[0]	D
							mc_cgl clk_out	siul GPIO[149]	dramc CS0	dramc BA[2]	E
VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		dramc RAS	siul GPIO[194]	siul GPIO[148]	dramc D[5]	F
VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		siul GPIO[196]	dramc DQS[0]	dramc DM[0]	dramc D[7]	G
VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		dramc D[2]	VDD_HV_DRAM_VTT	VDD_HV_DRAM	VSS_HV_DRAM	H
VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		dramc D[0]	dramc D[1]	dramc D[3]	dramc D[6]	J
VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		VSS_HV_IO	dramc D[4]	dramc D[8]	dramc D[9]	K
VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		VDD_HV_IO	VDD_HV_DRAM_VTT	VSS_HV_DRAM	VDD_HV_DRAM	L
VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		dramc ODT	dramc WEB	dramc D[11]	dramc D[10]	M

Figure 5. MPC5675K 473 MAPBGA pinout (northeast, viewed from above)

Table 4. 257 MAPBGA pins not populated on package

E5	E6	E7	E8	E9	E10	E11	E12
E13	F5	F13	G5	G13	H5	H13	J5
J13	K5	K13	L5	L13	M5	M13	N5
N6	N7	N8	N9	N10	N11	N12	N13

Table 5. 473 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F15	VDD_LV_COR	VDD_LV
A14	VDD_HV_IO	VDD_HV	F16	VDD_LV_COR	VDD_LV
B22	VDD_HV_IO	VDD_HV	F17	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F18	VDD_LV_COR	VDD_LV
D8	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G18	VDD_LV_COR	VDD_LV
L20	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	H18	VDD_LV_COR	VDD_LV
M4	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T4	VDD_HV_IO	VDD_HV	J18	VDD_LV_COR	VDD_LV
V2	VDD_HV_IO	VDD_HV	K6	VDD_LV_COR	VDD_LV
Y13	VDD_HV_IO	VDD_HV	K18	VDD_LV_COR	VDD_LV
Y20	VDD_HV_IO	VDD_HV	L6	VDD_LV_COR	VDD_LV
AB2	VDD_HV_IO	VDD_HV	L18	VDD_LV_COR	VDD_LV
AB22	VDD_HV_IO	VDD_HV	M6	VDD_LV_COR	VDD_LV
AC12	VDD_HV_ADR_0	VDD_HV_A	M18	VDD_LV_COR	VDD_LV
AC15	VDD_HV_ADR_1	VDD_HV_A	N6	VDD_LV_COR	VDD_LV
AC7	VDD_HV_ADR_23	VDD_HV_A	N18	VDD_LV_COR	VDD_LV
AA9	VDD_HV_ADV	VDD_HV_A	P6	VDD_LV_COR	VDD_LV
H22	VDD_HV_DRAM	VDD_HV	P18	VDD_LV_COR	VDD_LV
L23	VDD_HV_DRAM	VDD_HV	R6	VDD_LV_COR	VDD_LV
P23	VDD_HV_DRAM	VDD_HV	R18	VDD_LV_COR	VDD_LV
U22	VDD_HV_DRAM	VDD_HV	T6	VDD_LV_COR	VDD_LV
R20	VDD_HV_DRAM_VREF	VDD_HV	T18	VDD_LV_COR	VDD_LV
H21	VDD_HV_DRAM_VTT	VDD_HV	U6	VDD_LV_COR	VDD_LV
L21	VDD_HV_DRAM_VTT	VDD_HV	U18	VDD_LV_COR	VDD_LV

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
H11	VSS_LV_COR	VSS_LV	R16	VSS_LV_COR	VSS_LV
H12	VSS_LV_COR	VSS_LV	R17	VSS_LV_COR	VSS_LV
H13	VSS_LV_COR	VSS_LV	T7	VSS_LV_COR	VSS_LV
H14	VSS_LV_COR	VSS_LV	T8	VSS_LV_COR	VSS_LV
H15	VSS_LV_COR	VSS_LV	T9	VSS_LV_COR	VSS_LV
H16	VSS_LV_COR	VSS_LV	T10	VSS_LV_COR	VSS_LV
H17	VSS_LV_COR	VSS_LV	T11	VSS_LV_COR	VSS_LV
J7	VSS_LV_COR	VSS_LV	T12	VSS_LV_COR	VSS_LV
J8	VSS_LV_COR	VSS_LV	T13	VSS_LV_COR	VSS_LV
J9	VSS_LV_COR	VSS_LV	T14	VSS_LV_COR	VSS_LV
J10	VSS_LV_COR	VSS_LV	T15	VSS_LV_COR	VSS_LV
J11	VSS_LV_COR	VSS_LV	T16	VSS_LV_COR	VSS_LV
J12	VSS_LV_COR	VSS_LV	T17	VSS_LV_COR	VSS_LV
J13	VSS_LV_COR	VSS_LV	U7	VSS_LV_COR	VSS_LV
J14	VSS_LV_COR	VSS_LV	U8	VSS_LV_COR	VSS_LV
J15	VSS_LV_COR	VSS_LV	U9	VSS_LV_COR	VSS_LV
J16	VSS_LV_COR	VSS_LV	U10	VSS_LV_COR	VSS_LV
J17	VSS_LV_COR	VSS_LV	U11	VSS_LV_COR	VSS_LV
K7	VSS_LV_COR	VSS_LV	U12	VSS_LV_COR	VSS_LV
K8	VSS_LV_COR	VSS_LV	U13	VSS_LV_COR	VSS_LV
K9	VSS_LV_COR	VSS_LV	U14	VSS_LV_COR	VSS_LV
K10	VSS_LV_COR	VSS_LV	U15	VSS_LV_COR	VSS_LV
K11	VSS_LV_COR	VSS_LV	U16	VSS_LV_COR	VSS_LV
K12	VSS_LV_COR	VSS_LV	U17	VSS_LV_COR	VSS_LV
K13	VSS_LV_COR	VSS_LV	W4	VSS_LV_PLL	VSS_LV
K14	VSS_LV_COR	VSS_LV	AC19	VSS_HV_PMU	VSS_LV
K15	VSS_LV_COR	VSS_LV	D5	RESERVED	VSS_HV
K16	VSS_LV_COR	VSS_LV	AB20	RESERVED	VSS_HV
K17	VSS_LV_COR	VSS_LV			

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
A13	GPIO	fec MDIO	A0: siul_GPIO[198] A1: fec_MDIO A2: _ A3: dspi2_CS0	I: _ I: _ I: siul_EIRQ[28]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A14	GPIO	fec TX_EN	A0: siul_GPIO[200] A1: fec_TX_EN A2: _ A3: lin0_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO
B4	GPIO	can1 TXD	A0: siul_GPIO[14] A1: can1_TXD A2: _ A3: _	I: _ I: _ I: siul_EIRQ[13]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B5	GPIO	nexus MDO[14][1]	A0: siul_GPIO[219] A1: _ A2: npc_wrapper_MDO[14] A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
B6	GPIO	dspi2 CS1	A0: siul_GPIO[9] A1: dspi2_CS1 A2: _ A3: _	I: flexpwm0_FAULT[0] I: lin3_RXD I: can2_RXD	—	disabled	GP Slow/ Medium	VDD_HV_IO
B7	GPIO	flexray CB_TR_EN	A0: siul_GPIO[52] A1: flexray_CB_TR_EN A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B8	GPIO	flexray CA_TX	A0: siul_GPIO[48] A1: flexray_CA_TX A2: _ A3: _	I: ctu1_EXT_IN I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
D1	GPIO	nexus MDO[2][1]	A0: siul_GPIO[85] A1: _ A2: npc_wrapper_MDO[2] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D2	GPIO	nexus MDO[3][1]	A0: siul_GPIO[84] A1: _ A2: npc_wrapper_MDO[3] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D3	GPIO	can1 RXD	A0: siul_GPIO[15] A1: _ A2: _ A3: _	I: can1_RXD I: can0_RXD I: siul_EIRQ[14]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D4	GPIO	dspi0 SOUT	A0: siul_GPIO[38] A1: dspi0_SOUT A2: _ A3: sscm_DEBUG[6]	I: _ I: _ I: siul_EIRQ[24]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D6	GPIO	etimer0 ETC[5]	A0: siul_GPIO[44] A1: etimer0_ETC[5] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D7	GPIO	etimer0 ETC[4]	A0: siul_GPIO[43] A1: etimer0_ETC[4] A2: _ A3: _	I: _ I: mc_rgm_ABS[0] I: _	—	pulldown	GP Slow/ Medium	VDD_HV_IO
D10	GPIO	fec TXD[2]	A0: siul_GPIO[203] A1: fec_TXD[2] A2: _ A3: _	I: flexpwm1_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D11	GPIO	fec TXD[1]	A0: siul_GPIO[202] A1: fec_TXD[1] A2: _ A3: dspi2_SCK	I: flexpwm1_FAULT[0] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D12	GPIO	fec RX_DV	A0: siul_GPIO[210] A1: flexray_DBG3 A2: etimer2_ETC[0] A3: dspi0_CS7	I: fec_RX_DV I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
A13	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	pdi DATA[3]	A0: siul_GPIO[134] A1: flexpwm2_X[1] A2: _ A3: _	I: pdi_DATA[3] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A16	GPIO	pdi DATA[1]	A0: siul_GPIO[132] A1: flexpwm2_B[3] A2: _ A3: _	I: pdi_DATA[1] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A17	GPIO	pdi CLOCK	A0: siul_GPIO[128] A1: flexpwm2_B[1] A2: _ A3: etimer1_ETC[3]	I: pdi_CLOCK I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A18	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A19	GPIO	pdi DATA[10]	A0: siul_GPIO[141] A1: flexpwm2_X[3] A2: _ A3: _	I: pdi_DATA[10] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A20	GPIO	pdi DATA[13]	A0: siul_GPIO[144] A1: pdi_SENS_SEL[2] A2: ctu1_EXT_TGR A3: _	I: pdi_DATA[13] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A21	GPIO	pdi DATA[15]	A0: siul_GPIO[146] A1: pdi_SENS_SEL[0] A2: i2c2_data A3: _	I: pdi_DATA[15] I: ctu1_EXT_IN I: _	—	disabled	PDI Medium	VDD_HV_PDI
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
B13	GPIO	fec TX_ER	A0: siul_GPIO[205] A1: fec_TX_ER A2: dspi2_CS3 A3: _	I: flexpwm1_FAULT[3] I: lin0_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B16	GPIO	pdi DATA[4]	A0: siul_GPIO[135] A1: flexpwm2_A[2] A2: _ A3: etimer1_ETC[4]	I: pdi_DATA[4] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B17	GPIO	pdi DATA[0]	A0: siul_GPIO[131] A1: _ A2: lin3_TXD A3: _	I: pdi_DATA[0] I: _ I: flexpwm2_FAULT[2]	—	disabled	PDI Medium	VDD_HV_PDI
B18	GPIO	pdi LINE_V	A0: siul_GPIO[129] A1: _ A2: lin2_TXD A3: _	I: pdi_LINE_V I: _ I: flexpwm2_FAULT[0]	—	disabled	PDI Medium	VDD_HV_PDI
B19	GPIO	pdi DATA[9]	A0: siul_GPIO[140] A1: flexpwm2_X[2] A2: _ A3: _	I: pdi_DATA[9] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B20	GPIO	pdi DATA[14]	A0: siul_GPIO[145] A1: pdi_SENS_SEL[1] A2: i2c2_clock A3: _	I: pdi_DATA[14] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B21	GPIO	can0 TXD	A0: siul_GPIO[16] A1: can0_TXD A2: _ A3: sscm_DEBUG[0]	I: _ I: _ I: siul_EIRQ[15]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C2	GPIO	nexus MDO[15][1]	A0: siul_GPIO[220] A1: _ A2: npc_wrapper_MDO[15] A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
C14	GPIO	fec RXD[1]	A0: siul_GPIO[212] A1: dspi1_CS1 A2: etimer2_ETC[5] A3: _	I: fec_RXD[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C15	GPIO	fec COL	A0: siul_GPIO[206] A1: fec_COL A2: _ A3: lin1_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C16	GPIO	pdi DATA[5]	A0: siul_GPIO[136] A1: flexpwm2_A[0] A2: _ A3: etimer1_ETC[0]	I: pdi_DATA[5] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C17	GPIO	pdi DATA[2]	A0: siul_GPIO[133] A1: flexpwm2_A[1] A2: _ A3: etimer1_ETC[2]	I: pdi_DATA[2] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C18	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C19	GPIO	pdi DATA[12]	A0: siul_GPIO[143] A1: _ A2: _ A3: _	I: pdi_DATA[12] I: lin3_RXD I: flexpwm2_FAULT[3]	—	disabled	PDI Medium	VDD_HV_PDI
C20	GPIO	can0 RXD	A0: siul_GPIO[17] A1: _ A2: _ A3: sscm_DEBUG[1]	I: can0_RXD I: can1_RXD I: siul_EIRQ[16]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C22	GPIO	siul GPIO[197]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_AD31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
C23	GPIO	dramc CAS	A0: siul_GPIO[152] A1: dramc_CAS A2: ebi_WE_BE_1 A3: flexpwm0_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
E23	GPIO	dramc BA[2]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F1	GPIO	nexus MDO[10][1]	A0: siul_GPIO[109] A1: _ A2: npc_wrapper_MDO[10] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F4	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F20	GPIO	dramc RAS	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F21	GPIO	siul GPIO[194]	A0: siul_GPIO[194] A1: flexpwm0_X[0] A2: ebi_AD28 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F22	GPIO	siul GPIO[148]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F23	GPIO	dramc D[5]	A0: siul_GPIO[179] A1: dramc_D[5] A2: ebi_AD13 A3: ebi_ADD29	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
G1	GPIO	nexus MCKO	A0: siul_GPIO[87] A1: _ A2: npc_wrapper_MCKO A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G3	GPIO	nexus MDO[8][1]	A0: siul_GPIO[111] A1: _ A2: npc_wrapper_MDO[8] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G4	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
G20	GPIO	siul GPIO[196]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_AD30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
G21	GPIO	dramc DQS[0]	A0: siul_GPIO[190] A1: dramc_DQS[0] A2: ebi_AD24 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G22	GPIO	dramc DM[0]	A0: siul_GPIO[192] A1: dramc_DM[0] A2: ebi_AD26 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
G23	GPIO	dramc D[7]	A0: siul_GPIO[181] A1: dramc_D[7] A2: ebi_AD15 A3: ebi_ADD31	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
H1	GPIO	nexus EVTO_B	A0: siul_GPIO[90] A1: _ A2: npc_wrapper_EVTO_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
H3	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AB15	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR1
AB16	ANA	adc1 AN[3]	—	siul_GPI[32]	AN: adc1_AN[3]	—	Analog	VDD_HV_ADR1
AB17	ANA	adc1 AN[4]	—	siul_GPI[75]	AN: adc1_AN[4]	—	Analog	VDD_HV_ADR1
AB18	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
AB21	GPIO	lin1 RXD	A0: siul_GPIO[95] A1: _ A2: i2c1_data A3: _	I: lin1_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC3	GPIO	dspi2 SIN	A0: siul_GPIO[13] A1: _ A2: _ A3: _	I: dspi2_SIN I: flexpwm0_FAULT[0] I: siul_EIRQ[12]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC4	GPIO	flexpwm1 A[3]	A0: siul_GPIO[126] A1: flexpwm1_A[3] A2: etimer2_ETC[4] A3: dspi0_CS7	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC5	GPIO	flexpwm1 B[3]	A0: siul_GPIO[127] A1: flexpwm1_B[3] A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC6	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	GP Slow/ Medium	VDD_HV_ADR23
AC9	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR23

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

The “Symbol” column of the electrical parameter and timings tables may contain an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the *input* voltage of a voltage regulator.
- “CC” identifies specifications that define normal device operation. Where available, the letters “P”, “C”, “T”, or “D” replace the letter “CC” and apply to these controller characteristics. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 11. Absolute maximum ratings[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	–0.3	5.5[2]	V
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	–0.1	0.1	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	–0.3	3.63[3,4]	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	–0.1	0.1	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	–0.3	3.63[,4]	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	–0.1	0.1	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	–0.3	3.63[,4]	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	–0.1	0.1	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	–0.3	3.63[,4]	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	–0.1	0.1	V
11	$V_{DD\_HV\_DRAM}$[5]	SR	DRAM interface supply voltage	—	–0.3	3.63[,4]	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	–0.1	0.1	V
13	$V_{DD\_HV\_ADRx}$[6]	SR	ADC*x* high reference voltage	—	–0.3	6.0	V
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	–0.1	0.1	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	–0.3	3.63[3,4]	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	–0.1	0.1	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic	—	–0.3	1.32[7]	V

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$\mathbf{T_J = T_T + (\Psi_{JT} \times P_D)} \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

See [6] to [10] in Section 6, Reference documents, for more information.

3.5 Electromagnetic interference (EMI) characteristics

3.5.1 Test Setup

Electromagnetic emission tests are performed by TEM cell [2] and via direct coupling [3] (150 Ω) measurements.

Electromagnetic immunity is measured by DPI [4].

See Section 6, Reference documents, for more information.

3.5.2 Test parameters

The following test parameters shall be used:

Table 14. EMC test parameters

Method	Frequency Range	Receiver	
		BW	Step Size
150 Ω	1 MHz to 1000 MHz	1 MHz	500 kHz
TEM			

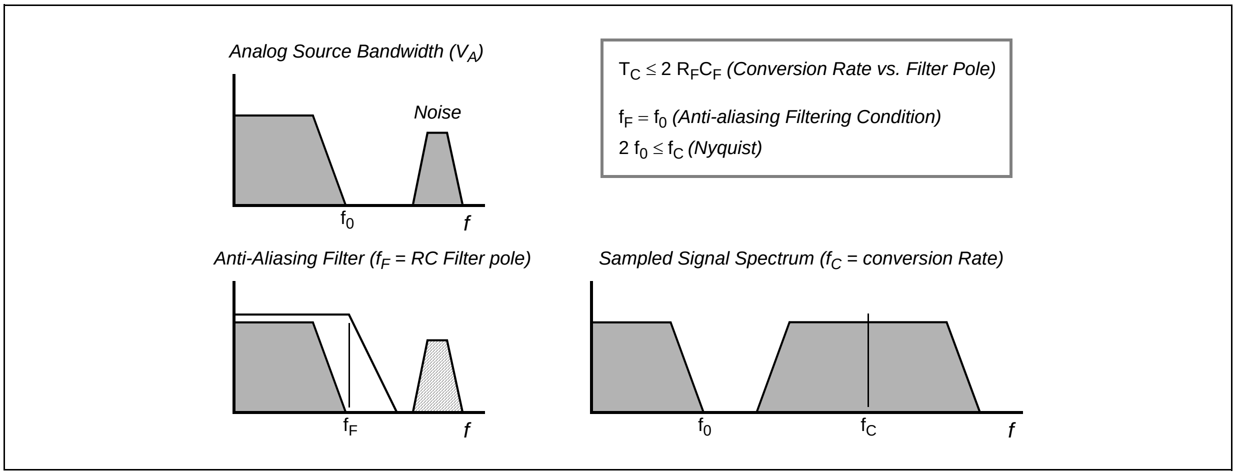


Figure 11. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

$$C_F > 8192 \bullet C_S$$

Eqn. 12

Table 24. ADC conversion characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	f_{CK}	SR	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
2	f_s	SR	Sampling frequency	—	—	—	959	kHz
3	t_{ADC_S}	D	Sample time[3]	60 MHz	383	—	—	ns
4	$t_{ADC\_S\_PMC}$	C	Sample time of internal PMC channels.	—	717	—	—	ns
5	t_{ADC_E}	P	Evaluation time[4]	60 MHz	600	—	—	ns

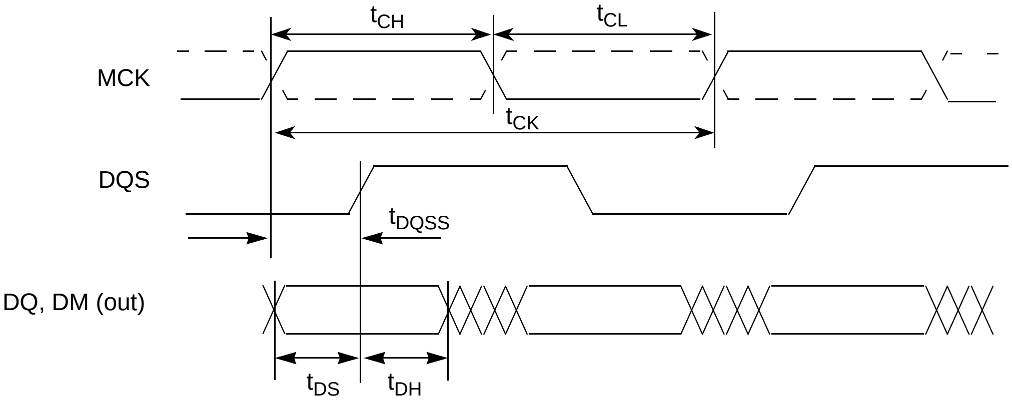


Figure 22. DDR write timing

Figure 23 and Figure 24 show the DDR SDRAM read timing.

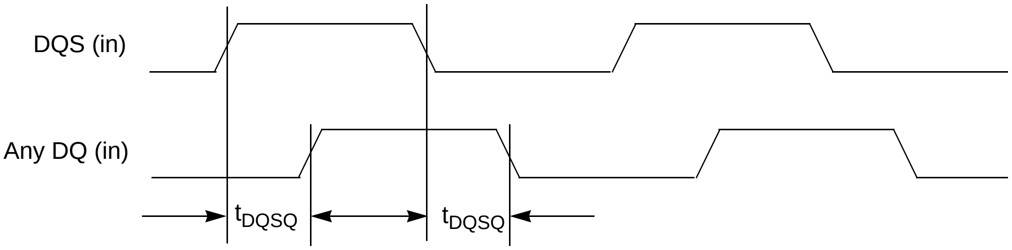


Figure 23. DDR read timing, DQ vs. DQS

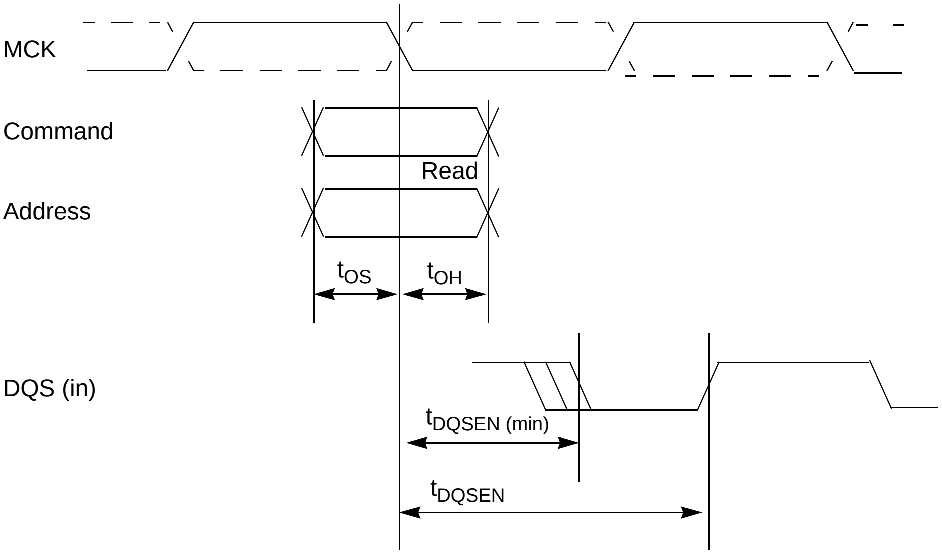


Figure 24. DDR read timing, DQSEN

Figure 25 provides the AC test load for the DDR bus.

Table 70. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
5	t_A	CC	Slave access time	$\overline{\text{SS}}$ active to SOUT valid	—	40	ns
6	t_{DIS}	CC	Slave SOUT disable time	$\overline{\text{SS}}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	CC	PCSx to $\overline{\text{PCSS}}$ time	—	13	—	ns
8	t_{PASC}	CC	$\overline{\text{PCSS}}$ to PCS*x* time	—	13	—	ns
9	t_{SUI}	CC	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	CC	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	11	
				Master (MTFE = 1, CPHA = 1)	—	5	
12	t_{HO}	CC	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	
13	t_{DT}	CC	Delay after Transfer (minimum $\overline{\text{CS}}$ negation time)	Continuous mode Non-continuos mode[2]	62 134	— —	ns

[1] Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. Note that in this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

[2] In non-continuous mode, this value is always t_{SCK} × DSPI_CTAR*n*[DT] × DSPI_CTAR*n*[PDT]. The minimum permissible value of DT is 2 and the minimum permissible value of PDT is 1. See the DSPI chapter of the *MPC5675K Reference Manual* for more information.

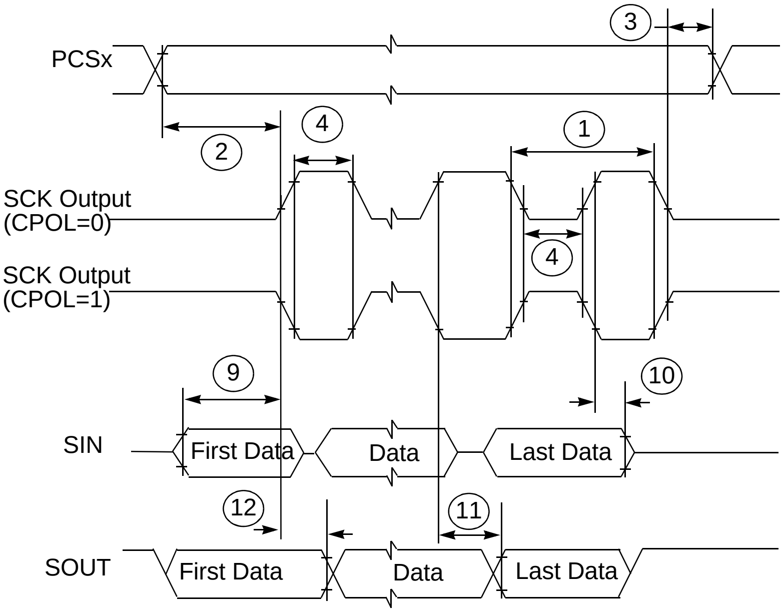


Figure 37. DSPI modified transfer format timing—master, CPHA = 0

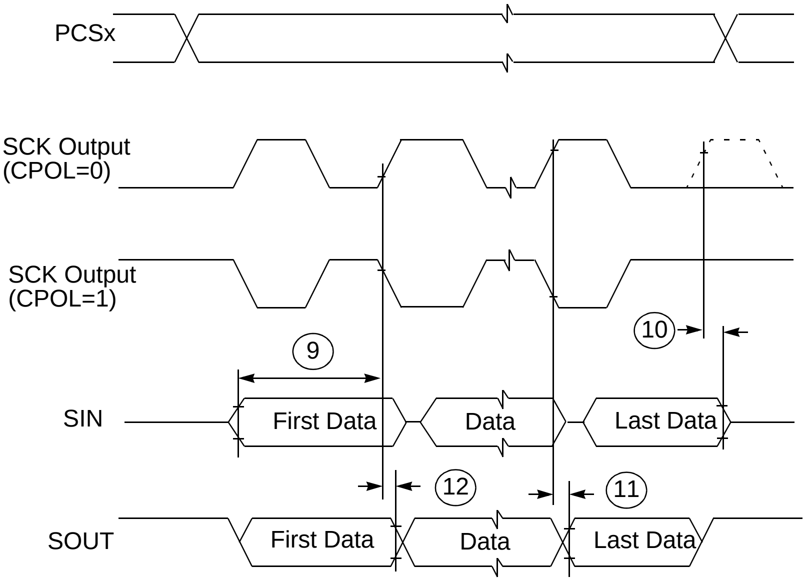


Figure 38. DSPI modified transfer format timing—master, CPHA = 1

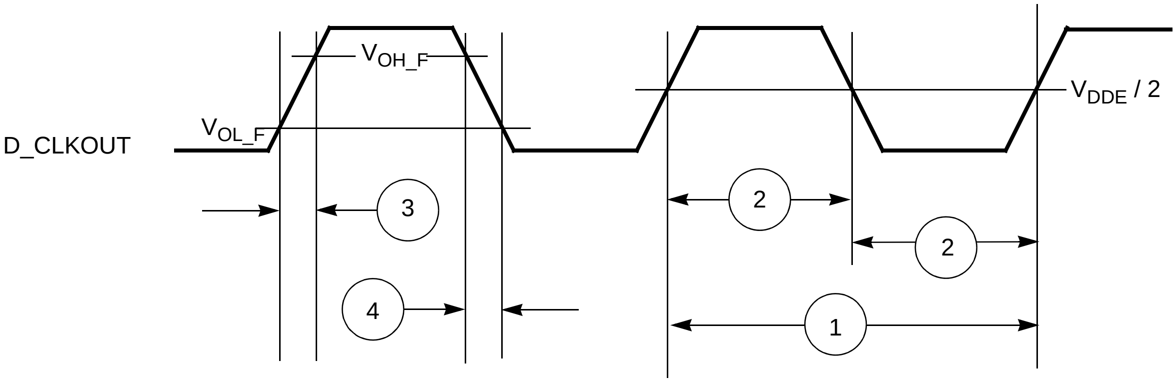


Figure 49. D_CLKOUT timing

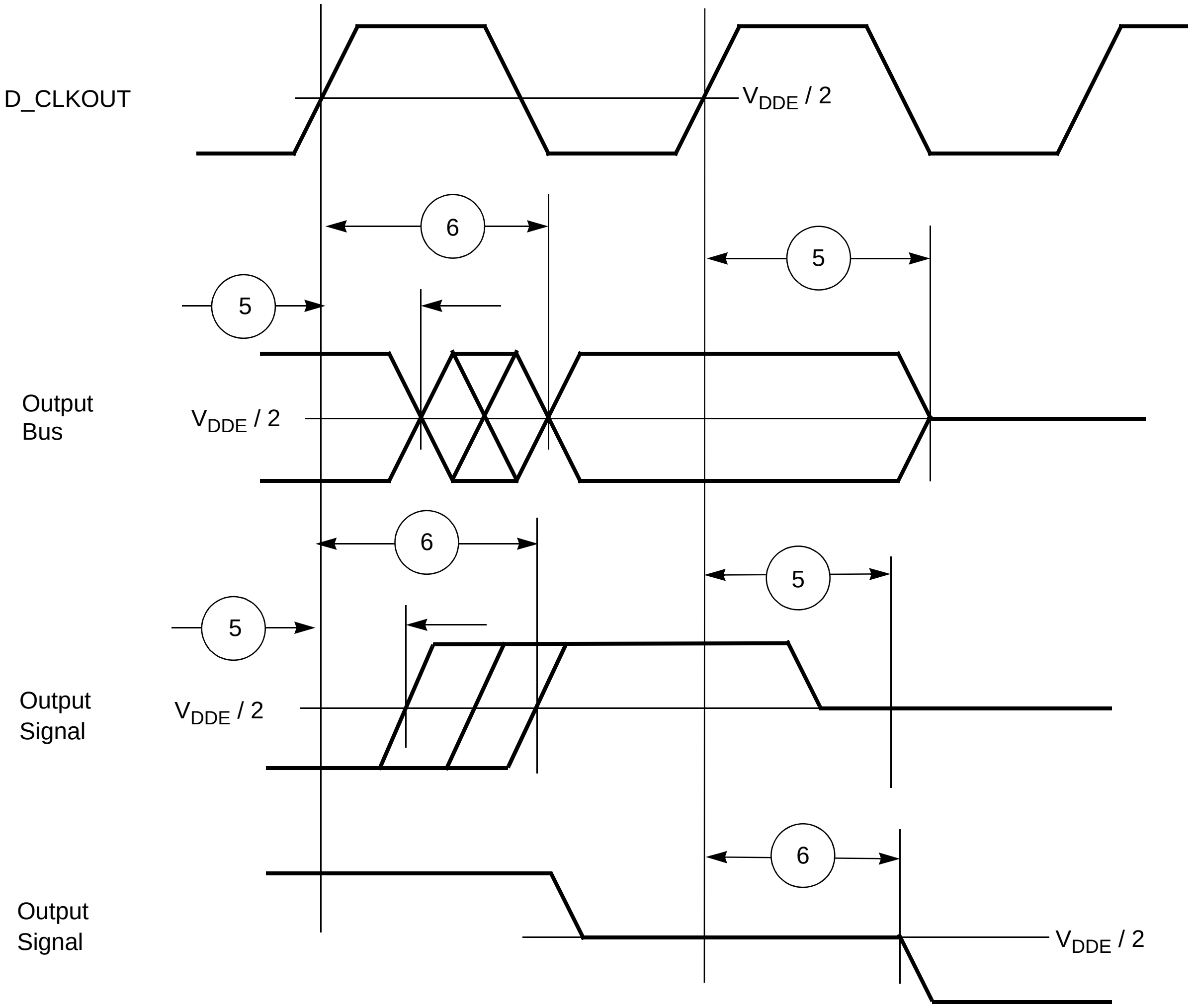
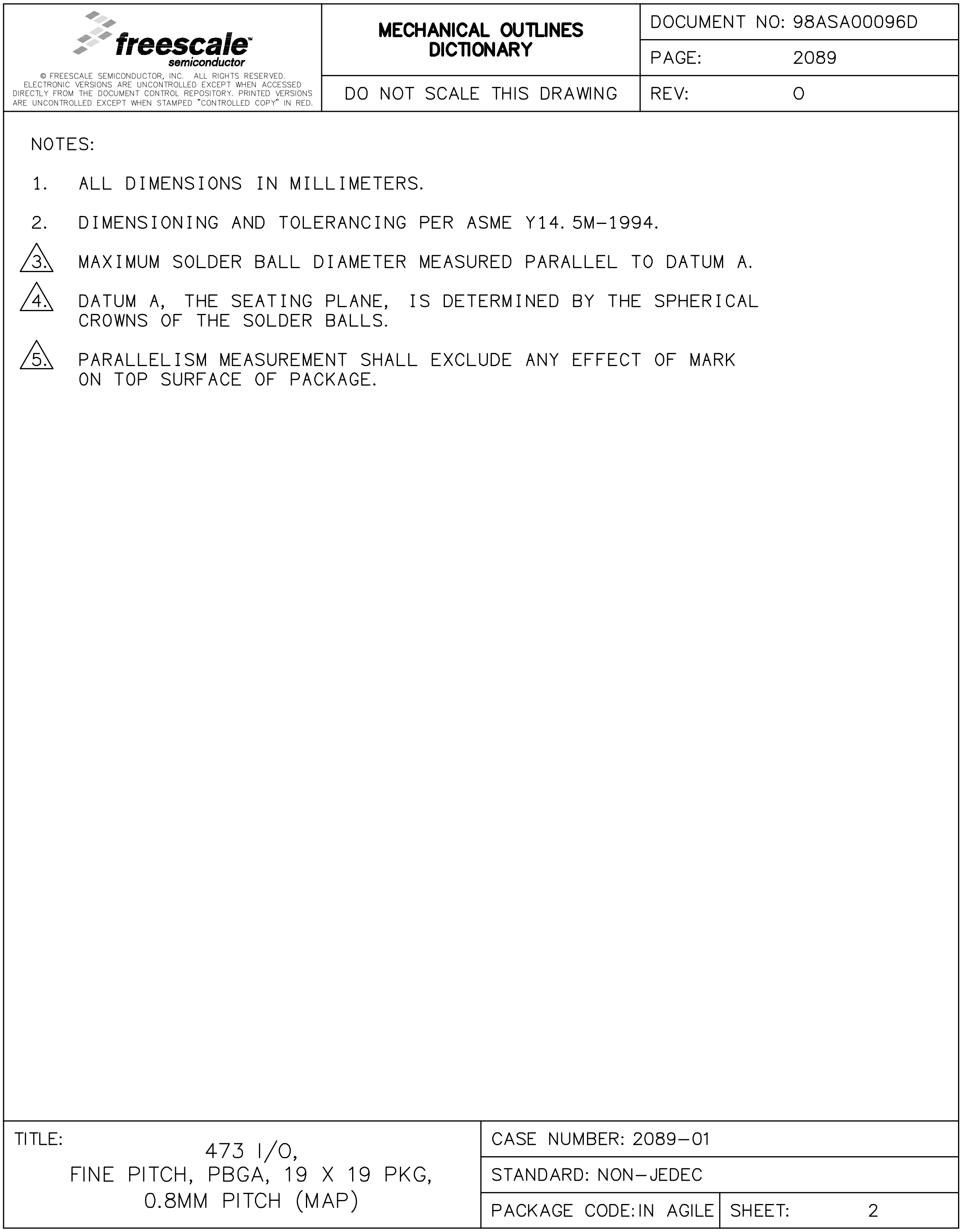


Figure 50. Synchronous output timing



freescale semiconductor © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00096D
		PAGE: 2089
	DO NOT SCALE THIS DRAWING	REV: 0

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

△3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

△4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

△5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 473 I/O, FINE PITCH, PBGA, 19 X 19 PKG, 0.8MM PITCH (MAP)	CASE NUMBER: 2089-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: IN AGILE	SHEET: 2

Figure 57. 473 MAPBGA package mechanical data (2 of 3)