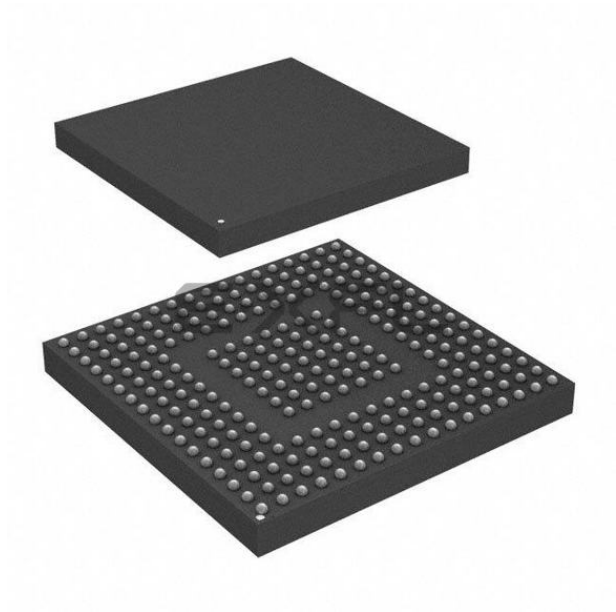

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kfavmm2r

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_ HV_IO	VSS_ HV_IO	VDD_ HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	fec RX_DV	fec MDIO	fec TX_CLK	fec TX_EN
B	VSS_ HV_IO	VSS_ HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO[14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	fec RXD[3]	fec RX_ER	fec TXD[0]	fec RXD[0]
C	VDD_ HV_IO	nexus MDO[15]	VSS_ HV_IO	FCCU_ F[1]	flexray CB_RX	etimer0 ETC[4]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	fec TXD[2]	fec TXD[1]	fec CRS
D	nexus MDO[1]	nexus MDO[3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[0]	VDD_ HV_IO	VSS_ HV_IO	JCOMP	VSS_ HV_IO	VSS_ HV_FLA
E	nexus MDO[0]	nexus MDO[2]	flexray CA_RX	NMI								
F	nexus MDO[10]	nexus MDO[11]	nexus MDO[6]	nexus MDO[4]		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
G	nexus MCKO	VDD_ HV_IO	nexus MDO[8]	nexus MSEO_B[1]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
H	nexus EVTO_B	VSS_ HV_IO	nexus MSEO_B[0]	nexus EVTI_B		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
J	nexus RDY_B	nexus MDO[13]	nexus MDO[12]	dspi1 SIN		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
K	dspi0 SCK	dspi1 CS0	dspi1 SCK	dspi1 SOUT		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
L	dspi0 CS0	dspi2 CS2	dspi2 CS0	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
M	flexpwm0 X[0]	VDD_ HV_IO	dspi0 SIN	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR

Figure 3. MPC5675K 473 MAPBGA pinout (northwest, viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12
N	flexpwm0 A[0]	VSS_ HV_IO	flexpwm0 X[1]	flexpwm0 B[2]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
P	flexpwm0 B[0]	flexpwm0 B[1]	flexpwm0 A[2]	flexpwm0 A[3]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
R	flexpwm0 X[2]	flexpwm0 X[3]	flexpwm0 A[1]	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
T	flexpwm0 B[3]	flexpwm1 A[0]	flexpwm1 A[1]	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
U	flexpwm1 B[0]	flexpwm1 B[1]	flexpwm1 A[2]	dspi2 SCK		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
V	VDD_ HV_OSC	VDD_ HV_IO	flexpwm1 B[2]	dspi1 CS2		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
W	XTALIN	VSS_ HV_IO	dspi0 CS3	VSS_ LV_PLL								
Y	VSS_ HV_OSC	$\overline{\text{RESET}}$	dspi0 CS2	VDD_ LV_PLL	flexpwm1 X[0]	adc3 AN[0]	adc2_adc3 AN[11]	adc2_adc3 AN[14]	etimer1 ETC[1]	etimer1 ETC[2]	etimer1 ETC[3]	VSS_ HV_IO
AA	XTALOUT	FCCU_ F[0]	VSS_ HV_IO	dspi1 CS3	flexpwm1 X[1]	adc3 AN[1]	adc2_adc3 AN[12]	adc2 AN[0]	VDD_ HV_ADV	VSS_ HV_ADV	adc0 AN[2]	adc0 AN[5]
AB	VSS_ HV_IO	VDD_ HV_IO	dspi2 SOUT	flexpwm1 X[2]	flexpwm1 X[3]	adc3 AN[2]	adc2_adc3 AN[13]	adc2 AN[1]	adc2 AN[2]	adc0 AN[0]	adc0 AN[4]	adc0 AN[6]
AC	VSS_ HV_IO	VSS_ HV_IO	dspi2 SIN	flexpwm1 A[3]	flexpwm1 B[3]	adc3 AN[3]	VDD_HV_ ADR_23	VSS_HV_ ADR_23	adc2 AN[3]	adc0 AN[1]	adc0 AN[3]	VDD_ HV_ADR_0

Figure 4. MPC5675K 473 MAPBGA pinout (southwest, viewed from above)

	13	14	15	16	17	18	19	20	21	22	23
A	fec TXD[3]	VDD_ HV_IO	pdi DATA[3]	pdi DATA[1]	pdi CLOCK	pdi DATA[7]	pdi DATA[10]	pdi DATA[13]	pdi DATA[15]	VSS_ HV_IO	VSS_ HV_IO
B	fec TX_ER	VSS_ HV_IO	pdi DATA[6]	pdi DATA[4]	pdi DATA[0]	pdi LINE_V	pdi DATA[9]	pdi DATA[14]	can0 TXD	VDD_ HV_IO	VSS_ HV_IO
C	fec RX_CLK	fec RXD[1]	fec COL	pdi DATA[5]	pdi DATA[2]	pdi DATA[8]	pdi DATA[12]	can0 RXD	VSS_ HV_PDI	siul GPIO[197]	dramc CAS
D	VDD_ HV_FLA	fec RXD[2]	fec MDC	VDD_ HV_PDI	VSS_ HV_PDI	pdi DATA[11]	pdi FRAME_V	VDD_ HV_PDI	dramc BA[1]	siul GPIO[195]	dramc BA[0]
E								mc_cgl clk_out	siul GPIO[149]	dramc CS0	dramc BA[2]
F	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR		dramc RAS	siul GPIO[194]	siul GPIO[148]	dramc D[5]
G	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		siul GPIO[196]	dramc DQS[0]	dramc DM[0]	dramc D[7]
H	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[2]	VDD_HV_ DRAM_VTT	VDD_HV_ DRAM	VSS_HV_ DRAM
J	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[0]	dramc D[1]	dramc D[3]	dramc D[6]
K	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VSS_ HV_IO	dramc D[4]	dramc D[8]	dramc D[9]
L	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VDD_ HV_IO	VDD_HV_ DRAM_VTT	VSS_HV_ DRAM	VDD_HV_ DRAM
M	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ODT	dramc WEB	dramc D[11]	dramc D[10]

Figure 5. MPC5675K 473 MAPBGA pinout (northeast, viewed from above)

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
P6	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P7	ANA	adc0 AN[0]	—	siul_GPI[23] lin0_RXD	AN: adc0_AN[0]		Analog	VDD_HV_ADR02
P8	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
P11	ANA	adc0_adc1 AN[14]	—	siul_GPI[28]	AN: adc0_adc1_AN[14]		Analog Shared	VDD_HV_ADR02
P12	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
P13	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
P15	GPIO	flexpwm0 A[3]	A0: siul_GPIO[153] A1: dramc_WEB A2: ebi_WE_BE_2 A3: flexpwm0_A[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P16	GPIO	flexpwm0 A[0]	A0: siul_GPIO[147] A1: dramc_CKE A2: ebi_OE A3: flexpwm0_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P17	GPIO	flexpwm1 B[1]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
T3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO
T4	ANA	adc3 AN[0]	—	siul_GPI[229]	AN: adc3_AN[0]	—	Analog	VDD_HV_ADR13
T5	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	Analog	VDD_HV_ADR13
T6	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR02
T8	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR02
T10	ANA	adc0 AN[1]	—	siul_GPI[24] etimer0_ETC[5]	AN: adc0_AN[1]	—	Analog	VDD_HV_ADR02
T11	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR02
T12	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR13
T13	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR13
T14	GPIO	lin0 RXD	A0: siul_GPIO[19] A1: _ A2: i2c0_data A3: sscm_DEBUG[3]	I: lin0_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
A13	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	pdi DATA[3]	A0: siul_GPIO[134] A1: flexpwm2_X[1] A2: _ A3: _	I: pdi_DATA[3] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A16	GPIO	pdi DATA[1]	A0: siul_GPIO[132] A1: flexpwm2_B[3] A2: _ A3: _	I: pdi_DATA[1] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A17	GPIO	pdi CLOCK	A0: siul_GPIO[128] A1: flexpwm2_B[1] A2: _ A3: etimer1_ETC[3]	I: pdi_CLOCK I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A18	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A19	GPIO	pdi DATA[10]	A0: siul_GPIO[141] A1: flexpwm2_X[3] A2: _ A3: _	I: pdi_DATA[10] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A20	GPIO	pdi DATA[13]	A0: siul_GPIO[144] A1: pdi_SENS_SEL[2] A2: ctu1_EXT_TGR A3: _	I: pdi_DATA[13] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A21	GPIO	pdi DATA[15]	A0: siul_GPIO[146] A1: pdi_SENS_SEL[0] A2: i2c2_data A3: _	I: pdi_DATA[15] I: ctu1_EXT_IN I: _	—	disabled	PDI Medium	VDD_HV_PDI
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
J23	GPIO	dramc D[6]	A0: siul_GPIO[180] A1: dramc_D[6] A2: ebi_AD14 A3: ebi_ADD30	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K1	GPIO	dspi0 SCK	A0: siul_GPIO[37] A1: dspi0_SCK A2: _ A3: sscm_DEBUG[5]	I: flexpwm0_FAULT[3] I: _ I: siul_EIRQ[23]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K2	GPIO	dspi1 CS0	A0: siul_GPIO[5] A1: dspi1_CS0 A2: _ A3: dspi0_CS7	I: _ I: _ I: siul_EIRQ[5]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K3	GPIO	dspi1 SCK	A0: siul_GPIO[6] A1: dspi1_SCK A2: _ A3: _	I: _ I: _ I: siul_EIRQ[6]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K4	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K21	GPIO	dramc D[4]	A0: siul_GPIO[178] A1: dramc_D[4] A2: ebi_AD12 A3: ebi_ADD28	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K22	GPIO	dramc D[8]	A0: siul_GPIO[182] A1: dramc_D[8] A2: ebi_AD16 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K23	GPIO	dramc D[9]	A0: siul_GPIO[183] A1: dramc_D[9] A2: ebi_AD17 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
L1	GPIO	dspi0 CS0	A0: siul_GPIO[36] A1: dspi0_CS0 A2: _ A3: sscm_DEBUG[4]	I: _ I: _ I: siul_EIRQ[22]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
Y9	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y10	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y11	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
Y14	ANA	adc0_adc1 AN[11]	—	siul_GPI[25]	AN: adc0_adc1_AN[11]	—	Analog Shared	VDD_HV_ADR0
Y15	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y16	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y17	ANA	adc1 AN[8]	—	siul_GPI[74]	AN: adc1_AN[8]	—	Analog	VDD_HV_ADR1
Y18	ANA	adc1 AN[6]	—	siul_GPI[76]	AN: adc1_AN[6]	—	Analog	VDD_HV_ADR1
Y21	GPIO	dramc ADD[15]	A0: siul_GPIO[173] A1: dramc_ADD[15] A2: ebi_AD7 A3: ebi_ADD23	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AB4	GPIO	flexpwm1 X[2]	A0: siul_GPIO[122] A1: flexpwm1_X[2] A2: etimer2_ETC[2] A3: dspi0_CS5	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AB5	GPIO	flexpwm1 X[3]	A0: siul_GPIO[125] A1: flexpwm1_X[3] A2: etimer2_ETC[3] A3: dspi0_CS6	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AB6	ANA	adc3 AN[2]	—	siul_GPI[231]	AN: adc3_AN[2]	—	Analog	VDD_HV_ADR23
AB7	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR23
AB8	ANA	adc2 AN[1]	—	siul_GPI[222]	AN: adc2_AN[1]	—	Analog	VDD_HV_ADR23
AB9	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR23
AB10	ANA	adc0 AN[0]	—	siul_GPI[23] lin0_RXD	AN: adc0_AN[0]	—	Analog	VDD_HV_ADR0
AB11	ANA	adc0 AN[4]	—	siul_GPI[70]	AN: adc0_AN[4]	—	Analog	VDD_HV_ADR0
AB12	ANA	adc0 AN[6]	—	siul_GPI[71]	AN: adc0_AN[6]	—	Analog	VDD_HV_ADR0
AB13	ANA	adc0 AN[7]	—	siul_GPI[68]	AN: adc0_AN[7]	—	Analog	VDD_HV_ADR0
AB14	ANA	adc0_adc1 AN[13]	—	siul_GPI[27]	AN: adc0_adc1_AN[13]	—	Analog Shared	VDD_HV_ADR0

In case of only narrow band disturbances the maximum of the results will not change. In case of broadband signals the emission has to be below the limits.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	750 (corners) 500	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Power Management Controller (PMC) electrical characteristics

3.8.1 PMC electrical specifications

This section contains electrical characteristics for the PMC.

Table 24. ADC conversion characteristics (continued)

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
6	C_S[5]	D	ADC input sampling capacitance	—	—	—	7.32	pF
7	C_{P1}[5]	D	ADC input pin capacitance 1	—	—	—	2.5	pF
8	C_{P2}[5]	D	ADC input pin capacitance 2	—	—	—	0.8	pF
9	R_{SW1}[5]	D	Channel selection switch resistance	V_{REF} range = 4.5 to 5.5 V	—	—	1.0	kΩ
10				V_{REF} range = 3.0 to 3.6 V	—	—	1.2	kΩ
11	R_{AD}[5]	D	Sample switching resistance	—	—	—	825	Ω
12	I_{INJ}	T	Current injection	Current injection on one ADC input channel, different from the converted one. Other parameters stay within specified limits as long as the ADC supply stays within its specified limits due to the current injection.	–3	—	3	mA
13	INL	P	Integral non linearity	—	–3	—	3	LSB
14	DNL	P	Differential non linearity[6]	—	–1.0	—	2	LSB
15	OFS	T	Offset error	—	–4	—	4	LSB
16	GNE	T	Gain error	—	–4	—	4	LSB
17	TUE[7]	P	Total unadjusted error	—	–6	—	6	LSB
18	TUE[7]	T	Total unadjusted error with current injection	—	–6	—	6	LSB
19	SNR	T	Signal-to-noise ratio	—	69	—	—	dB
20	THD	T	Total harmonic distortion	—	–72	—	—	dB
21	SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
22	ENOB	T	Effective number of bits	—	10.5	—	—	bits

1 V_{DD} = 3.3 V, T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.

2 AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

4 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.

5 See Figure 9.

6 No missing codes.

7 When operating the MPC5675K in a switched mode power supply configuration, the specifications for the ADCs under worst case conditions can be upheld only through the use of averaging back-to-back samples. In the 257 package, 10 samples must be averaged when using ADC 0, 2, or 3. In the 473 package, 5 samples must be averaged. For ADC 1, due to its close proximity to the PMC, the TUE spec must be increased to +/-10 counts, 10 samples of averaging must be used in both packages, and the VDD_HV_PMU supply must be below 3.6 V. Better performance can be obtained with lower VDD_HV_PMU supplies and higher VDD_HV_ADRx supplies. The ADC1 self test limit for the S2 algorithm needs to be modified by the user to accommodate for the increased TUE limit of +/-10 counts when operating the device in internal regulation mode. This can be accomplished by reading the current value from the test flash and subtracting 4 counts before storing the value to the ADC1 Self Test Analog Watchdog Register 2 (STAW2R).

Table 31. Data flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	—	90	MHz

3.16 SRAM memory electrical characteristics

Table 32. System SRAM memory read/write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	$s_{READ/WRITE}$	CC	Maximum frequency for system SRAM reading/writing (system clock frequency SYS_CLK)	1 wait state	90	MHz

3.17 GP pads specifications

This section specifies the electrical characteristics of the GP pads. Please refer to the tables in Section 2.2, Pin descriptions, for a cross reference between package pins and pad types.

3.17.1 GP pads DC specifications

Table 33 gives the DC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IO} < 3.6\ V$).

Table 33. GP pads DC electrical characteristics[1]

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	V_{IL}	SR	Low level input voltage	—	–0.1[2]	—	0.35 $V_{DD\_HV\_IO}$	V
2	V_{IH}	SR	High level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.1[2]	V
3	V_{HYS}	CC	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	—	V
4	V_{OL_S}	CC	Slow, low level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
5	V_{OH_S}	CC	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IO}$ – 0.8	—	—	V
6	V_{OL_M}	CC	Medium, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
7	V_{OH_M}	CC	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IO}$ – 0.8	—	—	V
8	V_{OL_F}	CC	Fast, high level output voltage	I_{OL} = 11 mA	—	—	0.5	V
9	V_{OH_F}	CC	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IO}$ – 0.8	—	—	V
10	V_{OL_SYM}	CC	Symmetric, high level output voltage	I_{OL} = 5 mA	—	—	0.5	V
11	V_{OH_SYM}	CC	Symmetric, high level output voltage	I_{OH} = –5 mA	$V_{DD\_HV\_IO}$ – 0.8	—	—	V

Table 36. Power sequence pin states for GPIO pads

VDD_LV_COR	VDD_HV_IO	Pad Function
High	High	Normal Operation

3.18 PDI pads specifications

This section specifies the electrical characteristics of the PDI pads. Please refer to the tables in Section 2.2, Pin descriptions, for a cross reference between package pins and pad types.

PDI pads feature list:

- Direction
  - Input
  - Output
  - Bidirectional
- Driver
  - Push/Pull/Open Drain
  - Configurable Four Drive Strengths on Fast driver pads
  - Configurable No Slew-Rate, Slow Slew-Rate, and Fast Slew-Rate on Slow, Medium, and SLR driver pads
  - VDD_HV_PDI NOTE: All pads are NOT 5 V TOLERANT. Pads are not capable of driving to or from voltages above their respective VDD_HV_PDI. In other words, you cannot connect a 3.3V external device to a pad supplied with 2.5 V. If a pad must be connected to a 3.3V device, its local VDD_HV_PDI must be 3.3 V. Injection current is then handled by the intrinsic diodes from the pad transistors and by the ESD diodes.
  - VDD_HV_PDI range 1.8 V to 3.3 V, as specified in the following tables
- Receiver
  - Selectable hysteresis input buffer
  - CMOS Input Buffer

The electrical data provided in this section applies:

- To the pads listed in Table 37
- Over the voltage range 1.62–3.6 V

Table 37. PDI I/O pads

No.	Name	Voltage	Used for	Notes
1	PDI Fast	1.62–3.6 V	I/O	Enhanced operating voltage range fast slew-rate output with four selectable slew-rates. Contains an input buffer and weak pullup/pulldown.
2	PDI Medium			Enhanced operating voltage range medium slew-rate output with four selectable slew-rates. Contains an input buffer and weak pullup/pulldown.

Table 38. PDI pads DC electrical characteristics[1]

No.	Symbol		Parameter	Min	Max	Unit
1	$V_{DD\_HV\_PDI}$	SR	I/O supply voltage	1.62	3.6	V
2	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis enabled)	0.65 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V
3	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis disabled)	0.58 × $V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI}$ + 0.3	V

Table 49. Output drive current @ V_{DDE} = 2.5 V (±200 mV)

Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
DRAM ACC	011	–16.2	16.2
DRAM DQ	011		
DRAM CLK	011		

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 50. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 2.5 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.5	2.5/2.4	2.1/2.1	4.3/4.1	5	011
		1.7/1.7	2.8/2.7	0.6/0.7	1.1/1.3	20	
2	DRAM DQ	1.4/1.5	2.5/2.4	2.1/2.1	4.3/4.1	5	011
		1.7/1.7	2.8/2.7	0.6/0.7	1.1/1.3	20	
3	DRAM CLK	1.4/1.4	2.4/2.4	2.1/2.1	4.4/4.1	5	011
		1.6/1.6	2.7/2.7	0.6/0.7	1.6/1.8	20	

1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19.3 DRAM pads electrical specification ($V_{DD\_HV\_DRAM}$ = 1.8 V)

Table 51. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	1.62	1.9	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	0.49 × $V_{DD\_HV\_DRAM}$	0.51 × $V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.125	—	V
5	V_{IL}	CC	Input low voltage	—	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.125	V
6	V_{OH}	CC	Output high voltage	—	1.42	—	V
7	V_{OL}	CC	Output low voltage	—	—	0.28	V

1 BGA473: Termination voltage can be supplied via package pins. BGA257 Termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT.

Table 52. Output drive current @ V_{DDE} = 1.8 V (±100 mV)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
2	DRAM DQ	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
3	DRAM CLK	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.
2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 53. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	
2	DRAM DQ	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	

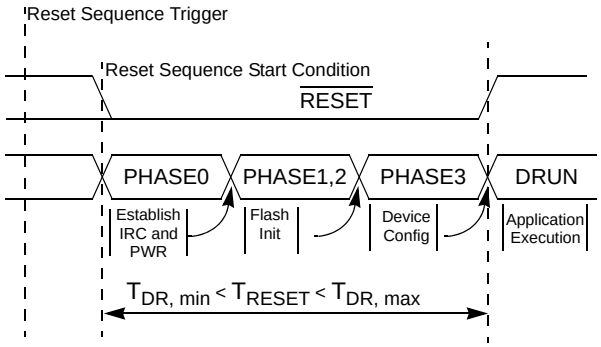

Figure 13. Destructive reset sequence, BIST disabled

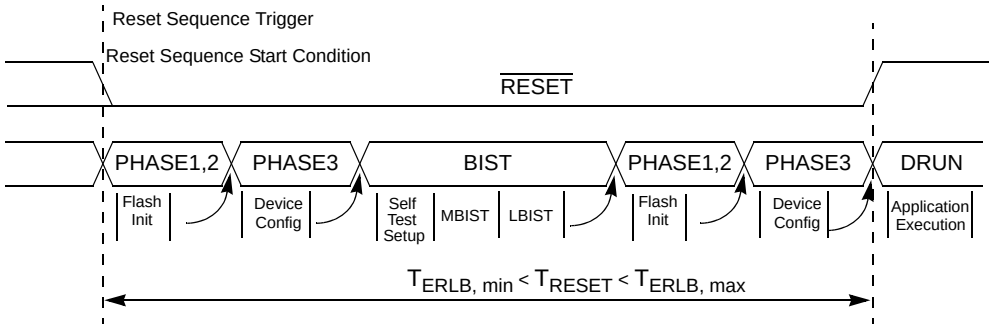

Figure 14. External reset sequence long, BIST enabled

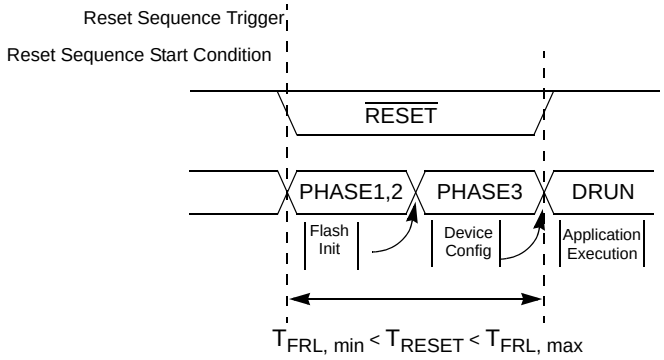

Figure 15. Functional reset sequence long

8 If $\overline{\text{RESET}}$ is configured for short reset.

9 Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.21.4 Reset sequence—start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.21.4.1 Internal VREG mode

Figure 17 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*. The last voltage rail crossing the levels shown in Figure 17 determines the start of the reset times specified in Table 58.

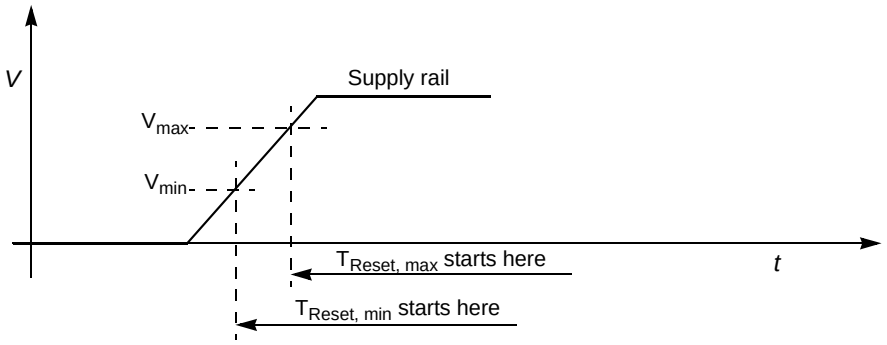

Figure 17. Reset sequence start in internal VREG mode

Table 60. Voltage thresholds

Variable name	Value
V_{min}	LvdReg – 3.5%
V_{max}	LvdReg + 3.5%
Supply Rail	VDD_HV_PMU VDD_HV_IO VDD_HV_FLASH VDD_HV_ADV

3.21.4.2 External VREG mode

Figure 18 and Figure 19 show the voltage thresholds that determine the start of the Destructive Reset Sequence, BIST enabled and the start for the Destructive Reset Sequence, BIST disabled.

NOTE

$\overline{\text{RESET\_SUP}}$ must not be released unless $V_{DD\_LV\_xxx}$ is within its valid range of operation. $\overline{\text{RESET\_SUP}}$ input circuitry needs a valid $V_{DD\_HV\_IO}$ rail in order to detect a high level on $\overline{\text{RESET\_SUP}}$.

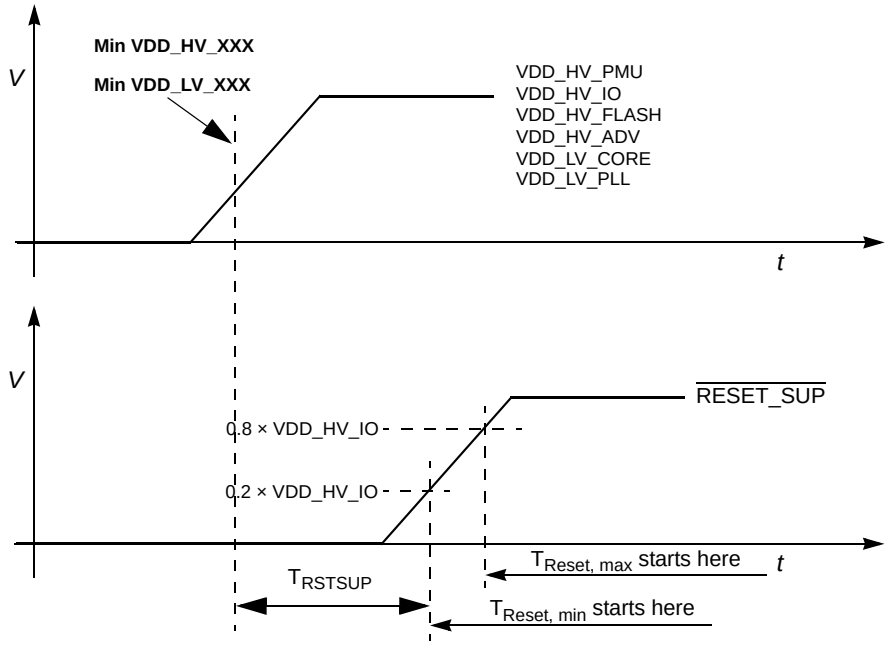

Figure 18. External VREG mode, $\overline{\text{RESET\_SUP}}$ rises after $V_{DD\_HV\_xxx}$ are stable

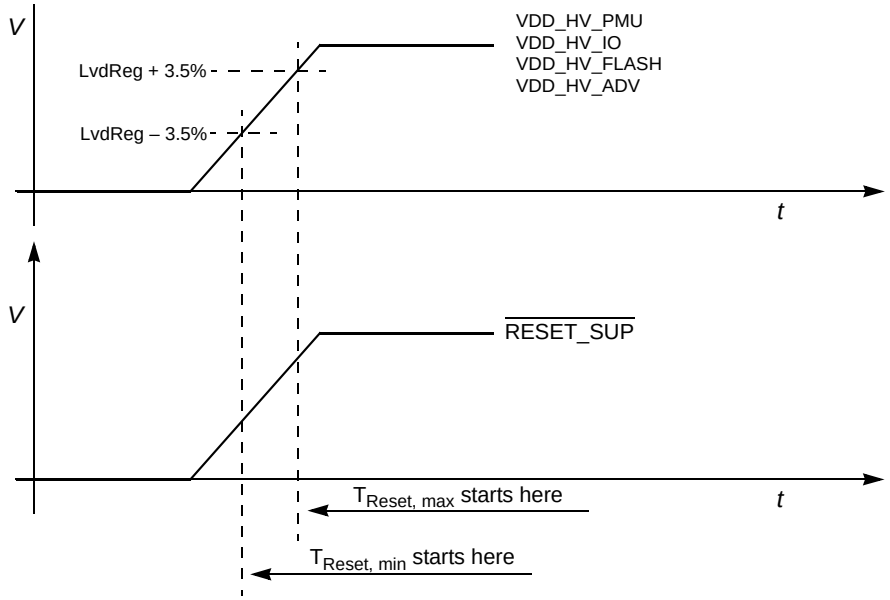

Figure 19. External VREG mode, $\overline{\text{RESET\_SUP}}$ rises with $V_{DD\_HV\_xxx}$

NOTE

In case $\overline{\text{RESET\_SUP}}$ has reached a valid high level before $V_{DD\_HV\_IO}$ is stable, the reset sequence will start as documented in Figure 19 as the $\overline{\text{RESET\_SUP}}$ input circuitry needs a valid $V_{DD\_HV\_IO}$ rail in order to detect a high level on $\overline{\text{RESET\_SUP}}$.

Table 79. Revision history (continued)

Revision	Date	Description of Changes
6 (cont.)	6 Feb 2012	In Table 68 (External interrupt timing (GPIO IRQ)): • Changed T_{IPWL} min value from TBD to 3. • Changed T_{IPWH} min value from TBD to 3. • Changed T_{ICYC} min value from TBD to 6. • Changed all units from ns to t_{CYC}. In Table 77 (I^2C SCL and SDA input timing specifications), corrected the line numbering.
6.1	30 Mar 2012	No content changes, technical or editorial, were made in this revision. Change bars are identical to those in Rev. 6. Removed the “preliminary” footers throughout. Changed “Data Sheet: Advance Information” to “Data Sheet: Technical Data” on page Removed the “product under development” disclaimer on page 1.
7	18 May 2012	Minor editorial changes and improvements throughout. In Section 1.3, Device comparison, Table 1 (MPC5675K family device comparison), • Changed the CPU/Data Cache entry from "16 KB, 4-way with EDC (SoR)" to "16 KB, 4-way with Parity (SoR)". • Added footnotes to stipulate the peripheral instances that are used on derivative devices: - Added footnote to **MPC5673K** DSPI module: “DSPI_0 and DSPI_1.“ - Added footnote to **MPC5673K** I2C module: “I2C_0 and I2C_1.“ - Added footnote to **MPC5673K** LinFlex module: “LinFlex_0, LinFlex_1, and LinFlex_2“ In Section 1.4, Block diagram: • Added missing modules (PMC, SPE2, VLE, and flash. • Added an arrow each from Core_0 and Core_1 to the XBAR modules to represent the data path. • Updated the Redundancy Checkers to reflect the actual implementation. • Renamed the “JTAG/Nexus” block to “Debug”, with JTAG and Nexus shown as submodules. In Section 1.5, Feature list, changed “Junction temperature sensor” to “Silicon substrate (die) temperature sensor”. In Section 1.6.1, High-performance e200z7d core processor and Section 1.6.9, Cache memory, removed the bullet “Supports tag and data parity" and added the following bullets: — Supports tag and data cache parity — Supports EDC for instruction cache In Section 1.6.19, System Timer Module (STM), changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)” In Section 1.6.20.2, Cross Triggering Unit (CTU), changed “DMA support with safety features” to “Supports safety measures using DMA”. In Section 1.6.21, Redundancy Control and Checker Unit (RCCU), changed “Duplicated module to guarantee highest possible diagnostic coverage (check of checker)” to “Duplicated module to enable high diagnostic coverage (check of checker)”. In Section 1.6.22, Software Watchdog Timer (SWT), • Changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)”. • Changed “Allows high level of safety (SIL3 monitor)” to “Provides measures to target high safety integrity levels (for example, SIL 3, ASIL D)”. In Section 1.6.25, Cyclic Redundancy Checker (CRC) unit, in the sentence “Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol”, changed “allow” to “support”.

Table 79. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.18, PDI pads specifications, Table 38 (PDI pads DC electrical characteristics), added footnote to table: “Over- and undershoots occurring due to impedance mismatch of the external driver and the transmission line at PDI pads in input mode can be allowed up to 0.7 V repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.” In Section 5, Orderable parts, • Removed “3 = 220 MHz” under Operating frequency heading and changed the Operating frequency of the example from “3” to “2”. • Deleted Table 73 (Orderable part number summary**)**.