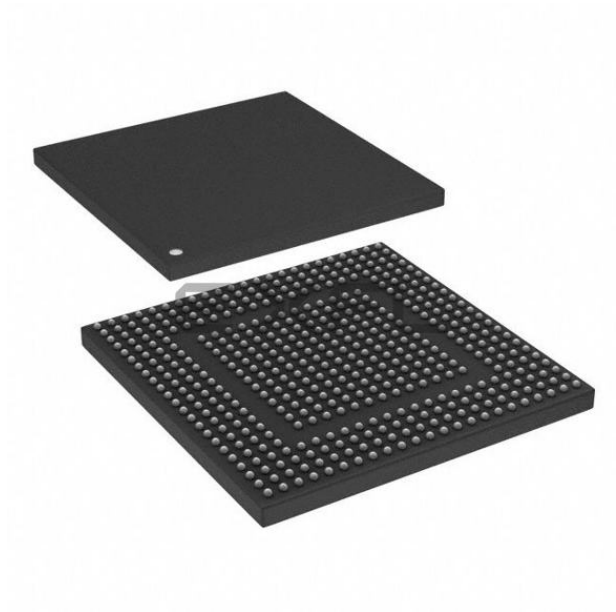

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kfavms2r

- On-chip CAN/UART bootstrap loader
- Capable of operating on a single 3.3 V voltage supply
  - 3.3 V-only modules: I/O, oscillators, flash memory
  - 3.3 V or 5 V modules: ADCs, supply to internal VREG
  - 1.8–3.3 V supply range: DRAM/PDI
- Operating junction temperature range –40 to 150 °C

1.6 Feature details

1.6.1 High-performance e200z7d core processor

- Dual 32-bit Power Architecture® processor core
- Loose or tight core coupling
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 64-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 16 KB Instruction and 16 KB Data caches per core with line locking
  - Four way set associative
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data cache parity
  - Supports EDC for instruction cache
- Vectored interrupt support
- Signal processing engine 2 (SPE2) auxiliary processing unit (APU) operating on 64-bit general purpose registers
- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single precision in hardware; double precision with software library
  - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions (except for guarded loads) do not increase interrupt latency in the MPC5675K
- To reduce latency, long cycle time instructions are aborted upon interrupt requests
- Extensive system development support through Nexus debug module

1.6.2 Crossbar Switch (XBAR)

- 32-bit address bus, 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

1.6.3 Memory Protection Unit (MPU)

Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

1.6.20.3 Analog-To-Digital Converter (ADC)

- Four independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V or 0–3.3 V
- Twenty-two single-ended input channels
- Supports eight FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal, or external triggers
- DMA and interrupt request support

1.6.20.4 eTimer module

Three 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Ability to operate up to platform frequency
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality is not in use
- DMA support

1.6.21 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to enable high diagnostic coverage (check of checker)
- Replicated IP to be used as checkers on the PBRIDGE output, Flash Controller output, SRAM output, DMA Channel Mux inputs

1.6.22 Software Watchdog Timer (SWT)

This module implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Fault-tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the MPC5675K in the 257 MAPBGA package. Figure 3, Figure 4, Figure 5, and Figure 6 show the MPC5675K in the 473 MAPBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS_HV_IO	VSS_HV_IO	VDD_HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	VDD_HV_IO	fec RXD[2]	fec RX_CLK	fec RXD[0]	fec MDIO	fec TX_EN	fec TXD[3]	VSS_HV_IO	VSS_HV_IO	A
B	VSS_HV_IO	VSS_HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO [14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	VSS_HV_IO	fec RXD[3]	fec RX_ER	fec RXD[1]	fec TX_ER	fec TX_CLK	can0 TXD	VDD_HV_IO	VSS_HV_IO	B
C	VDD_HV_IO	nexus MDO [15]	VSS_HV_IO	FCCU_F[1]	flexray CB_RX	etimer0 ETC[0]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	JCOMP	fec CRS	fec TXD[0]	fec COL	can0 RXD	VSS_HV_PDI	pdi DATA [5]	pdi CLOCK	C
D	nexus MDO [2]	nexus MDO [3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[4]	VDD_HV_FLA	VSS_HV_FLA	fec TXD[2]	fec TXD[1]	fec RX_DV	fec MDC	VDD_HV_PDI	VSS_HV_IO	pdi DATA [0]	pdi DATA [1]	D
E	nexus MDO [0]	nexus MDO [1]	flexray CA_RX	NMI										pdi LINE_V	pdi DATA [2]	pdi DATA [3]	pdi DATA [4]	E
F	nexus MDO[6]	nexus MDO [11]	dspi1 SOUT	dspi1 SIN		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		mc_cgl clk_out	pdi DATA [6]	pdi DATA [7]	pdi DATA [8]	F
G	nexus MDO [4]	VDD_HV_IO	dspi0 SCK	dspi1 SCK		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [9]	pdi DATA [10]	pdi DATA [11]	pdi FRAME_V	G
H	nexus MDO [10]	VSS_HV_IO	dspi0 CS0	dspi1 CS0		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [12]	pdi DATA [13]	VDD_HV_PDI	flexpwm 0 X[0]	H
J	nexus MCKO	nexus MDO[8]	dspi2 CS0	dspi2 CS2		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [14]	pdi DATA [15]	VSS_HV_PDI	flexpwm 0 X[1]	J
K	nexus MSEO_B[0]	nexus MSEO_B[1]	nexus RDY_B	dspi0 SIN		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		flexpwm 0 X[2]	flexpwm 0 X[3]	flexpwm 0 A[1]	flexpwm 0 B[0]	K
L	nexus EVTO_B	nexus EVTI_B	dspi2 SCK	nexus MDO [13]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		VDD_HV_DRAM_VREF	TCK	flexpwm 0 B[1]	TDO	L
M	VDD_HV_OSC	VDD_HV_IO	dspi1 CS2	nexus MDO [12]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		flexpwm 0 B[2]	TDI	TMS	flexpwm 1 A[1]	M
N	XTALIN	VSS_HV_IO	dspi0 CS3	VSS_LV_PLL										flexpwm 0 B[3]	flexpwm 0 A[2]	flexpwm 1 A[0]	flexpwm 1 B[0]	N
P	VSS_HV_OSC	RESET	dspi0 CS2	VDD_LV_PLL	etimer1 ETC[1]	etimer1 ETC[2]	adc0 AN[0]	etimer1 ETC[3]	VSS_HV_IO	VDD_HV_IO	adc0_adc1 AN[14]	etimer1 ETC[4]	etimer1 ETC[5]	VDD_HV_IO	flexpwm 0 A[3]	flexpwm 0 A[0]	flexpwm 1 B[1]	P
R	XTAL OUT	FCCU_F[0]	VSS_HV_IO	dspi1 CS3	adc2 AN[0]	adc2 AN[3]	VDD_HV_ADR_13	adc2_adc3 AN[14]	VDD_HV_ADR_02	adc0 AN[2]	adc0_adc1 AN[13]	adc1 AN[1]	VREG_CTRL	lin0 TXD	VSS_HV_IO	flexpwm 1 A[2]	flexpwm 1 B[2]	R
T	VSS_HV_IO	VDD_HV_IO	dspi2 SOUT	adc3 AN[0]	adc3 AN[3]	adc2 AN[2]	VSS_HV_ADR_13	adc2_adc3 AN[13]	VSS_HV_ADR_02	adc0 AN[1]	adc0_adc1 AN[12]	adc1 AN[0]	adc1 AN[2]	lin0 RXD	etimer1 ETC[0]	VDD_HV_IO	VSS_HV_IO	T
U	VSS_HV_IO	VSS_HV_IO	dspi2 SIN	adc3 AN[1]	adc3 AN[2]	adc2 AN[1]	adc2_adc3 AN[11]	adc2_adc3 AN[12]	VDD_HV_ADV	VSS_HV_ADV	adc0_adc1 AN[11]	VREG_INT_ENABLE	RESET_SUP	VDD_HV_PMU	VSS_HV_PMU	VSS_HV_IO	VSS_HV_IO	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2. MPC5675K 257 MAPBGA pinout (top view)

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
AA21	VSS_HV_IO	VSS_HV	M15	VSS_LV_COR	VSS_LV
AB1	VSS_HV_IO	VSS_HV	M16	VSS_LV_COR	VSS_LV
AB23	VSS_HV_IO	VSS_HV	M17	VSS_LV_COR	VSS_LV
AC1	VSS_HV_IO	VSS_HV	N7	VSS_LV_COR	VSS_LV
AC2	VSS_HV_IO	VSS_HV	N8	VSS_LV_COR	VSS_LV
AC22	VSS_HV_IO	VSS_HV	N9	VSS_LV_COR	VSS_LV
AC23	VSS_HV_IO	VSS_HV	N10	VSS_LV_COR	VSS_LV
AC13	VSS_HV_ADR_0	VSS_HV_A	N11	VSS_LV_COR	VSS_LV
AC16	VSS_HV_ADR_1	VSS_HV_A	N12	VSS_LV_COR	VSS_LV
AC8	VSS_HV_ADR_23	VSS_HV_A	N13	VSS_LV_COR	VSS_LV
AA10	VSS_HV_ADV	VSS_HV_A	N14	VSS_LV_COR	VSS_LV
H23	VSS_HV_DRAM	VSS_HV	N15	VSS_LV_COR	VSS_LV
L22	VSS_HV_DRAM	VSS_HV	N16	VSS_LV_COR	VSS_LV
P22	VSS_HV_DRAM	VSS_HV	N17	VSS_LV_COR	VSS_LV
V22	VSS_HV_DRAM	VSS_HV	P7	VSS_LV_COR	VSS_LV
D12	VSS_HV_FLA	VSS_HV	P8	VSS_LV_COR	VSS_LV
Y1	VSS_HV_OSC	VSS_HV	P9	VSS_LV_COR	VSS_LV
C21	VSS_HV_PDI	VSS_HV	P10	VSS_LV_COR	VSS_LV
D17	VSS_HV_PDI	VSS_HV	P11	VSS_LV_COR	VSS_LV
G7	VSS_LV_COR	VSS_LV	P12	VSS_LV_COR	VSS_LV
G8	VSS_LV_COR	VSS_LV	P13	VSS_LV_COR	VSS_LV
G9	VSS_LV_COR	VSS_LV	P14	VSS_LV_COR	VSS_LV
G10	VSS_LV_COR	VSS_LV	P15	VSS_LV_COR	VSS_LV
G11	VSS_LV_COR	VSS_LV	P16	VSS_LV_COR	VSS_LV
G12	VSS_LV_COR	VSS_LV	P17	VSS_LV_COR	VSS_LV
G13	VSS_LV_COR	VSS_LV	R7	VSS_LV_COR	VSS_LV
G14	VSS_LV_COR	VSS_LV	R8	VSS_LV_COR	VSS_LV
G15	VSS_LV_COR	VSS_LV	R9	VSS_LV_COR	VSS_LV
G16	VSS_LV_COR	VSS_LV	R10	VSS_LV_COR	VSS_LV
G17	VSS_LV_COR	VSS_LV	R11	VSS_LV_COR	VSS_LV
H7	VSS_LV_COR	VSS_LV	R12	VSS_LV_COR	VSS_LV
H8	VSS_LV_COR	VSS_LV	R13	VSS_LV_COR	VSS_LV
H9	VSS_LV_COR	VSS_LV	R14	VSS_LV_COR	VSS_LV
H10	VSS_LV_COR	VSS_LV	R15	VSS_LV_COR	VSS_LV

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
M15	GPIO	TDI	A0: siul_GPIO[21] A1: _ A2: _ A3: _	I: jtagc_TDI I: _ I: _	—	pullup	GP Slow/ Medium	VDD_HV_IO
M17	GPIO	flexpwm1 A[1]	A0: siul_GPIO[157] A1: dramc_ODT A2: ebi_CS1 A3: flexpwm1_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N14	GPIO	flexpwm0 B[3]	A0: siul_GPIO[154] A1: dramc_BA[0] A2: ebi_WE_BE_3 A3: flexpwm0_B[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N15	GPIO	flexpwm0 A[2]	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N16	GPIO	flexpwm1 A[0]	A0: siul_GPIO[155] A1: dramc_BA[1] A2: ebi_BDIP A3: flexpwm1_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N17	GPIO	flexpwm1 B[0]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P3	GPIO	dspi0 CS2	A0: siul_GPIO[54] A1: dspi0_CS2 A2: i2c2_data A3: _	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P5	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
B13	GPIO	fec TX_ER	A0: siul_GPIO[205] A1: fec_TX_ER A2: dspi2_CS3 A3: _	I: flexpwm1_FAULT[3] I: lin0_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B16	GPIO	pdi DATA[4]	A0: siul_GPIO[135] A1: flexpwm2_A[2] A2: _ A3: etimer1_ETC[4]	I: pdi_DATA[4] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B17	GPIO	pdi DATA[0]	A0: siul_GPIO[131] A1: _ A2: lin3_TXD A3: _	I: pdi_DATA[0] I: _ I: flexpwm2_FAULT[2]	—	disabled	PDI Medium	VDD_HV_PDI
B18	GPIO	pdi LINE_V	A0: siul_GPIO[129] A1: _ A2: lin2_TXD A3: _	I: pdi_LINE_V I: _ I: flexpwm2_FAULT[0]	—	disabled	PDI Medium	VDD_HV_PDI
B19	GPIO	pdi DATA[9]	A0: siul_GPIO[140] A1: flexpwm2_X[2] A2: _ A3: _	I: pdi_DATA[9] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B20	GPIO	pdi DATA[14]	A0: siul_GPIO[145] A1: pdi_SENS_SEL[1] A2: i2c2_clock A3: _	I: pdi_DATA[14] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
B21	GPIO	can0 TXD	A0: siul_GPIO[16] A1: can0_TXD A2: _ A3: sscm_DEBUG[0]	I: _ I: _ I: siul_EIRQ[15]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C2	GPIO	nexus MDO[15][1]	A0: siul_GPIO[220] A1: _ A2: npc_wrapper_MDO[15] A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
C14	GPIO	fec RXD[1]	A0: siul_GPIO[212] A1: dspi1_CS1 A2: etimer2_ETC[5] A3: _	I: fec_RXD[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C15	GPIO	fec COL	A0: siul_GPIO[206] A1: fec_COL A2: _ A3: lin1_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C16	GPIO	pdi DATA[5]	A0: siul_GPIO[136] A1: flexpwm2_A[0] A2: _ A3: etimer1_ETC[0]	I: pdi_DATA[5] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C17	GPIO	pdi DATA[2]	A0: siul_GPIO[133] A1: flexpwm2_A[1] A2: _ A3: etimer1_ETC[2]	I: pdi_DATA[2] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C18	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C19	GPIO	pdi DATA[12]	A0: siul_GPIO[143] A1: _ A2: _ A3: _	I: pdi_DATA[12] I: lin3_RXD I: flexpwm2_FAULT[3]	—	disabled	PDI Medium	VDD_HV_PDI
C20	GPIO	can0 RXD	A0: siul_GPIO[17] A1: _ A2: _ A3: sscm_DEBUG[1]	I: can0_RXD I: can1_RXD I: siul_EIRQ[16]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C22	GPIO	siul GPIO[197]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_AD31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
C23	GPIO	dramc CAS	A0: siul_GPIO[152] A1: dramc_CAS A2: ebi_WE_BE_1 A3: flexpwm0_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
N3	GPIO	flexpwm0 X[1]	A0: siul_GPIO[60] A1: flexpwm0_X[1] A2: _ A3: _	I: lin2_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N4	GPIO	flexpwm0 B[2]	A0: siul_GPIO[100] A1: flexpwm0_B[2] A2: _ A3: _	I: _ I: etimer0_ETC[5] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N20	GPIO	dramc DQS[1]	A0: siul_GPIO[191] A1: dramc_DQS[1] A2: ebi_AD25 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N21	GPIO	dramc DM[1]	A0: siul_GPIO[193] A1: dramc_DM[1] A2: ebi_AD27 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N22	GPIO	dramc D[13]	A0: siul_GPIO[187] A1: dramc_D[13] A2: ebi_AD21 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N23	GPIO	dramc D[12]	A0: siul_GPIO[186] A1: dramc_D[12] A2: ebi_AD20 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
P1	GPIO	flexpwm0 B[0]	A0: siul_GPIO[59] A1: flexpwm0_B[0] A2: _ A3: _	I: _ I: etimer0_ETC[1] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P2	GPIO	flexpwm0 B[1]	A0: siul_GPIO[62] A1: flexpwm0_B[1] A2: _ A3: _	I: _ I: etimer0_ETC[3] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P3	GPIO	flexpwm0 A[2]	A0: siul_GPIO[99] A1: flexpwm0_A[2] A2: _ A3: _	I: _ I: etimer0_ETC[4] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
Y22	GPIO	dramc ADD[11]	A0: siul_GPIO[169] A1: dramc_ADD[11] A2: ebi_AD3 A3: ebi_ADD19	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
Y23	GPIO	dramc ADD[5]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AA4	GPIO	dspi1 CS3	A0: siul_GPIO[55] A1: dspi1_CS3 A2: lin2_TXD A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA5	GPIO	flexpwm1 X[1]	A0: siul_GPIO[119] A1: flexpwm1_X[1] A2: etimer2_ETC[1] A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA6	ANA	adc3 AN[1]	—	siul_GPI[230]	AN: adc3_AN[1]	—	Analog	VDD_HV_ADR23
AA7	ANA	adc2_adc3 AN[12]	—	siul_GPI[226]	AN: adc2_adc3_AN[12]	—	Analog Shared	VDD_HV_ADR23
AA8	ANA	adc2 AN[0]	—	siul_GPI[221]	AN: adc2_AN[0]	—	Analog	VDD_HV_ADR23
AA11	ANA	adc0 AN[2]	—	siul_GPI[33]	AN: adc0_AN[2]	—	Analog	VDD_HV_ADR0
AA12	ANA	adc0 AN[5]	—	siul_GPI[66]	AN: adc0_AN[5]	—	Analog	VDD_HV_ADR0
AA13	ANA	adc0 AN[8]	—	siul_GPI[69]	AN: adc0_AN[8]	—	Analog	VDD_HV_ADR0

Table 12. Recommended operating conditions (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	0	0	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	3.0	3.63	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	0	0	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	3.0	3.63	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	0	0	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	3.0	3.63	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	0	0	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	1.62	3.63	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	0	0	V
11	$V_{DD\_HV\_DRAM}$	SR	DRAM interface supply voltage	—	1.62	3.63	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	0	0	V
13	$V_{DD\_HV\_ADRx}$	SR	ADC*x* high reference voltage[1]	—	3.0	3.63	V
				Alternate input voltage	4.5	5.5	
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	0	0	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	3.0	3.63	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	0	0	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic[2]	External VREG mode	1.14	1.32	V
17a		CC		Internal VREG Mode	1.14	1.32	V
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	0	0	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage[2]	External VREG mode	1.14	1.32	V
19a		CC		Internal VREG Mode	1.14	1.32	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	0	0	V
21	T_A	SR	Ambient temperature under bias[3,4]	257 MAPBGA	–40	125	°C
				473 MAPBGA	–40	125	°C
22	T_J	SR	Junction temperature under bias[4]	257 MAPBGA	–40	150	°C
				473 MAPBGA	–40	150	

1 If this supply is not above its absolute minimum recommended operating level, LBIST operations can fail.

2 The jitter specifications for both PLLs holds true only up to 50 mV noise (peak to peak) on $V_{DD\_LV\_COR}$ and $V_{DD\_LV\_PLL}$.

3 See Table 1 for available frequency and package options.

4 When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition.

Table 34. GP pads AC electrical characteristics[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	7	—	40	50
		1	—	6	3	—	12	—	—	40	7	—	40	100
		1	—	6	5	—	18	—	—	25	7	—	40	200
4	Symmetric	1	—	8	1	—	5	—	—	50	3	—	25	25
5	Pullup/down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

3.17.3 I/O pad current specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated based on the voltage, frequency, and load on the pin.

Table 35. I/O pad current specifications

Pad Type	Load (pF)	Frequency (MHz)	VDD_HV_IO (V)	Current (mA)
GP Slow/Medium	20	4	3.6	0.30
GP Slow/Symmetric	20	10	3.6	0.76
GP Slow/Fast	20	45	3.6	3.40
GP Slow	20	0.5	3.6	0.04

3.17.4 Power Sequence Pin States for GPIO Pads

Table 36. Power sequence pin states for GPIO pads

VDD_LV_COR	VDD_HV_IO	Pad Function
Low	Low	Outputs Disabled
Low	High	Outputs Disabled
High	Low	Outputs Disabled

Table 42. Power sequence pin states for PDI pads

VDD_LV_COR	VDD_HV_IO	VDD_HV_PDI	Pad Function
Low	High	x	Outputs Disabled
High	Low	Low	Outputs Disabled
High	Low	High	Outputs drive high
High	High	Low	Normal Operation[1]
High	High	High	Normal Operation

1 Normal operation except no drive current and input buffer output is unknown. The pad pre-drive circuitry will function normally but since VDD_HV_PDI is unpowered the outputs will not drive high even though the output PMOS can be enabled.

3.19 DRAM pad specifications

This section specifies the electrical characteristics of the DRAM pads. Please refer to the tables in Section 2.2, Pin descriptions, for a cross reference between package pins and pad types.

DRAM pads feature list:

- Driver
  - Configurable to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR modes.
  - VDD_HV_DRAM range of
    - 1.8 V nominal
    - 2.5 V nominal
    - 3.3 V nominal
- Receiver
  - Differential or pseudo-differential input buffer in all DRAM pads
  - All inputs are tolerant up to their VDD_HV_DRAM absolute maximum rating
  - Data and strobe pads can be configured to support four signal termination options
    - Infinite/no termination
    - 50 Ω
    - 75 Ω
    - 150 Ω

The electrical data provided in Section 3.19, DRAM pad specifications, applies to the pads listed in Table 43.

Table 43. DRAM pads

Name	Voltage	Used For	Notes[1]
DRAM ACC	1.62 V–3.6 V	I/O	Bidirectional DDR pad
DRAM CLK	1.62 V–3.6 V	O	Output only differential clock driver pad
DRAM DQ	1.62 V–3.6 V	I/O	Bidirectional DDR pad with integrated ODT

1 All pads can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.

All three pad types can be configured to support SDR, DDR, DDR2 half and full strength, and LPDDR half and full strength modes, according to Table 44.

JEDEC standards define the minimum set of requirements for compliant memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, MAY 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The MPC5675K supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strength (intended for lighter loads or point-to-point environments)

The MPC5675K memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the Section 3.19, DRAM pad specifications.

3.22.1.1 DDR and DDR2 SDRAM AC timing specifications

Table 61. DDR and DDR2 (DDR2-400) SDRAM timing specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

No.	Symbol		Parameter	Min	Max	Unit
1	t_{CK}	CC	Clock cycle time, CL = *x*	—	90	MHz
2	$V_{IX\text{-}AC}$	CC	MCK AC differential crosspoint voltage[1]	$V_{DD\_MEM\_IO}$ × 0.5 – 0.1	$V_{DD\_MEM\_IO}$ × 0.5 + 0.1	V
3	t_{CH}	CC	CK HIGH pulse width[1, 2]	0.47	0.53	t_{CK}
4	t_{CL}	CC	CK LOW pulse width[1, 2]	0.47	0.53	t_{CK}
5	t_{DQSS}	CC	Skew between MCK and DQS transitions[2, 3]	–0.25	0.25	t_{CK}
6	$t_{OS(base)}$	CC	Address and control output setup time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)		ps
7	$t_{OH(base)}$	CC	Address and control output hold time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)	—	ps
8	$t_{DS1(base)}$	CC	DQ and DM output setup time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
9	$t_{DH1(base)}$	CC	DQ and DM output hold time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
10	t_{DQSQ}	CC	DQS-DQ skew for DQS and associated DQ inputs[2]	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps

1 Measured with clock pin loaded with differential 100 Ω termination resistor.

2 All transitions measured at mid-supply ($V_{DD\_MEM\_IO}$/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

Figure 22 shows the DDR SDRAM write timing.

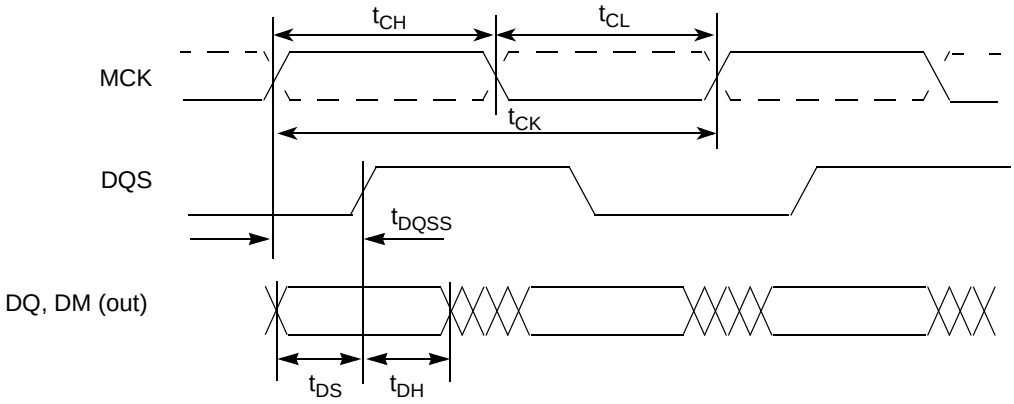

Figure 22. DDR write timing

Figure 23 and Figure 24 show the DDR SDRAM read timing.

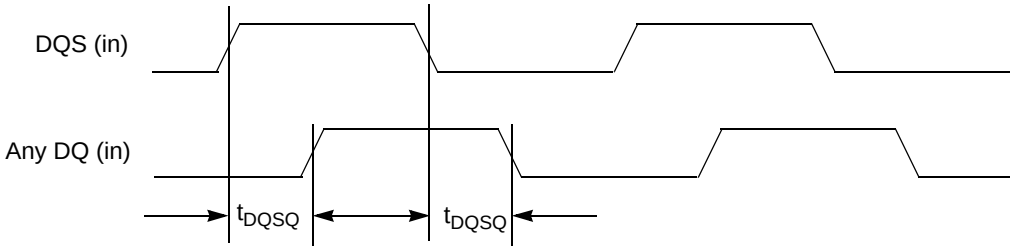

Figure 23. DDR read timing, DQ vs. DQS

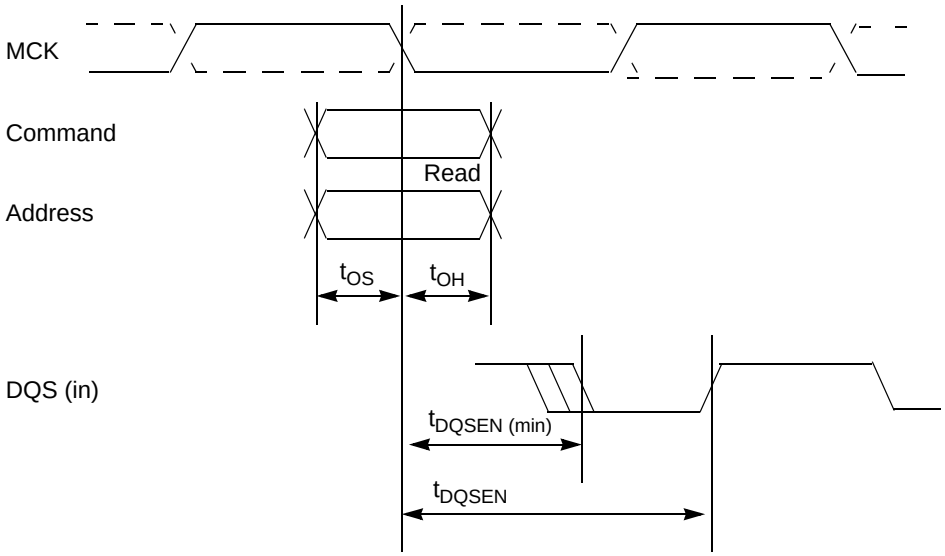

Figure 24. DDR read timing, DQSEN

Figure 25 provides the AC test load for the DDR bus.

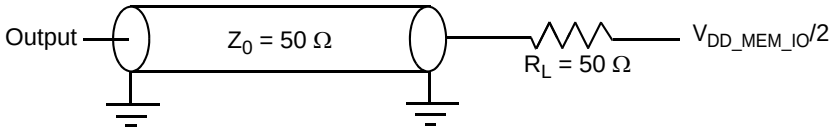

Figure 25. DDR AC test load

3.22.2 IEEE 1149.1 (JTAG) interface timing

3.22.2.1 Standard interface timing

Table 62. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	60	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDE}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	12	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	6	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	18	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	6	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	18	ns
9	t_{BSDV}	D	TCK falling edge to output valid (BSR)	—	—	14	ns
10	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance (BSR)	—	—	15	ns
11	t_{BSDHZ}	D	TCK falling edge to output high impedance (BSR)	—	—	10	ns
12	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	15	—	ns
13	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	2	—	ns

[1] $f_{TCK} = 1/t_{TCK}$. f_{TCK} must not exceed 1/4 the frequency of the system clock (SYS_CLK).

3.22.2.2 Interface timing for Full Cycle mode

Table 63. JTAG pin Full Cycle mode AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	40	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDE}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	12	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	6	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	18	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	6	—	ns

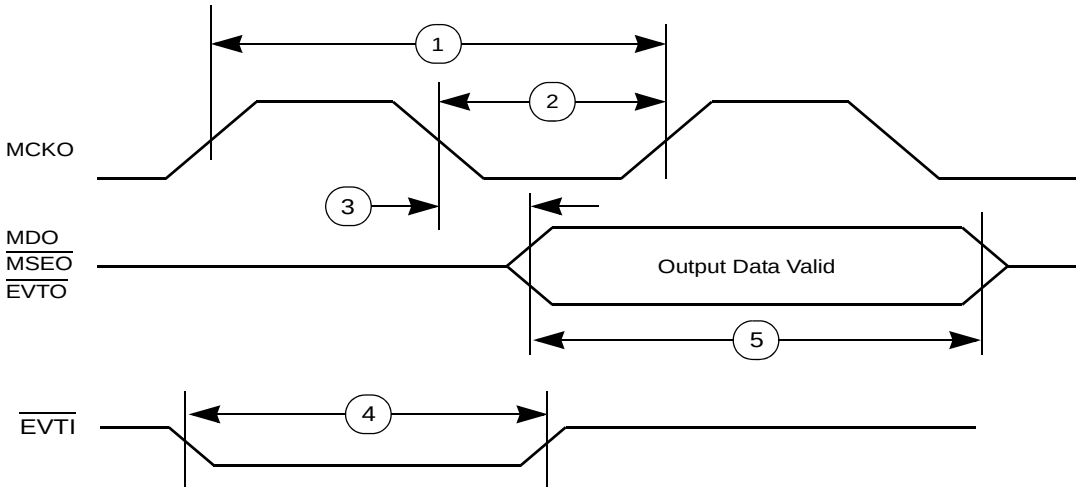

Figure 29. Nexus SDR (Even divisor) timing

Table 65. Nexus debug port timing Divide by 3 SDR mode[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCKO}	CC	MCKO cycle time	—	16.67	—	ns
2	t_{MDC}	CC	MCKO duty cycle[2]	—	33	66	%
3	t_{MDOV}	CC	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ data valid	—	–1.67	3.34	ns
4	t_{EVTIPW}	CC	$\overline{\text{EVTI}}$ pulse width. Captured on JTAG TCK.	—	4.0	—	t_{JCYC}
5	t_{PW}	CC	MDO, $\overline{\text{MSEO}}$,$\overline{\text{EVTO}}$ pulse width in SDR mode	—	1	—	t_{MCKO}

1 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle in SDR mode. Rise/Fall time for Nexus signals can be derived from Fast GPIO pad specification section.

2 Jitter/tolerance for MCKO clock is derived from PLL. Please see PLL section for jitter specification.

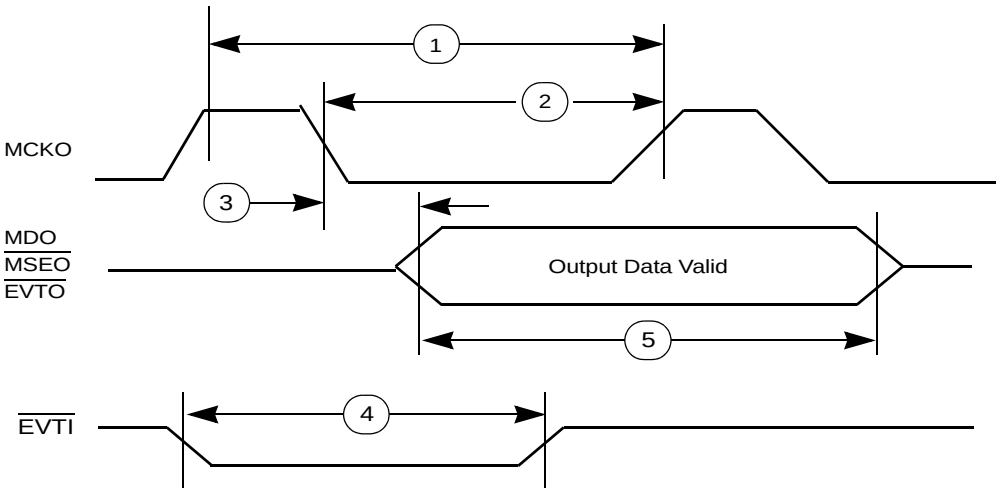

Figure 30. Nexus SDR output timing for DIV=3

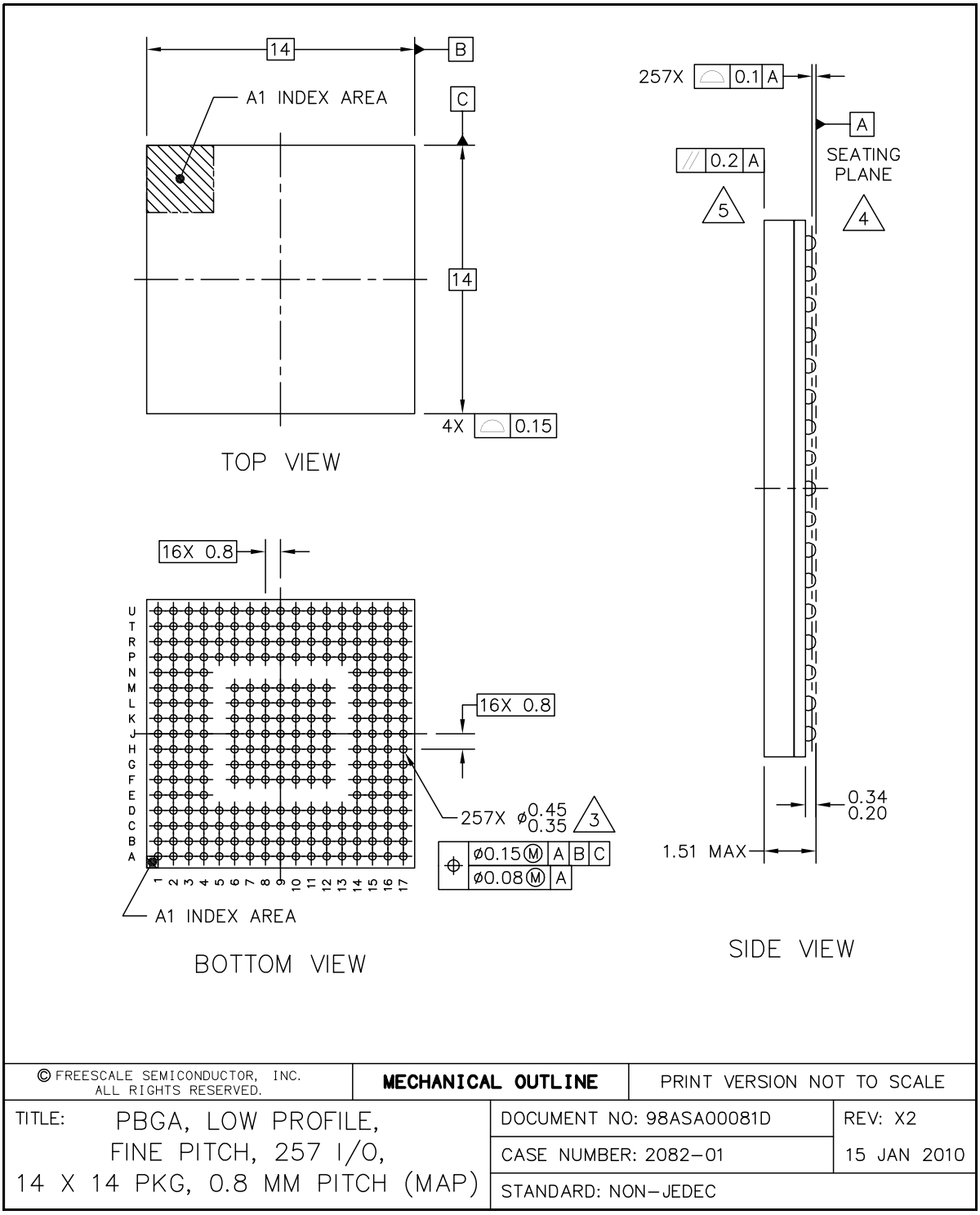

Figure 54. 257 MAPBGA mechanical data (1 of 2)

Table 79. Revision history (continued)

Revision	Date	Description of Changes
6 (cont.)	6 Feb 2012	In Table 68 (External interrupt timing (GPIO IRQ)): • Changed T_{IPWL} min value from TBD to 3. • Changed T_{IPWH} min value from TBD to 3. • Changed T_{ICYC} min value from TBD to 6. • Changed all units from ns to t_{CYC}. In Table 77 (I^2C SCL and SDA input timing specifications), corrected the line numbering.
6.1	30 Mar 2012	No content changes, technical or editorial, were made in this revision. Change bars are identical to those in Rev. 6. Removed the “preliminary” footers throughout. Changed “Data Sheet: Advance Information” to “Data Sheet: Technical Data” on page Removed the “product under development” disclaimer on page 1.
7	18 May 2012	Minor editorial changes and improvements throughout. In Section 1.3, Device comparison, Table 1 (MPC5675K family device comparison), • Changed the CPU/Data Cache entry from "16 KB, 4-way with EDC (SoR)" to "16 KB, 4-way with Parity (SoR)". • Added footnotes to stipulate the peripheral instances that are used on derivative devices: - Added footnote to **MPC5673K** DSPI module: “DSPI_0 and DSPI_1.“ - Added footnote to **MPC5673K** I2C module: “I2C_0 and I2C_1.“ - Added footnote to **MPC5673K** LinFlex module: “LinFlex_0, LinFlex_1, and LinFlex_2“ In Section 1.4, Block diagram: • Added missing modules (PMC, SPE2, VLE, and flash. • Added an arrow each from Core_0 and Core_1 to the XBAR modules to represent the data path. • Updated the Redundancy Checkers to reflect the actual implementation. • Renamed the “JTAG/Nexus” block to “Debug”, with JTAG and Nexus shown as submodules. In Section 1.5, Feature list, changed “Junction temperature sensor” to “Silicon substrate (die) temperature sensor”. In Section 1.6.1, High-performance e200z7d core processor and Section 1.6.9, Cache memory, removed the bullet “Supports tag and data parity" and added the following bullets: — Supports tag and data cache parity — Supports EDC for instruction cache In Section 1.6.19, System Timer Module (STM), changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)” In Section 1.6.20.2, Cross Triggering Unit (CTU), changed “DMA support with safety features” to “Supports safety measures using DMA”. In Section 1.6.21, Redundancy Control and Checker Unit (RCCU), changed “Duplicated module to guarantee highest possible diagnostic coverage (check of checker)” to “Duplicated module to enable high diagnostic coverage (check of checker)”. In Section 1.6.22, Software Watchdog Timer (SWT), • Changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)”. • Changed “Allows high level of safety (SIL3 monitor)” to “Provides measures to target high safety integrity levels (for example, SIL 3, ASIL D)”. In Section 1.6.25, Cyclic Redundancy Checker (CRC) unit, in the sentence “Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol”, changed “allow” to “support”.

Table 79. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.18, PDI pads specifications, Table 38 (PDI pads DC electrical characteristics), added footnote to table: “Over- and undershoots occurring due to impedance mismatch of the external driver and the transmission line at PDI pads in input mode can be allowed up to 0.7 V repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.” In Section 5, Orderable parts, • Removed “3 = 220 MHz” under Operating frequency heading and changed the Operating frequency of the example from “3” to “2”. • Deleted Table 73 (Orderable part number summary**)**.