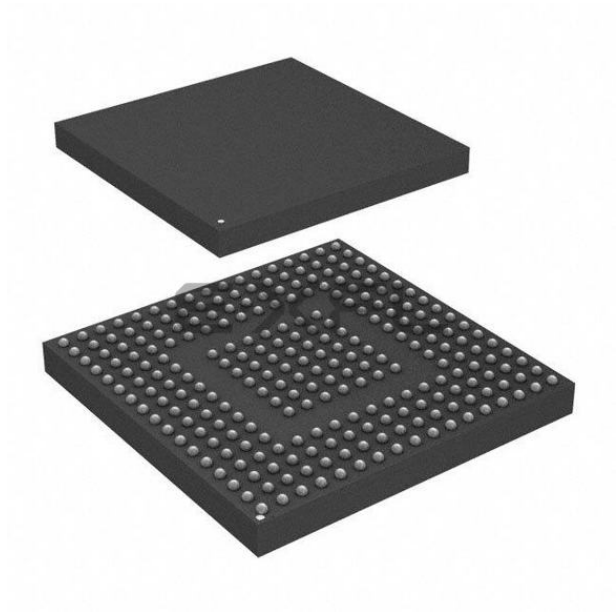

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kff0vmm2

1.5 Feature list

- High-performance e200z7d dual core
  - 32-bit Power Architecture® technology CPU
  - Up to 180 MHz core frequency
  - Dual-issue core
  - Variable length encoding (VLE)
  - Memory management unit (MMU) with 64 entries
  - 16 KB instruction cache and 16 KB data cache
- Memory available
  - Up to 2 MB code flash memory with ECC
  - 64 KB data flash memory with ECC
  - Up to 512 KB on-chip SRAM with ECC
- SIL3/ASILD innovative safety concept: LockStep mode and fail-safe protection
  - Sphere of replication (SoR) for key components
  - Redundancy checking units on outputs of the SoR connected to FCCU
  - Fault collection and control unit (FCCU)
  - Boot-time built-in self-test for memory (MBIST) and logic (LBIST) triggered by hardware
  - Boot-time built-in self-test for ADC and flash memory
  - Replicated safety-enhanced watchdog timer
  - Silicon substrate (die) temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) units
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority interrupt controller
- GPIOs individually programmable as input, output, or special function
- 3 general-purpose eTimer units (6 channels each)
- 3 FlexPWM units with four 16-bit channels per module
- Communications interfaces
  - 4 LINFlex modules
  - 3 DSPI modules with automatic chip select generation
  - 4 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1) with dual channel, up to 128 message objects and up to 10 Mbit/s
  - Fast Ethernet Controller (FEC)
  - 3 I^2C modules
- Four 12-bit analog-to-digital converters (ADCs)
  - 22 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADC conversion with timer and PWM
- External bus interface
- 16-bit external DDR memory controller
- Parallel digital interface (PDI)

- Program flow control monitor with 16-bit pseudorandom key generation
- Provides measures to target high safety integrity levels (for example, SIL 3, ASIL D)

1.6.23 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, NMI, reset, or safe mode)
  - External reaction (failure is reported to the outside world via configurable output pins)

1.6.24 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pullup/pulldown
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.6.25 Cyclic Redundancy Checker (CRC) unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to an input register.

The CRC unit has the following features:

- Three sets of registers to allow three concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores the result in an internal register
- Implements the following standard CRC polynomials:
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to support implementation of safe communication protocol
- Offloads the core from cycle-consuming CRC and helps in checking the configuration signature for safe start-up or periodic procedures
- Connected as a peripheral on the internal peripheral bus
- Provides DMA support

Table 2. Pad types (continued)

Pad Type	Description
DRAM ACC	Bidirectional DDR pad. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM CLK	Differential clock driver.
DRAM DQ	Bidirectional DDR pad with integrated ODT. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM ODT CTL	Enable On Die Termination control.
Analog	CMOS Schmitt trigger cell with injection proof analog switch.
Analog Shared	CMOS Schmitt trigger cell with two injection-proof analog switches.

2.2.2 Power supply and reference voltage pins

Table 3 shows the supply pins for the MPC5675K in the 257 MAPBGA package. Table 5 shows the supply pins for the MPC5675K in the 473 MAPBGA package.

Table 4 and Table 6 show the pins not populated on the MPC5675K 257 MAPBGA and 473 MAPBGA packages, respectively.

Table 3. 257 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F9	VDD_LV_COR	VDD_LV
A9	VDD_HV_IO	VDD_HV	F10	VDD_LV_COR	VDD_LV
B16	VDD_HV_IO	VDD_HV	F11	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F12	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	G12	VDD_LV_COR	VDD_LV
P10	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
P14	VDD_HV_IO	VDD_HV	H12	VDD_LV_COR	VDD_LV
T2	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T16	VDD_HV_IO	VDD_HV	J12	VDD_LV_COR	VDD_LV
L14	VDD_HV_DRAM_VREF	VDD_HV	K6	VDD_LV_COR	VDD_LV
D8	VDD_HV_FLA	VDD_HV	K12	VDD_LV_COR	VDD_LV
M1	VDD_HV_OSC	VDD_HV	L6	VDD_LV_COR	VDD_LV
D14	VDD_HV_PDI	VDD_HV	L12	VDD_LV_COR	VDD_LV
H16	VDD_HV_PDI	VDD_HV	M6	VDD_LV_COR	VDD_LV
U14	VDD_HV_PMU	VDD_HV	M7	VDD_LV_COR	VDD_LV
R7	VDD_HV_ADR_13	VDD_HV_A	M8	VDD_LV_COR	VDD_LV

Table 6. 473 MAPBGA pins not populated on package

E5	E6	E7	E8	E9	E10	E11	E12
E13	E14	E15	E16	E17	E18	E19	F5
F19	G5	G19	H5	H19	J5	J19	K5
K19	L5	L19	M5	M19	N5	N19	P5
P19	R5	R19	T5	T19	U5	U19	V5
V19	W5	W6	W7	W8	W9	W10	W11
W12	W13	W14	W15	W16	W17	W18	W19

2.2.3 System pins

Table 7 shows the system pins for the MPC5675K in the 257 MAPBGA package. Table 8 shows the system pins for the MPC5675K in the 473 MAPBGA package.

Table 7. 257 MAPBGA system pins

Ball number	Ball name	Weak pull during reset	Safe mode default condition	Pad type	Power domain
C4	FCCU_F[1]	disabled	not available	GP Slow/Medium	VDD_HV_IO
C10	JCOMP	pulldown	not available	GP Slow	VDD_HV_IO
E1	Nexus MDO[0][1]	—	not available	GP Slow/Fast	VDD_HV_IO
E4	NMI	pullup	not available	GP Slow	VDD_HV_IO
L15	TCK[2]	pullup	not available	GP Slow	VDD_HV_IO
M16	TMS	pullup	not available	GP Slow	VDD_HV_IO
N1	XTALIN	—	not available	Analog Feedthrough	VDD_HV_IO
P2	$\overline{\text{RESET}}$	pulldown	not available	Reset	VDD_HV_IO
R1	XTALOUT	—	not available	Analog Feedthrough	VDD_HV_IO
R2	FCCU_F[0]	disabled	not available	GP Slow/Medium	VDD_HV_IO
R13	VREG_CTRL	—	—	Analog Feedthrough	VDD_REG
U12	VREG_INT_ENABLE	—	—	Analog Feedthrough	VDD_HV_IO
U13	$\overline{\text{RESET\_SUP}}$	pulldown	—	Analog Feedthrough	VDD_HV_IO

1 Do not connect pin directly to a power supply or ground.

2 If LBIST is enabled, an external pull between 1K and 100K ohm must be connected from TCK to either power or ground to avoid LBIST failures.

Table 8. 473 MAPBGA system pins

Ball number	Ball name	Weak pull during reset	Safe mode default condition	Pad type	Power domain
C4	FCCU_F[1]	disabled	not available	GP Slow/Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
C7	GPIO	etimer0 ETC[1]	A0: siul_GPIO[1] A1: etimer0_ETC[1] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[1]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C8	GPIO	etimer0 ETC[2]	A0: siul_GPIO[2] A1: etimer0_ETC[2] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[2]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C9	GPIO	etimer0 ETC[3]	A0: siul_GPIO[3] A1: etimer0_ETC[3] A2: _ A3: _	I: _ I: mc_rgm_ABS[2] I: siul_EIRQ[3]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
C11	GPIO	fec CRS	A0: siul_GPIO[208] A1: flexray_DBG1 A2: etimer2_ETC[3] A3: dspi0_CS5	I: fec_CRS I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C12	GPIO	fec TXD[0]	A0: siul_GPIO[201] A1: fec_TXD[0] A2: etimer2_ETC[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C13	GPIO	fec COL	A0: siul_GPIO[206] A1: fec_COL A2: _ A3: lin1_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C14	GPIO	can0 RXD	A0: siul_GPIO[17] A1: _ A2: _ A3: sscm_DEBUG[1]	I: can0_RXD I: can1_RXD I: siul_EIRQ[16]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C16	GPIO	pdi DATA[5]	A0: siul_GPIO[136] A1: flexpwm2_A[0] A2: _ A3: etimer1_ETC[0]	I: pdi_DATA[5] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
C17	GPIO	pdi CLOCK	A0: siul_GPIO[128] A1: flexpwm2_B[1] A2: _ A3: etimer1_ETC[3]	I: pdi_CLOCK I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
J17	GPIO	flexpwm0 X[1]	A0: siul_GPIO[195] A1: flexpwm0_X[1] A2: ebi_AD29 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K1	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K2	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K3	GPIO	nexus RDY_B	A0: siul_GPIO[216] A1: _ A2: nexus_RDY_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K4	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
K14	GPIO	flexpwm0 X[2]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_AD30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K15	GPIO	flexpwm0 X[3]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_AD31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K16	GPIO	flexpwm0 A[1]	A0: siul_GPIO[149] A1: _ A2: ebi_RD_WR A3: flexpwm0_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K17	GPIO	flexpwm0 B[0]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
T3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO
T4	ANA	adc3 AN[0]	—	siul_GPI[229]	AN: adc3_AN[0]	—	Analog	VDD_HV_ADR13
T5	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	Analog	VDD_HV_ADR13
T6	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR02
T8	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR02
T10	ANA	adc0 AN[1]	—	siul_GPI[24] etimer0_ETC[5]	AN: adc0_AN[1]	—	Analog	VDD_HV_ADR02
T11	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR02
T12	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR13
T13	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR13
T14	GPIO	lin0 RXD	A0: siul_GPIO[19] A1: _ A2: i2c0_data A3: sscm_DEBUG[3]	I: lin0_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
J23	GPIO	dramc D[6]	A0: siul_GPIO[180] A1: dramc_D[6] A2: ebi_AD14 A3: ebi_ADD30	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K1	GPIO	dspi0 SCK	A0: siul_GPIO[37] A1: dspi0_SCK A2: _ A3: sscm_DEBUG[5]	I: flexpwm0_FAULT[3] I: _ I: siul_EIRQ[23]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K2	GPIO	dspi1 CS0	A0: siul_GPIO[5] A1: dspi1_CS0 A2: _ A3: dspi0_CS7	I: _ I: _ I: siul_EIRQ[5]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K3	GPIO	dspi1 SCK	A0: siul_GPIO[6] A1: dspi1_SCK A2: _ A3: _	I: _ I: _ I: siul_EIRQ[6]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K4	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K21	GPIO	dramc D[4]	A0: siul_GPIO[178] A1: dramc_D[4] A2: ebi_AD12 A3: ebi_ADD28	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K22	GPIO	dramc D[8]	A0: siul_GPIO[182] A1: dramc_D[8] A2: ebi_AD16 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K23	GPIO	dramc D[9]	A0: siul_GPIO[183] A1: dramc_D[9] A2: ebi_AD17 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
L1	GPIO	dspi0 CS0	A0: siul_GPIO[36] A1: dspi0_CS0 A2: _ A3: sscm_DEBUG[4]	I: _ I: _ I: siul_EIRQ[22]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
L2	GPIO	dspi2 CS2	A0: siul_GPIO[42] A1: dspi2_CS2 A2: lin3_TXD A3: can2_TXD	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
L3	GPIO	dspi2 CS0	A0: siul_GPIO[10] A1: dspi2_CS0 A2: _ A3: can3_TXD	I: _ I: _ I: siul_EIRQ[9]	—	disabled	GP Slow/ Medium	VDD_HV_IO
M1	GPIO	flexpwm0 X[0]	A0: siul_GPIO[57] A1: flexpwm0_X[0] A2: lin2_TXD A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M3	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M20	GPIO	dramc ODT	A0: siul_GPIO[157] A1: dramc_ODT A2: ebi_CS1 A3: flexpwm1_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
M21	GPIO	dramc WEB	A0: siul_GPIO[153] A1: dramc_WEB A2: ebi_WE_BE_2 A3: flexpwm0_A[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
M22	GPIO	dramc D[11]	A0: siul_GPIO[185] A1: dramc_D[11] A2: ebi_AD19 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
M23	GPIO	dramc D[10]	A0: siul_GPIO[184] A1: dramc_D[10] A2: ebi_AD18 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
N1	GPIO	flexpwm0 A[0]	A0: siul_GPIO[58] A1: flexpwm0_A[0] A2: _ A3: _	I: _ I: etimer0_ETC[0] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
Y22	GPIO	dramc ADD[11]	A0: siul_GPIO[169] A1: dramc_ADD[11] A2: ebi_AD3 A3: ebi_ADD19	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
Y23	GPIO	dramc ADD[5]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AA4	GPIO	dspi1 CS3	A0: siul_GPIO[55] A1: dspi1_CS3 A2: lin2_TXD A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA5	GPIO	flexpwm1 X[1]	A0: siul_GPIO[119] A1: flexpwm1_X[1] A2: etimer2_ETC[1] A3: dspi0_CS4	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA6	ANA	adc3 AN[1]	—	siul_GPI[230]	AN: adc3_AN[1]	—	Analog	VDD_HV_ADR23
AA7	ANA	adc2_adc3 AN[12]	—	siul_GPI[226]	AN: adc2_adc3_AN[12]	—	Analog Shared	VDD_HV_ADR23
AA8	ANA	adc2 AN[0]	—	siul_GPI[221]	AN: adc2_AN[0]	—	Analog	VDD_HV_ADR23
AA11	ANA	adc0 AN[2]	—	siul_GPI[33]	AN: adc0_AN[2]	—	Analog	VDD_HV_ADR0
AA12	ANA	adc0 AN[5]	—	siul_GPI[66]	AN: adc0_AN[5]	—	Analog	VDD_HV_ADR0
AA13	ANA	adc0 AN[8]	—	siul_GPI[69]	AN: adc0_AN[8]	—	Analog	VDD_HV_ADR0

In case of only narrow band disturbances the maximum of the results will not change. In case of broadband signals the emission has to be below the limits.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	750 (corners) 500	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Power Management Controller (PMC) electrical characteristics

3.8.1 PMC electrical specifications

This section contains electrical characteristics for the PMC.

Table 34. GP pads AC electrical characteristics[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	7	—	40	50
		1	—	6	3	—	12	—	—	40	7	—	40	100
		1	—	6	5	—	18	—	—	25	7	—	40	200
4	Symmetric	1	—	8	1	—	5	—	—	50	3	—	25	25
5	Pullup/down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

3.17.3 I/O pad current specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated based on the voltage, frequency, and load on the pin.

Table 35. I/O pad current specifications

Pad Type	Load (pF)	Frequency (MHz)	VDD_HV_IO (V)	Current (mA)
GP Slow/Medium	20	4	3.6	0.30
GP Slow/Symmetric	20	10	3.6	0.76
GP Slow/Fast	20	45	3.6	3.40
GP Slow	20	0.5	3.6	0.04

3.17.4 Power Sequence Pin States for GPIO Pads

Table 36. Power sequence pin states for GPIO pads

VDD_LV_COR	VDD_HV_IO	Pad Function
Low	Low	Outputs Disabled
Low	High	Outputs Disabled
High	Low	Outputs Disabled

Table 40. PDI pads AC electrical characteristics (continued)

No.	Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
2	PDI Fast	0.8/0.7 -------- 1.1/1.08	10/10	1.1/1.1	—	50	11
			15/15	2.6/2.6		200	
			15/15	2.4/2.4		50	10
			22/22	5/5		200	
			24/24	5/5		50	01
			33/33	8/8		200	
			66/66	16/16		50	00
			84/84	21/21		200	

1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.18.1 PDI pad current specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated based on the voltage, frequency, and load on the pin.

Table 41. PDI pad current specifications

Pad Type	Frequency (MHz)	Load (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
PDI Medium	66	50	3.6	11	8.7
	33	50	3.6	10	3.8
	20	50	3.6	01	2.3
	3	50	3.6	00	0.38
	3	200	3.6	00	1.5
PDI Fast	66	50	3.6	11	12
	50	50	3.6	10	6.2
	33	50	3.6	01	4.0
	20	50	3.6	00	2.4
	20	200	3.6	00	8.9

3.18.2 Power Sequence Pin States for PDI Pads

Table 42. Power sequence pin states for PDI pads

VDD_LV_COR	VDD_HV_IO	VDD_HV_PDI	Pad Function
Low	Low	High	Outputs drive high

Table 55. Power sequence pin states for DRAM pads

VDD_LV_COR	VDD_HV_IO	VDD_HV_PDI	Pad Function
High	High	Low	Normal Operation[1]
High	High	High	Normal Operation

1 Normal operation except no drive current and input buffer output is unknown. The pad pre-drive circuitry will function normally but since VDD_HV_DRAM is unpowered, the outputs will not drive high even though the output PMOS can be enabled. DDR pad is only guaranteed to operate and be in compliance with Jedec standards, when all three power supplies, VDD_LV_COR, VDD_HV_IO and VDD_HV_DRAM are fully powered up.

3.20 $\overline{\text{RESET}}$ characteristics

3.20.1 $\overline{\text{RESET}}$ pin characteristics

Table 56. $\overline{\text{RESET}}$ pin characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	W_{FRST}	SR	$\overline{\text{RESET}}$ pulse is sure to be filtered	—	—	70	ns
2	W_{NFRST}	SR	$\overline{\text{RESET}}$ pulse is sure not to be filtered	—	400	—	ns

3.20.2 $\overline{\text{RESET\_SUP\_B}}$ pin characteristics

Table 57. $\overline{\text{RESET\_SUP\_B}}$ pin characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	W_{FRST}	SR	$\overline{\text{RESET\_SUP\_B}}$ pulse is sure to be filtered (there is no internal filter on this pin)	—	—	0	ns
2	T_{RSTSUP}	SR	$\overline{\text{RESET\_SUP\_B}}$ release by an external delay/monitor circuit after all supplies are stable	—	0	—	ns

3.21 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences depending on internal or external VREG mode.

3.21.1 Reset sequence duration

Table 58 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Section 3.21.2, Reset sequence description.

Table 68. External interrupt timing (GPIO IRQ) (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
3	t_{ICYC}	SR	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

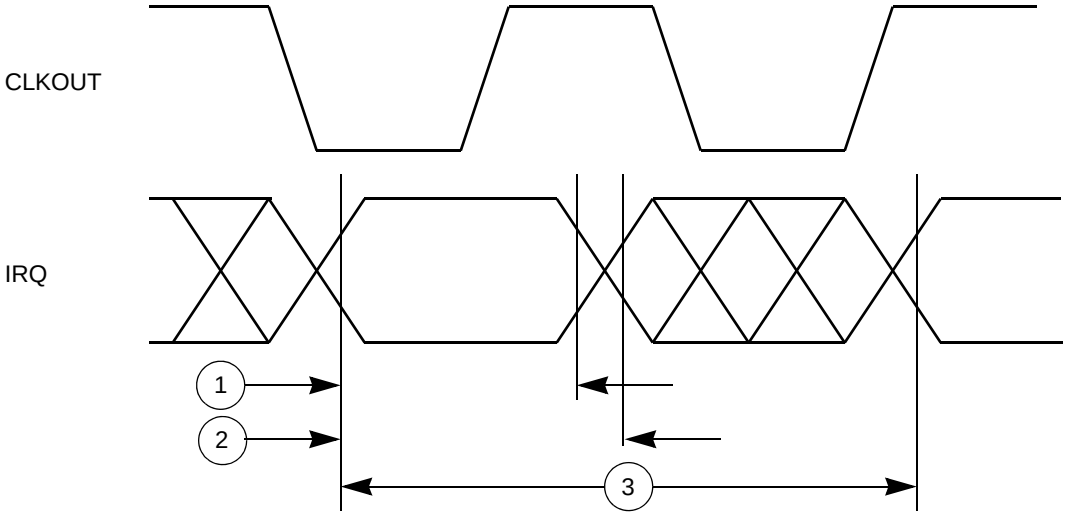

Figure 32. External interrupt timing

3.22.5 FlexCAN timing

Table 69. FlexCAN timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	f_{CAN_TX}	CC	FlexCAN design target transmit data rate	—	10	—	MBit/s
2	f_{CAN_RX}	CC	FlexCAN design target receive data rate	—	10	—	MBit/s

3.22.6 DSPI timing

Table 70. DSPI timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	DSPI cycle time	Master (MTFE = 0)	62	—	ns
				Slave (MTFE = 0)	62	—	
				Slave receive only mode[1]	16	—	
2	t_{CSC}	CC	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	After SCK delay	—	16	—	ns
4	t_{SDC}	CC	SCK duty cycle	—	0.4 × t_{SCK}	0.6 × t_{SCK}	ns

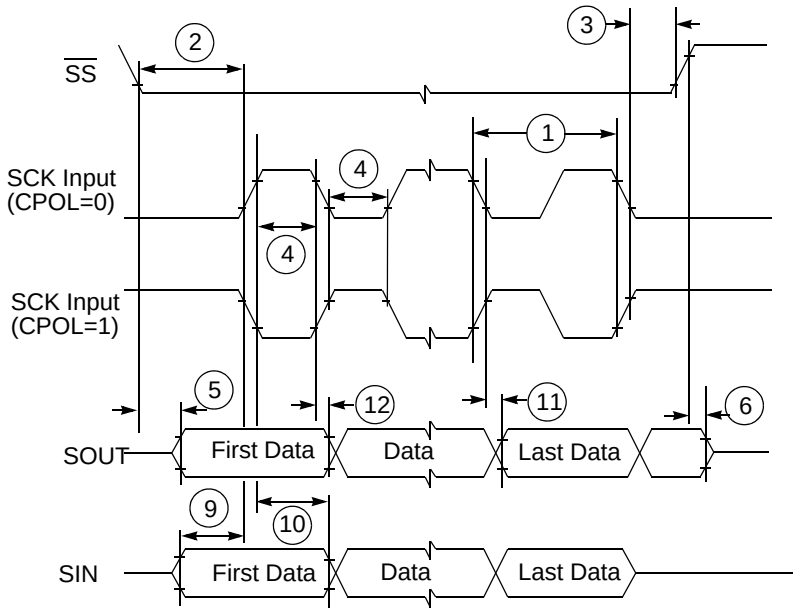

Figure 35. DSPI classic SPI timing—slave, CPHA = 0

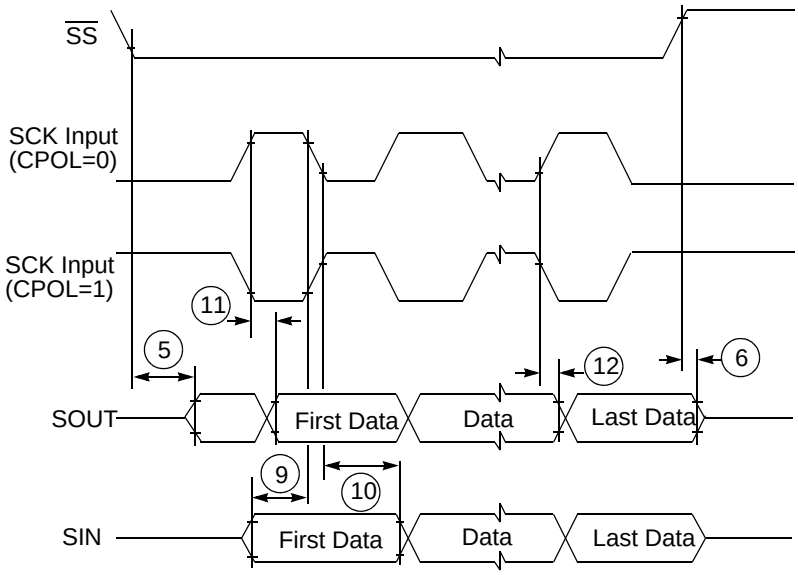

Figure 36. DSPI classic SPI timing—slave, CPHA = 1

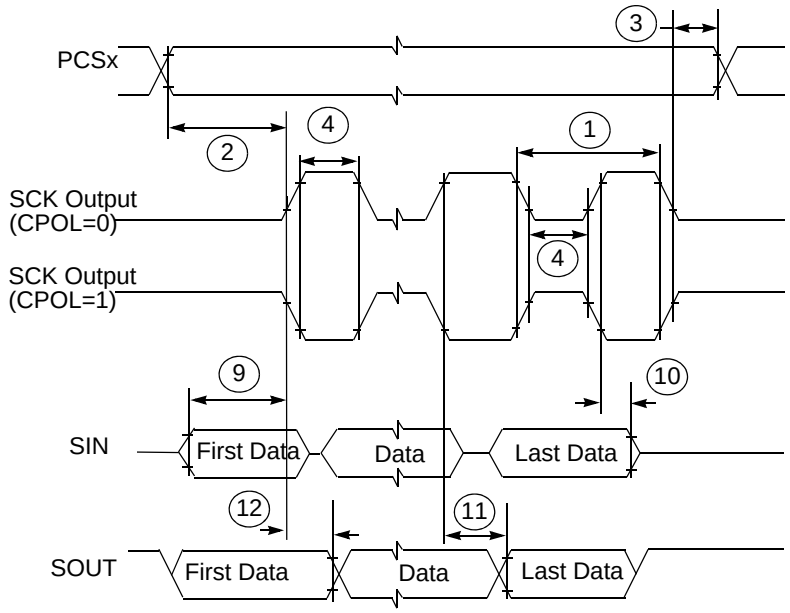

Figure 37. DSPI modified transfer format timing—master, CPHA = 0

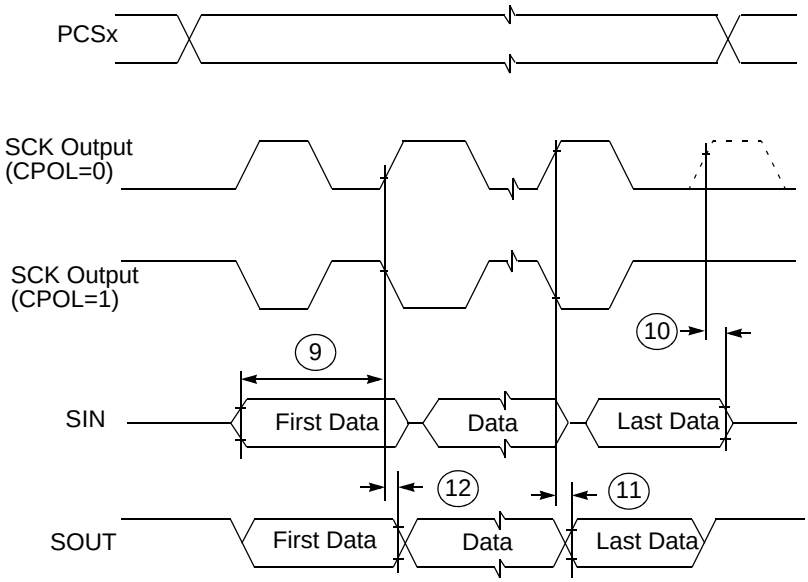

Figure 38. DSPI modified transfer format timing—master, CPHA = 1

4.1.2 473 MAPBGA

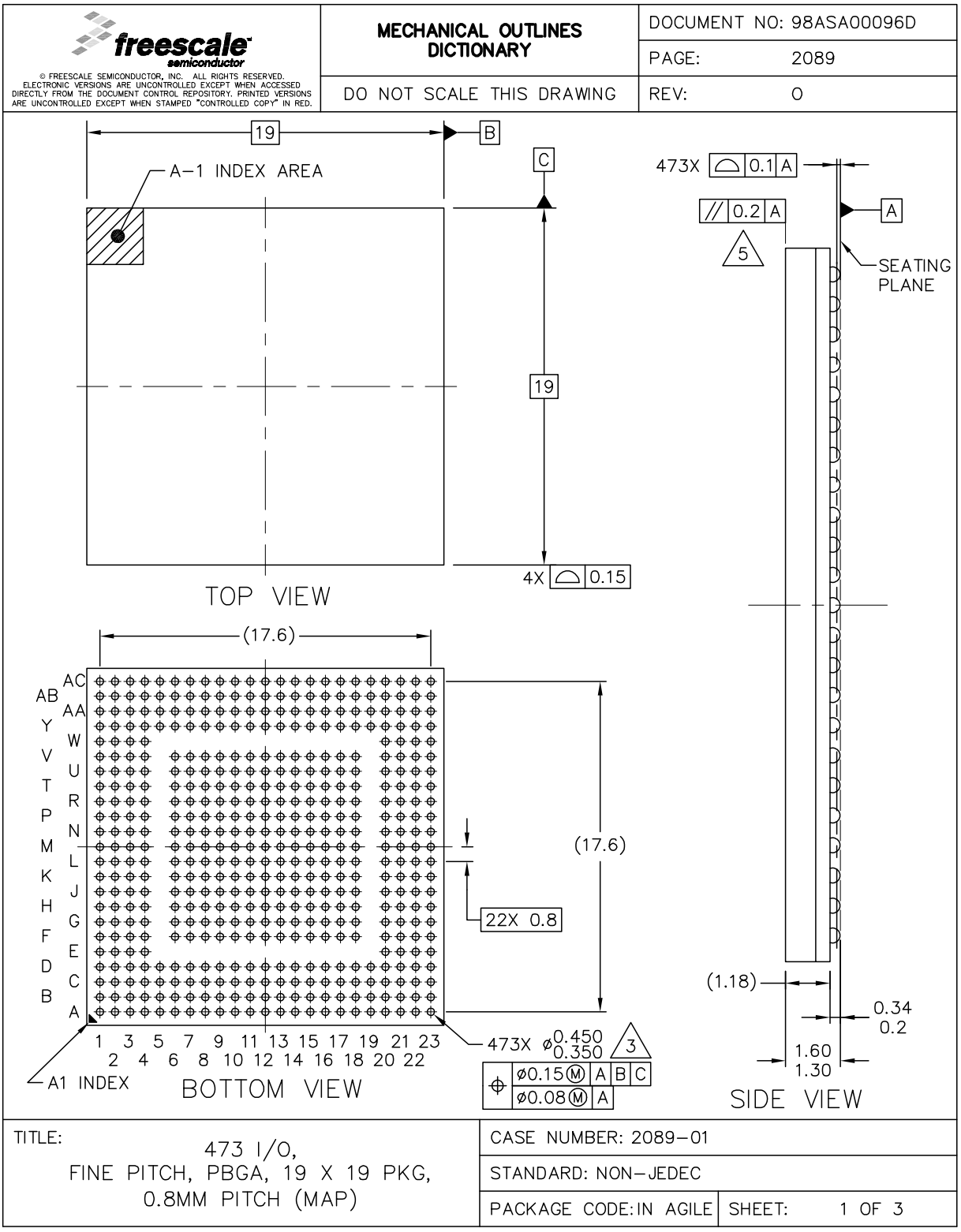

Figure 56. 473 MAPBGA package mechanical data (1 of 3)

Revision	Date	Description of Changes
8 (Contd..)	29 October 2013	In Table 58 (RESET sequences), changed min values of T_{DRB} and T_{ERLB} from 60 to 50 ms and typ values from 65 to 60 ms. In Table 62 (JTAG pin AC electrical characteristics), updated the footnote to - "$f_{TCK} = 1/t_{TCK}$. f_{TCK} must not exceed 1/4 the frequency of the system clock (SYS_CLK)." Reverted the first term of Equation 11.