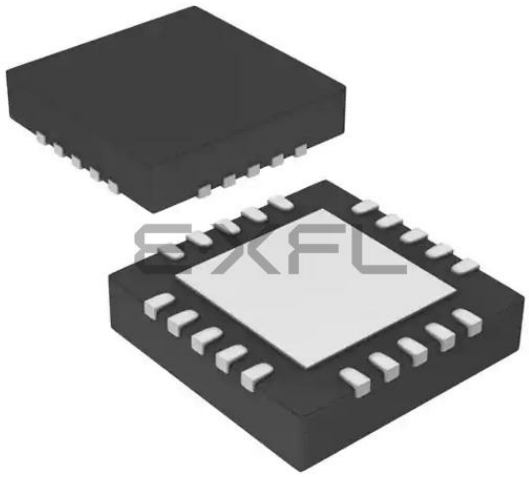


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl020-e-ml

Table of Contents

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0064GPL036 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0064GPL036 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0064GPL036 FAMILY BLOCK DIAGRAM

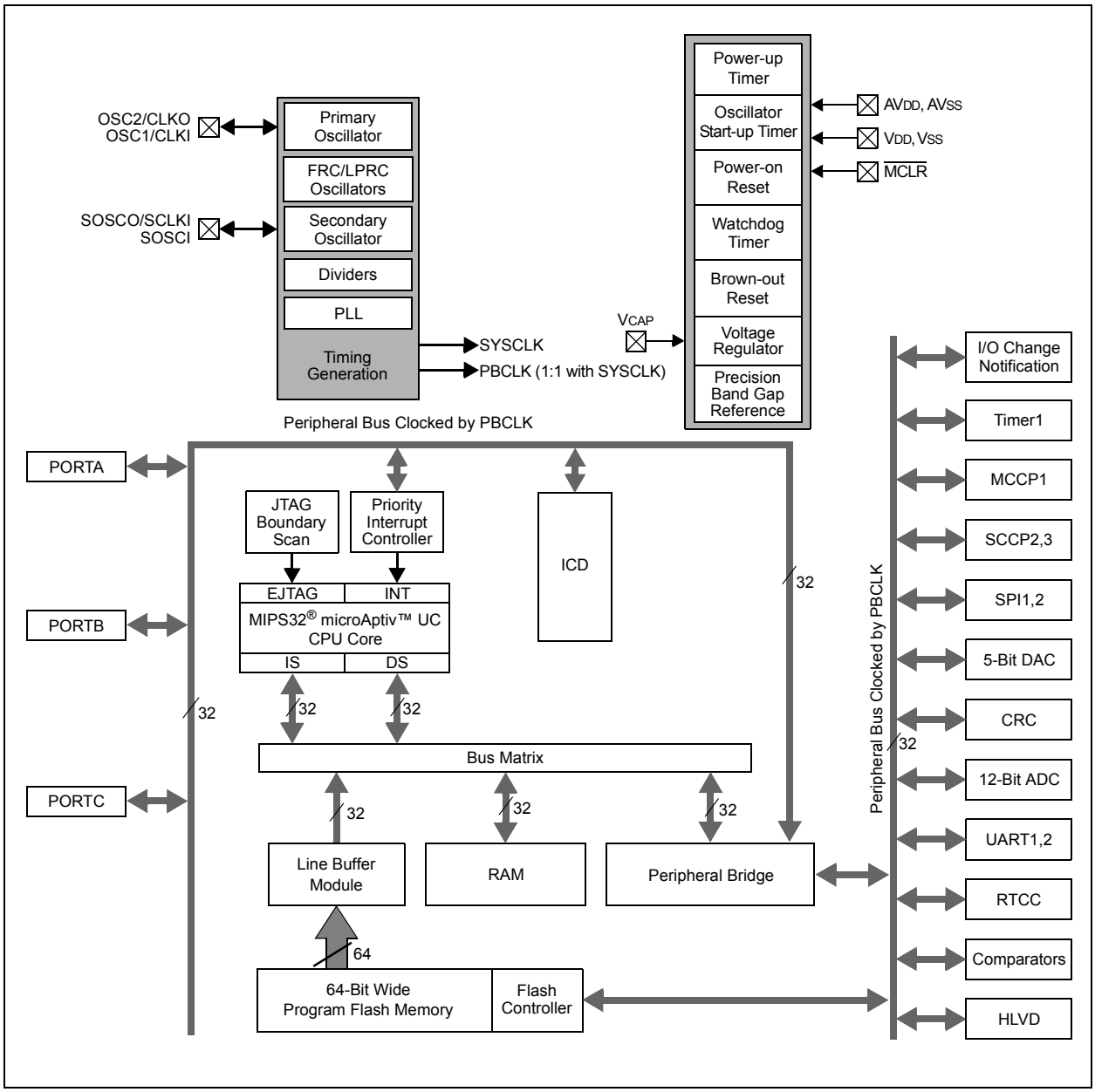
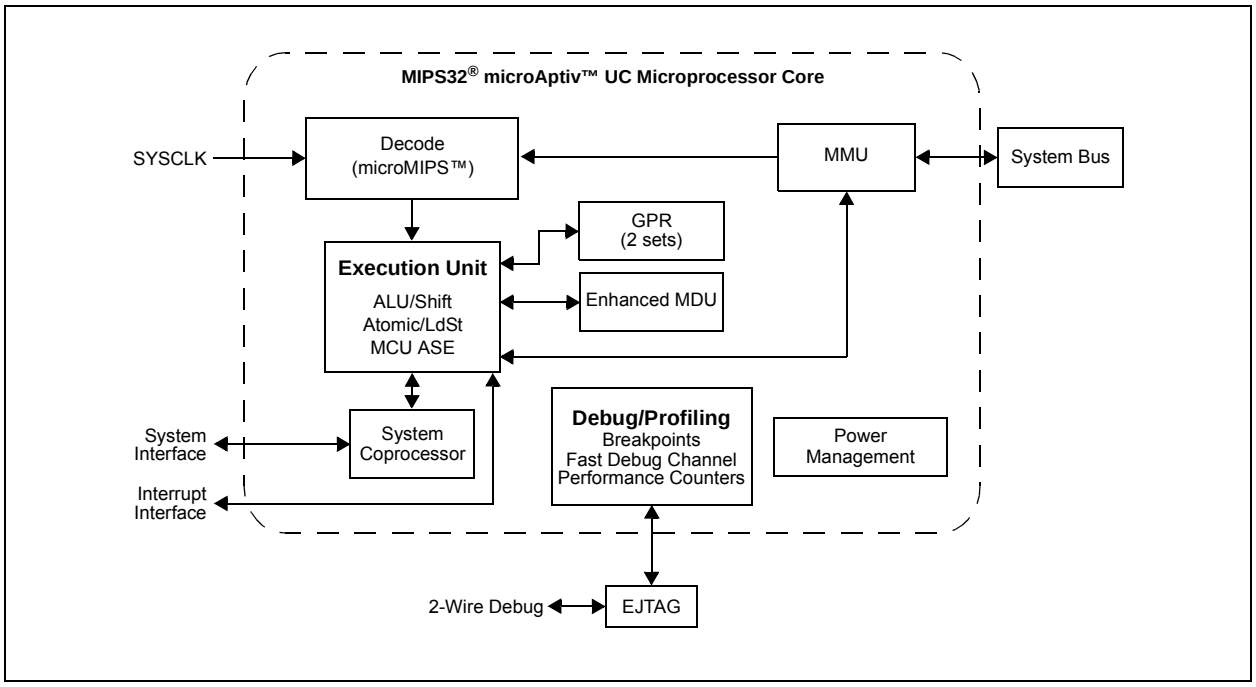


FIGURE 3-1: PIC32MM0064GPL036 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



3.2 Architecture Overview

The MIPS32® microAptiv™ UC microprocessor core in the PIC32MM0064GPL036 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the rs operand. The second number ('16' of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU`, `MADD/MADDU`, `MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL` (GPR destination)	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating-Point Unit bit
0 = Floating-Point Unit is not implemented

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

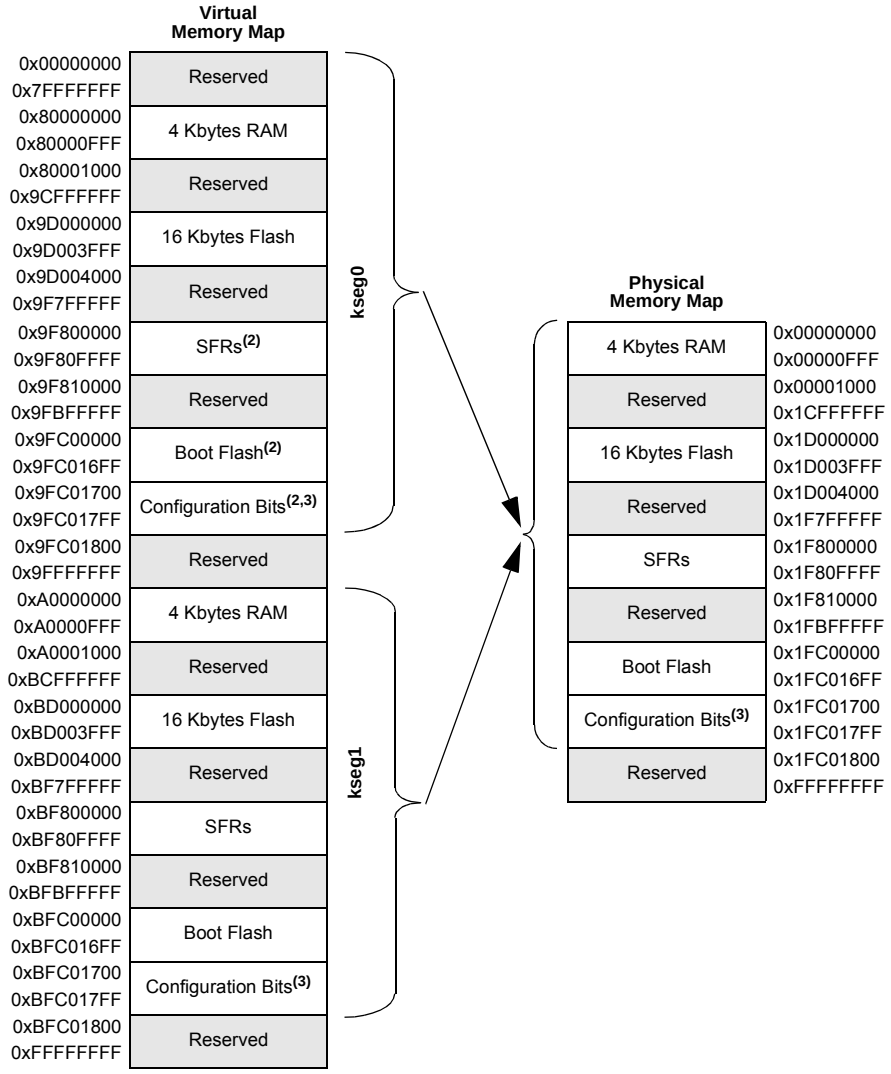
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 16 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. "Oscillators with DCO"** (DS60001329) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0064GPL036 family oscillator system has the following modules and features:

- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- Primary High-Frequency Crystal Oscillator
- Secondary Low-Frequency and Low-Power Crystal Oscillator
- On-Chip Fast RC (FRC) Oscillator with User-Selectable Output Divider
- Software-Controllable Switching between Various Clock Sources
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output (REFO)

A block diagram of the oscillator system is provided in Figure 8-1.

8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0064GPL036 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	OPSSRC(1)	RTRGEN(2)	—	—	OPS<3:0>(3)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TMRPS<1:0>		T32	CCSEL	MOD<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OPSSRC:** Output Postscaler Source Select bit(1)
- 1 = Output postscaler scales the Special Event Trigger output events
- 0 = Output postscaler scales the timer interrupt events

bit 30 **RTRGEN:** Retrigger Enable bit(2)
- 1 = Time base can be retriggered when CCPTRIG = 1
- 0 = Time base may not be retriggered when CCPTRIG = 1

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **OPS<3:0>:** CCPx Interrupt Output Postscale Select bits(3)
- 1111 = Interrupt every 16th time base period match
- 1110 = Interrupt every 15th time base period match
- ...
- 0100 = Interrupt every 5th time base period match
- 0011 = Interrupt every 4th time base period match or 4th input capture event
- 0010 = Interrupt every 3rd time base period match or 3rd input capture event
- 0001 = Interrupt every 2nd time base period match or 2nd input capture event
- 0000 = Interrupt after each time base period match or input capture event

bit 23 **TRIGEN:** CCPx Triggered Enable bit
- 1 = Triggered operation of the timer is enabled
- 0 = Triggered operation of the timer is disabled

bit 22 **ONESHOT:** One-Shot Mode Enable bit
- 1 = One-Shot Triggered mode is enabled; trigger duration is set by OSCNT<2:0>
- 0 = One-Shot Triggered mode is disabled

bit 21 **ALTSYNC:** CCPx Clock Select bit
- 1 = An alternate signal is used as the module synchronization output signal
- 0 = The module synchronization output signal is the Time Base Reset/rollover event

Note 1: This control bit has no function in Input Capture modes.

2: This control bit has no function when TRIGEN = 0.

3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

14.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "UART"** (DS61107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

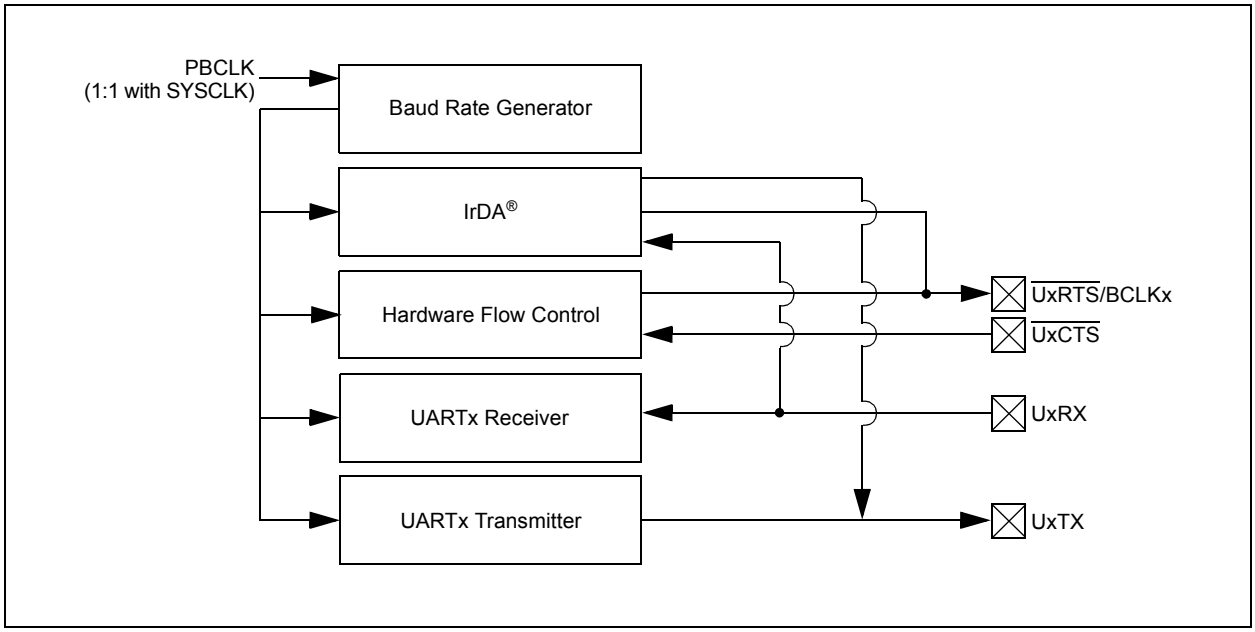
The UART module is one of the serial I/O modules available in the PIC32MM0064GPL036 family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN/J2602 and IrDA®. The module also supports the hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Auto-Baud Feature
- Hardware Flow Control Option
- Fully Integrated Baud Rate Generator (BRG) with 16-Bit Prescaler
- Baud Rates Ranging from 47.7 bps to 6.26 Mbps at 25 MHz
- 8-Level Deep First-In-First-Out (FIFO) Transmit Data Buffer
- 8-Level Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for Interrupt Only on Address Detect (9th bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- LIN/J2602 Protocol Support
- IrDA Encoder and Decoder with 16x Baud Clock Output for External IrDA Encoder/Decoder Support
- Supports Separate UART Baud Clock Input
- Ability to Continue to Run when a Receive Overflow (ROV) Condition Exists
- Ability to Run and Receive Data during Sleep mode

Figure 14-1 illustrates a simplified block diagram of the UART module.

FIGURE 14-1: UARTx SIMPLIFIED BLOCK DIAGRAM



REGISTER 16-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN(1)	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC VR+	ADC VR-
000	AVDD	AVSS
001	AVDD	External VREF- Pin
010	External VREF+ Pin	AVSS
011	External VREF+ Pin	External VREF- Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit(1)

1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Mode bit

1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1 (ADC buffers split into 2 x 8-word buffers).
1 = ADC is currently filling Buffers 8-15, user should access data in 0-7
0 = ADC is currently filling Buffers 0-7, user should access data in 8-15

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF(0...7), ADC1BUF(8...15)
0 = Buffer configured as one 16-word buffer, ADC1BUF(0...15)

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit only takes effect when the auto-scan feature is enabled (ASEN (AD1CON5<15>) = 1.

20.1 CDAC Control Registers

TABLE 20-1: CDAC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0980	DAC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	DACDAT<4:0>					0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

TABLE 26-4: OPERATING CURRENT (I_{DD})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC19	0.45	0.65	mA	2.0V	FSYS = 1 MHz
	0.45	0.65	mA	3.3V	
DC23	2.5	3.5	mA	2.0V	FSYS = 8 MHz
	2.5	3.5	mA	3.3V	
DC24	7.0	9.2	mA	2.0V	FSYS = 25 MHz
	7.0	9.2	mA	3.3V	
DC25	0.26	0.35	mA	2.0V	FSYS = 32 kHz
	0.26	0.35	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IDD current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 010 and POSCMOD<1:0> (FOSCSEL<9:8>) = 00)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- NOP instructions are executed

TABLE 26-5: IDLE CURRENT (I_{IDLE})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC40	0.26	0.46	mA	2.0V	FSYS = 1 MHz
	0.26	0.46	mA	3.3V	
DC41	0.85	1.5	mA	2.0V	FSYS = 8 MHz
	0.85	1.5	mA	3.3V	
DC42	2.3	3.7	mA	2.0V	FSYS = 25 MHz
	2.3	3.7	mA	3.3V	
DC44	0.18	0.34	mA	2.0V	FSYS = 32 kHz
	0.18	0.34	mA	3.3V	

Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = `010` and POSCMOD<1:0> (FOSCSEL<9:8>) = `00`)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = `1`)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = `00`)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = `0` and SOSCSEL (FOSCSEL<12>) = `0`)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = `00` and LPBOREN (FPOR<3>) = `0`)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = `0`)
- All I/O pins (excepting OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

FIGURE 26-5: TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS

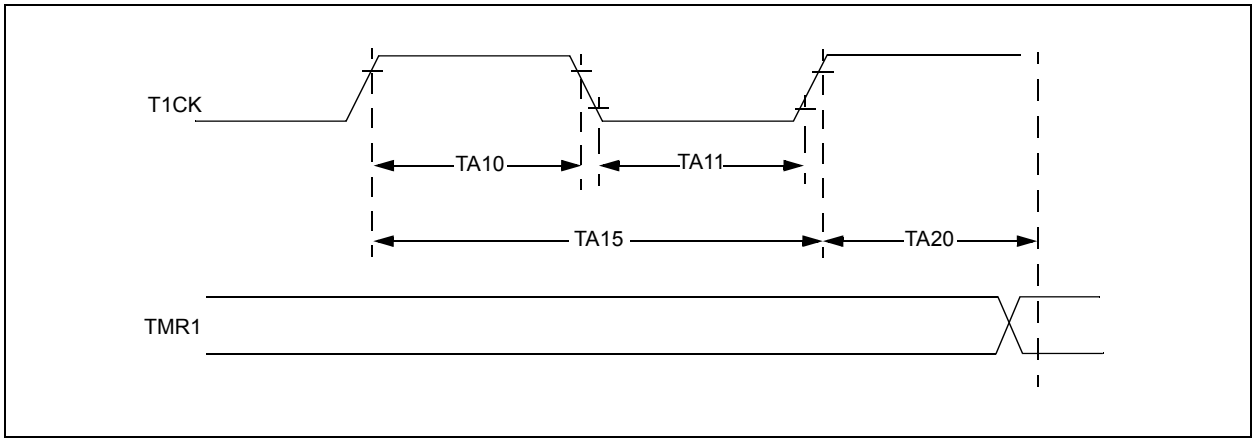


TABLE 26-23: MCCP/SCCP TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristics(1)**		**Min**	**Max**	**Units**	**Conditions**
TA10	TCKH	T1CK High Time	Synchronous	1	—	TPBCLK	Must also meet Parameter TA15
			Asynchronous	10	—	ns	
TA11	TCKL	T1CK Low Time	Synchronous	1	—	TPBCLK	Must also meet Parameter TA15
			Asynchronous	10	—	ns	
TA15	TCKP	T1CK Input Period	Synchronous	2	—	TPBCLK	
			Asynchronous	20	—	ns	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		—	3	TPBCLK	Synchronous mode

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-28: SPIx MODULE MASTER MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param. No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP10	TscL, TscH	SCKx Output Low or High Time	10	—	ns
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	7	ns
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	7	—	ns
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	7	—	ns
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

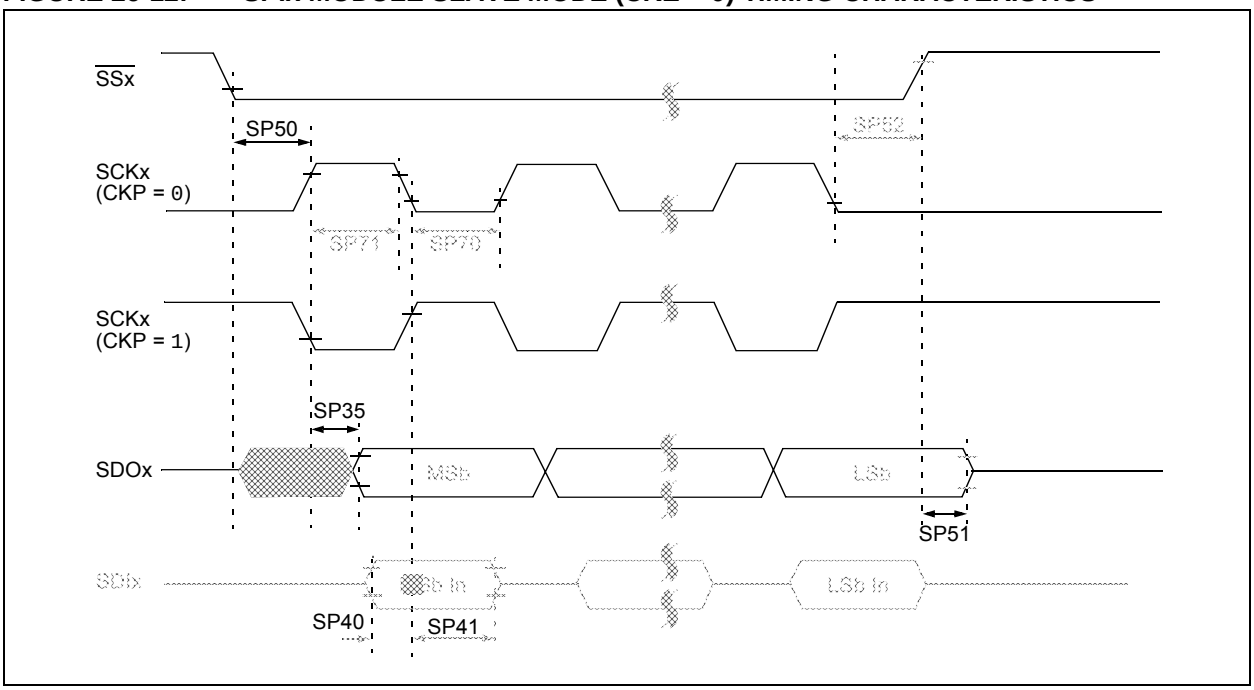


FIGURE 26-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

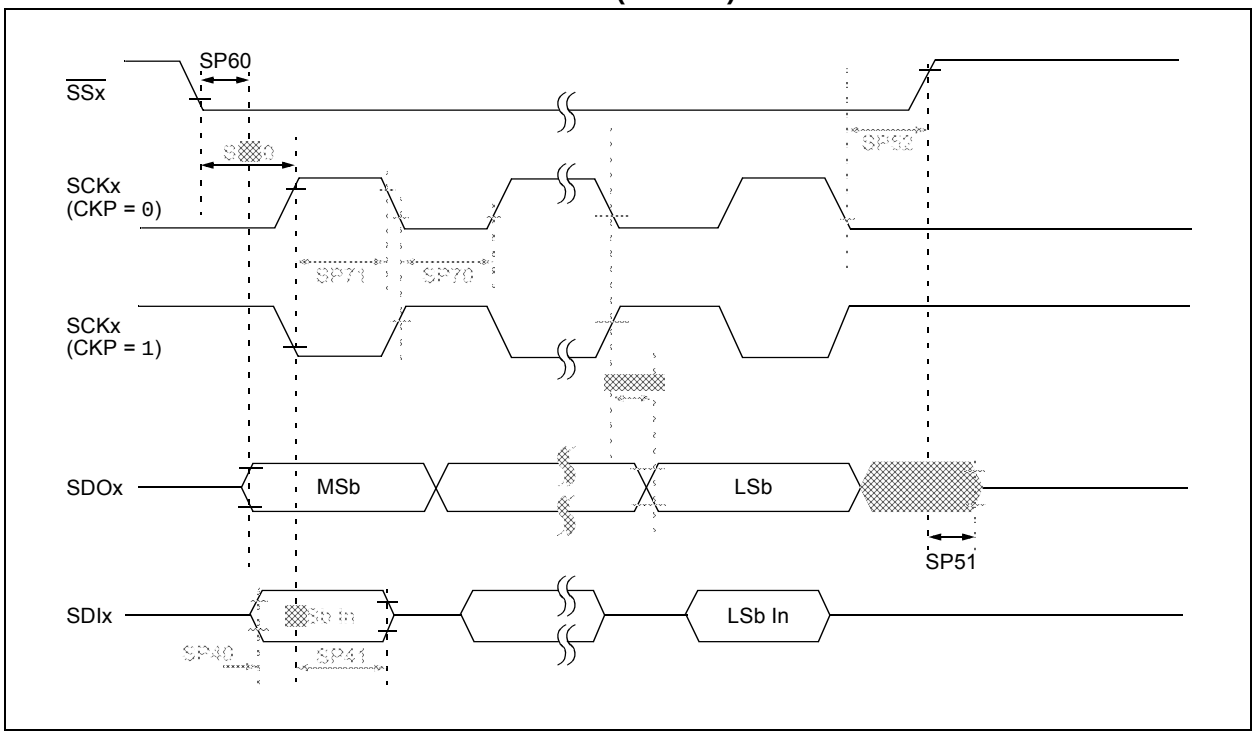


TABLE 26-29: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C (unless otherwise stated)					
Param.No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP70	TscL	SCKx Input Low Time	10	—	ns
SP71	TscH	SCKx Input High Time	10	—	ns
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	ns
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	ns
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	40	—	ns
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	2.5	12	ns
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	ns
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	12.5	ns

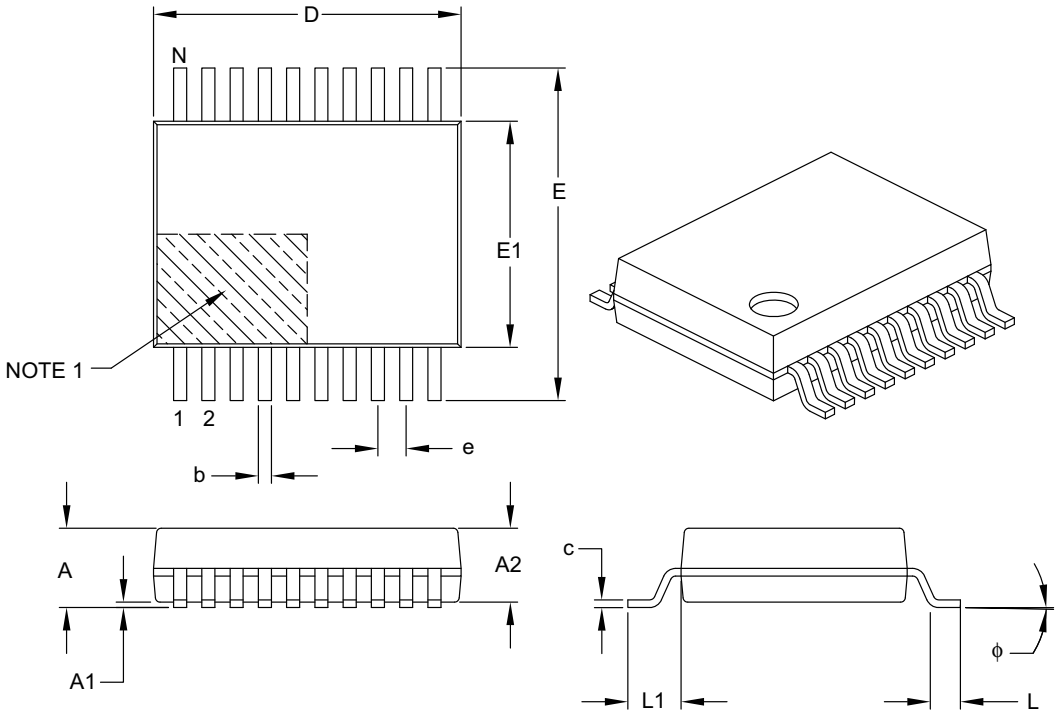
Note 1: These parameters are characterized but not tested in manufacturing.

27.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

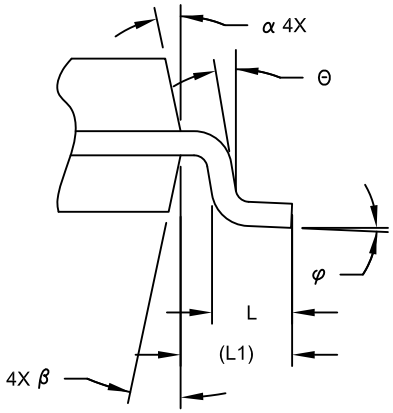
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

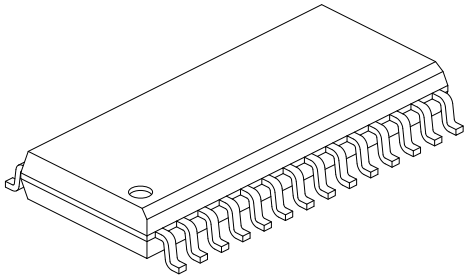
Microchip Technology Drawing C04-072B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

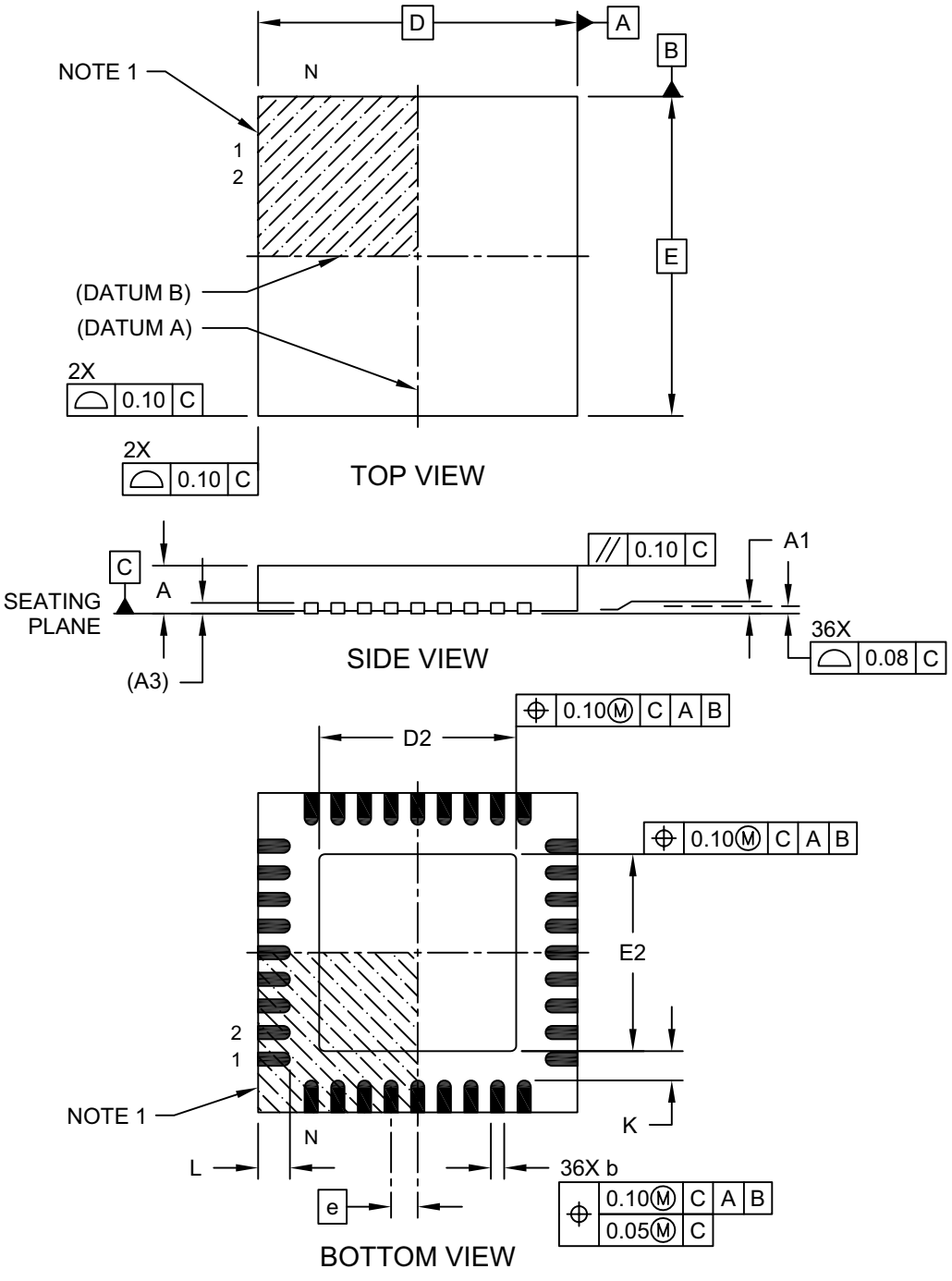
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2