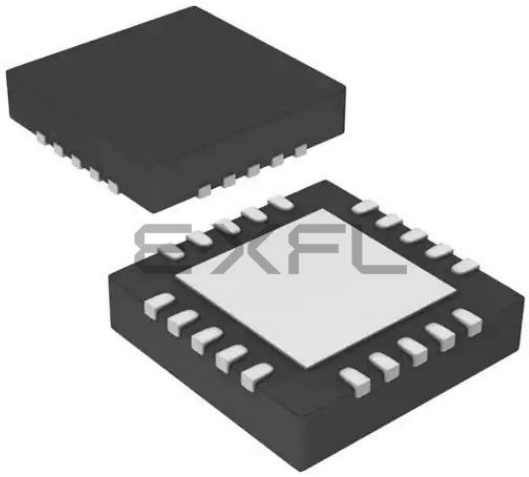

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 11x10/12b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-VFQFN Exposed Pad |
| Supplier Device Package | 20-QFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl020-i-ml |

## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0064GPL036 family devices contain an internal Flash program memory for executing user code. The Program and Boot Flash Memory can be write-protected. The erase page size is 512 32-bit words. The program row size is 64 32-bit words. The memory can be programmed by rows or by two 32-bit words.

The devices implement an Error Correcting Code (ECC). The memory control block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC bits. The ECC provides improved resistance to Flash errors. The ECC single-bit error will be transparently corrected. The ECC double-bit error results in a bus error exception.

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is described in **Section 5. "Flash Programming"** in the *"PIC32 Family Reference Manual"*. EJTAG programming is performed using the JTAG port of the device. ICSP programming requires fewer connections than for EJTAG programming. The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site.

### 5.1 Flash Controller Registers Write Protection

The NVMPWP and NVMBWP registers, and the WR bit in the NVMCON register are protected (locked) from an accidental write. A special unlock sequence is required to modify the content of these registers or bits.

To unlock, the following steps should be done:

1. Disable interrupts prior to the unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the NVMKEY register in two back-to-back Assembly or 'C' instructions.
3. Write the new value to the required bits.
4. Re-enable interrupts.

**REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)**

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 5 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 4 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 4 uses Shadow Set 0

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 3 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 2 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 1 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
- 1 = Single vector is presented with a shadow set
- 0 = Single vector is not presented with a shadow set

**Note 1:** These bits are ignored if the MVEC bit (INTCON<12>) = 0.

## 8.0 OSCILLATOR CONFIGURATION

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. "Oscillators with DCO"** (DS60001329) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0064GPL036 family oscillator system has the following modules and features:

- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- Primary High-Frequency Crystal Oscillator
- Secondary Low-Frequency and Low-Power Crystal Oscillator
- On-Chip Fast RC (FRC) Oscillator with User-Selectable Output Divider
- Software-Controllable Switching between Various Clock Sources
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output (REFO)

A block diagram of the oscillator system is provided in Figure 8-1.

### 8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0064GPL036 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

**REGISTER 8-6: OSCTUN: FRC TUNING REGISTER(1)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | TUN<5:0>(2) | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(2)

100000 = Center frequency – 1.5%
100001
•
•
•
111111
000000 = Center frequency; oscillator runs at 8 MHz
000001
•
•
•
011110
011111 = Center frequency + 1.5%

**Note 1:** Writes to this register require an unlock sequence. Refer to **Section 23.4 "System Registers Write Protection"** for details.

**2:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized nor tested.

**REGISTER 9-1: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER (x = A-C)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON | — | — | — | CNSTYLE | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notification (CN) Control On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx bits are used for a Change Notice event)
0 = Mismatch style (detects change from last PORTx read, CNSTATx bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

## 10.0 TIMER1

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

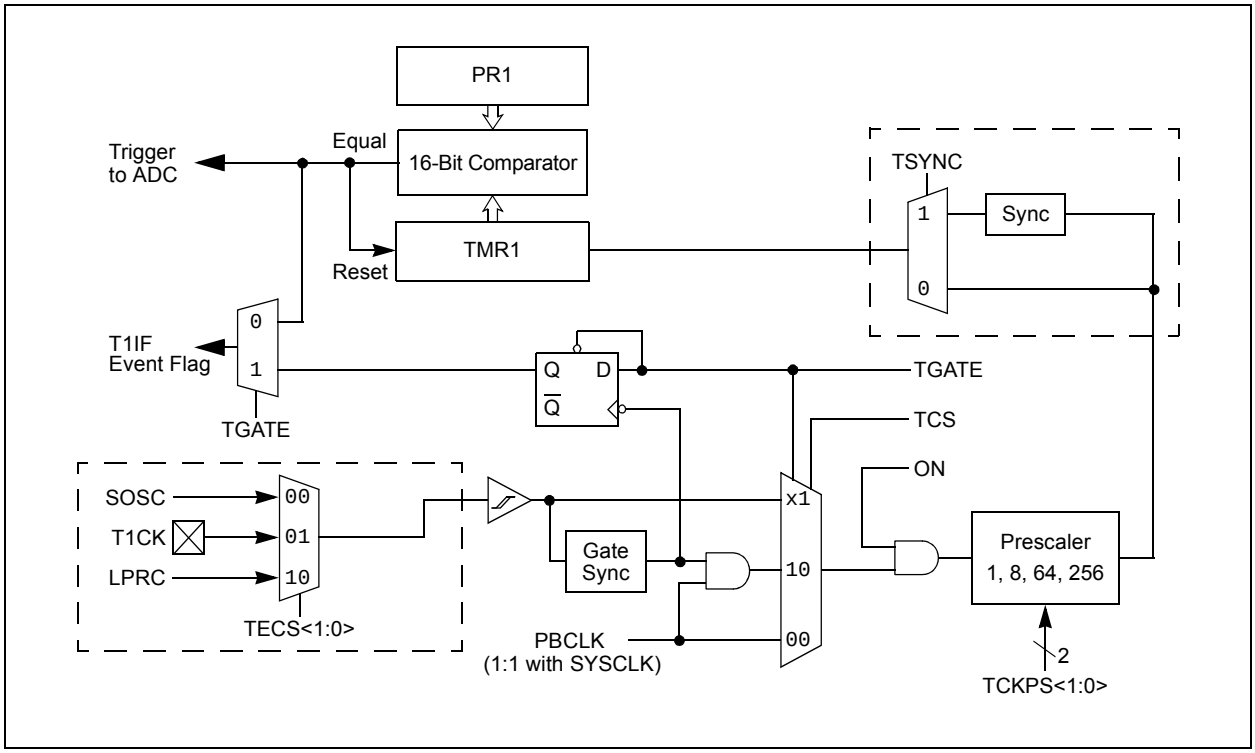
PIC32MM0064GPL036 family devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can be clocked from different sources, such as the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK), Secondary Oscillator (SOSC), T1CK pin or LPRC oscillator.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

The timer has a selectable clock prescaler and can operate in Sleep and Idle modes.

**FIGURE 10-1: TIMER1 BLOCK DIAGRAM**



**REGISTER 12-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | OETRIG | OSCNT<2:0> | | | — | OUTM<2:0>(1) | | |
| 23:16 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | POLACE | POLBDF(1) | PSSACE<1:0> | | PSSBDF<1:0>(1) | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | DT<5:0>(1) | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **OETRIG:** PWM Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1), the module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 30-28 **OSCNT<2:0>:** One-Shot Event Count bits
Extends the duration of a one-shot trigger event by an additional n clock cycles (n+1 total cycles).
111 = 7 timer count periods (8 cycles total)
110 = 6 timer count periods (7 cycles total)
101 = 5 timer count periods (6 cycles total)
100 = 4 timer count periods (5 cycles total)
011 = 3 timer count periods (4 cycles total)
010 = 2 timer count periods (3 cycles total)
001 = 1 timer count period (2 cycles total)
000 = Does not extend the one-shot trigger event (the event takes 1 timer count period)

bit 27 **Unimplemented:** Read as '0'

bit 26-24 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 23-22 **Unimplemented:** Read as '0'

bit 21 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 20 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 19-18 **PSSACE<1:0>:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

**Note 1:** These bits are implemented in MCCP modules only.

## 15.1 RTCC Control Registers

**TABLE 15-1: RTCC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | RTCCON1 | 31:16 | ALRMEN | CHIME | — | — | AMASK<3:0> | | | | ALMRPT<7:0> | | | | | | | | 0000 |
| | | 15:0 | ON | — | — | — | WRLOCK | — | — | — | RTCOE | OUTSEL<2:0> | | | — | — | — | — | 0000 |
| 0010 | RTCCON2 | 31:16 | DIV<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | FDIV<4:0> | | | | | — | — | — | — | — | — | — | — | — | CLKSEL<1:0> | | 0000 |
| 0030 | RTCSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ALMEVT | — | — | SYNC | ALMSYNC | HALFSEC | 0000 |
| 0040 | RTCTIME | 31:16 | — | HRTEN<2:0> | | | HRONE<3:0> | | | | — | MINTEN<2:0> | | | MINONE<3:0> | | | | xxxx |
| | | 15:0 | SECTEN<3:0> | | | | SECONE<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0050 | RTCDATE | 31:16 | YRTEN<3:0> | | | | YRONE<3:0> | | | | — | — | — | MTHTEN | MTHONE<3:0> | | | | 0000 |
| | | 15:0 | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | | — | — | — | — | — | WDAY<2:0> | | | 0000 |
| 0060 | ALMTIME | 31:16 | — | HRTEN<2:0> | | | HRONE<3:0> | | | | — | MINTEN<2:0> | | | MINONE<3:0> | | | | xxxx |
| | | 15:0 | SECTEN<3:0> | | | | SECONE<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0070 | ALMDATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | MTHTEN | MTHONE<3:0> | | | | 0000 |
| | | 15:0 | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | | — | — | — | — | — | WDAY<2:0> | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**REGISTER 15-5: RTCDATE: RTCC DATE REGISTERS**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | YRTEN<3:0> | | | | YRONE<3:0> | | | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MTHTEN | MTHONE<3:0> | | | |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | WDAY<2:0> | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **YRTEN<3:0>:** Binary Coded Decimal Value of Years 10-Digit bits

bit 27-24 **YRONE<3:0>:** Binary Coded Decimal Value of Years 1-Digit bits

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

**REGISTER 18-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)**

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits

For CLC1:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART1 RX input
011 = SPI1 SDO output
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin

For CLC2:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART2 RX input
011 = SPI2 SDO output
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

For CLC1:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion (EOC) event
011 = UART1 TX output
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion event
011 = UART2 TX output
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

111 = MCCP1 OCM1C output
110 = MCCP1 OCM1B output
101 = MCCP1 OCM1A output
100 = REFCLKO output
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (FSYS)
000 = CLCINA I/O pin

**REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)**

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 1
0 = The Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 1
0 = The Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

## 22.0 POWER-SAVING FEATURES

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes power-saving features for the PIC32MM0064GPL036 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

### 22.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted, and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- If WDT is enabled, the Run mode counter is not cleared upon entry to Sleep and the Sleep mode counter is reset upon entering Sleep.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC and Timer1).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The on-chip regulator enters Standby mode if the VREGS bit (PWRCON<0>) is set.
- A separate special low-power, low-voltage/ retention regulator is activated if the RETVR Configuration bit (FPOR<2>) is programmed to zero and the RETEN bit (PWRCON<1>) is set.

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than, or equal to, the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

### 22.2 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than, or equal to, the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

**REGISTER 23-10: ANCFG: BAND GAP CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS, HC | R/W-0, HS, HC | U-0 |
| | — | — | — | — | — | VBGADC | VBGCMP | — |

| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **VBGADC:** ADC Band Gap Enable bit
1 = ADC band gap is enabled
0 = ADC band gap is disabled

bit 1 **VBGCMP:** Comparator Band Gap Enable bit
1 = Comparator band gap is enabled
0 = Comparator band gap is disabled

bit 0 **Unimplemented:** Read as '0'

**FIGURE 26-5: TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS**

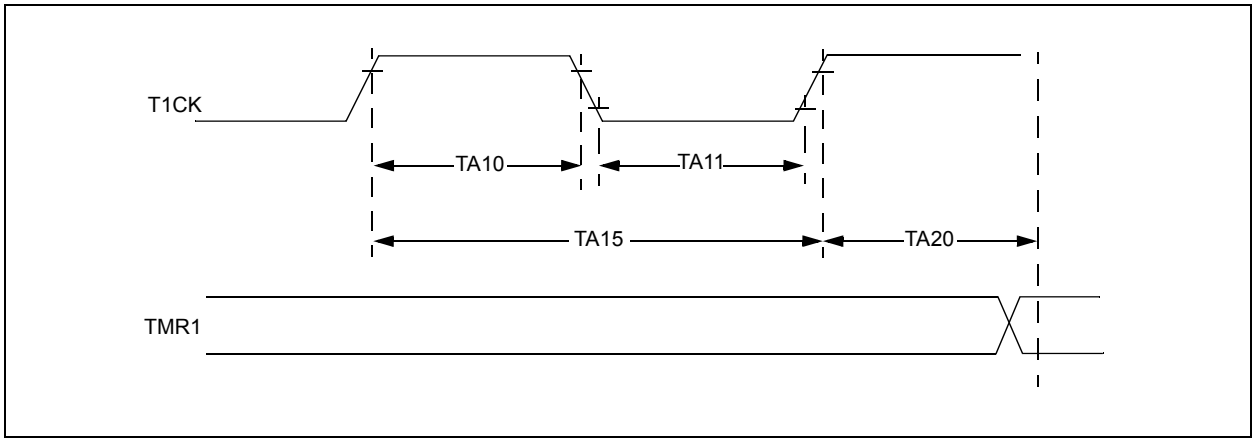



**TABLE 26-23: MCCP/SCCP TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS**

| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | | **Min** | **Max** | **Units** | **Conditions** |
| TA10 | TCKH | T1CK High Time | Synchronous | 1 | — | TPBCLK | Must also meet Parameter TA15 |
| | | | Asynchronous | 10 | — | ns | |
| TA11 | TCKL | T1CK Low Time | Synchronous | 1 | — | TPBCLK | Must also meet Parameter TA15 |
| | | | Asynchronous | 10 | — | ns | |
| TA15 | TCKP | T1CK Input Period | Synchronous | 2 | — | TPBCLK | |
| | | | Asynchronous | 20 | — | ns | |
| TA20 | TCKEXTMRL | Delay from External T1CK Clock Edge to Timer Increment | | — | 3 | TPBCLK | Synchronous mode |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 26-7: MCCP AND SCCP INPUT CAPTURE x MODE TIMING CHARACTERISTICS**

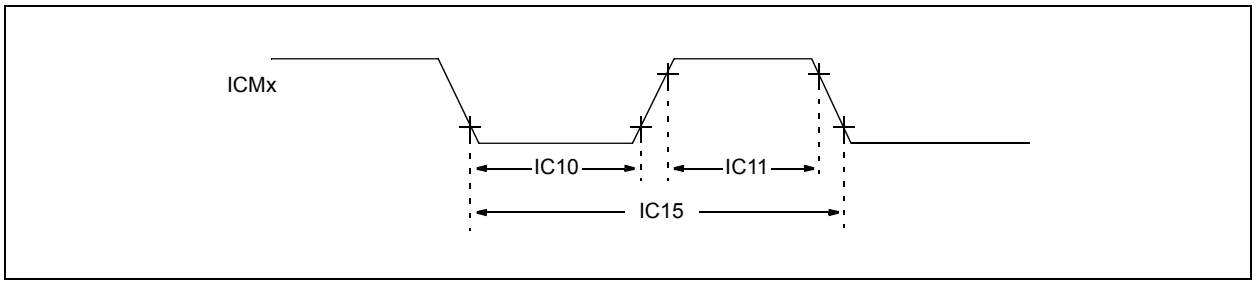
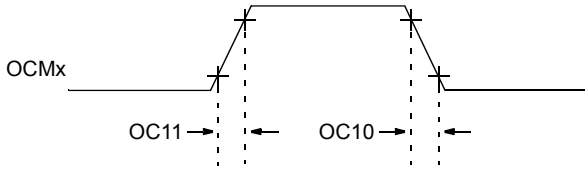



**TABLE 26-25: MCCP AND SCCP INPUT CAPTURE x MODE TIMING REQUIREMENTS**

| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min** | **Max** | **Units** | **Conditions** |
| IC10 | TICL | ICMx Input Low Time | 25 | — | ns | Must also meet Parameter IC15 |
| IC11 | TICH | ICMx Input High Time | 25 | — | ns | Must also meet Parameter IC15 |
| IC15 | TICP | ICMx Input Period | 50 | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 26-8: MCCP AND SCCP OUTPUT COMPARE x MODE TIMING CHARACTERISTICS**




**Note:** Refer to Figure 26-2 for load conditions.

**TABLE 26-26: MCCP AND SCCP OUTPUT COMPARE x MODE TIMING REQUIREMENTS**

| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min** | **Typ** | **Max** | **Units** |
| OC10 | TOCF | OCMx Output Fall Time | — | 10 | 25 | ns |
| OC11 | TOCR | OCMx Output Rise Time | — | 10 | 25 | ns |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 26-14: EJTAG TIMING CHARACTERISTICS**

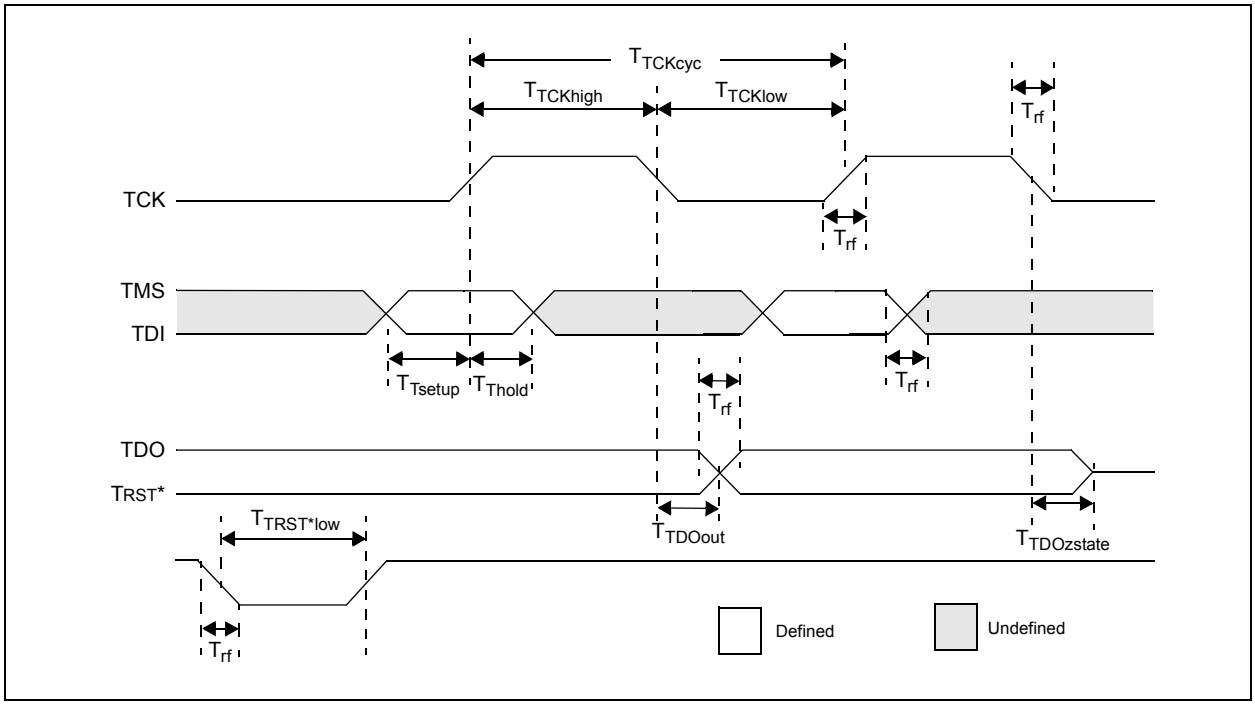



**TABLE 26-33: EJTAG TIMING REQUIREMENTS**

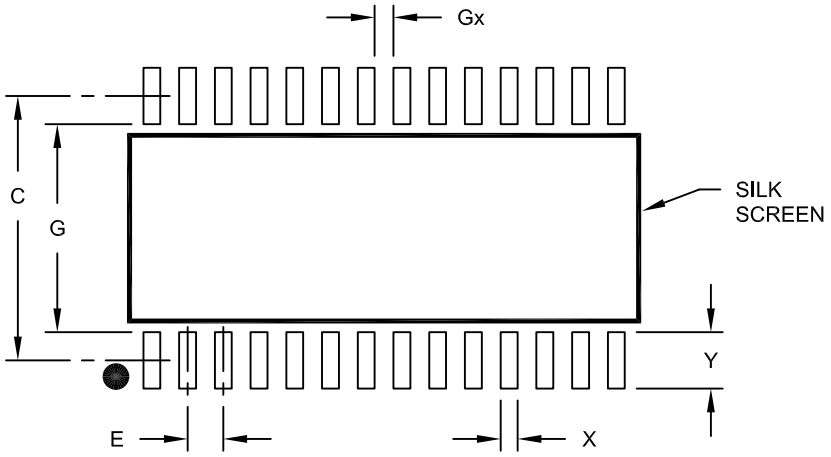
| **Operating Conditions:** 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Description(1)** | **Min** | **Max** | **Units** | **Conditions** |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | |
| EJ4 | TTSETUP | TAP Signals Setup Time before Rising TCK | 5 | — | ns | |
| EJ5 | TTHOLD | TAP Signals Hold Time after Rising TCK | 3 | — | ns | |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**NOTES:**

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width (X28) | X | | | 0.60 |
| Contact Pad Length (X28) | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:

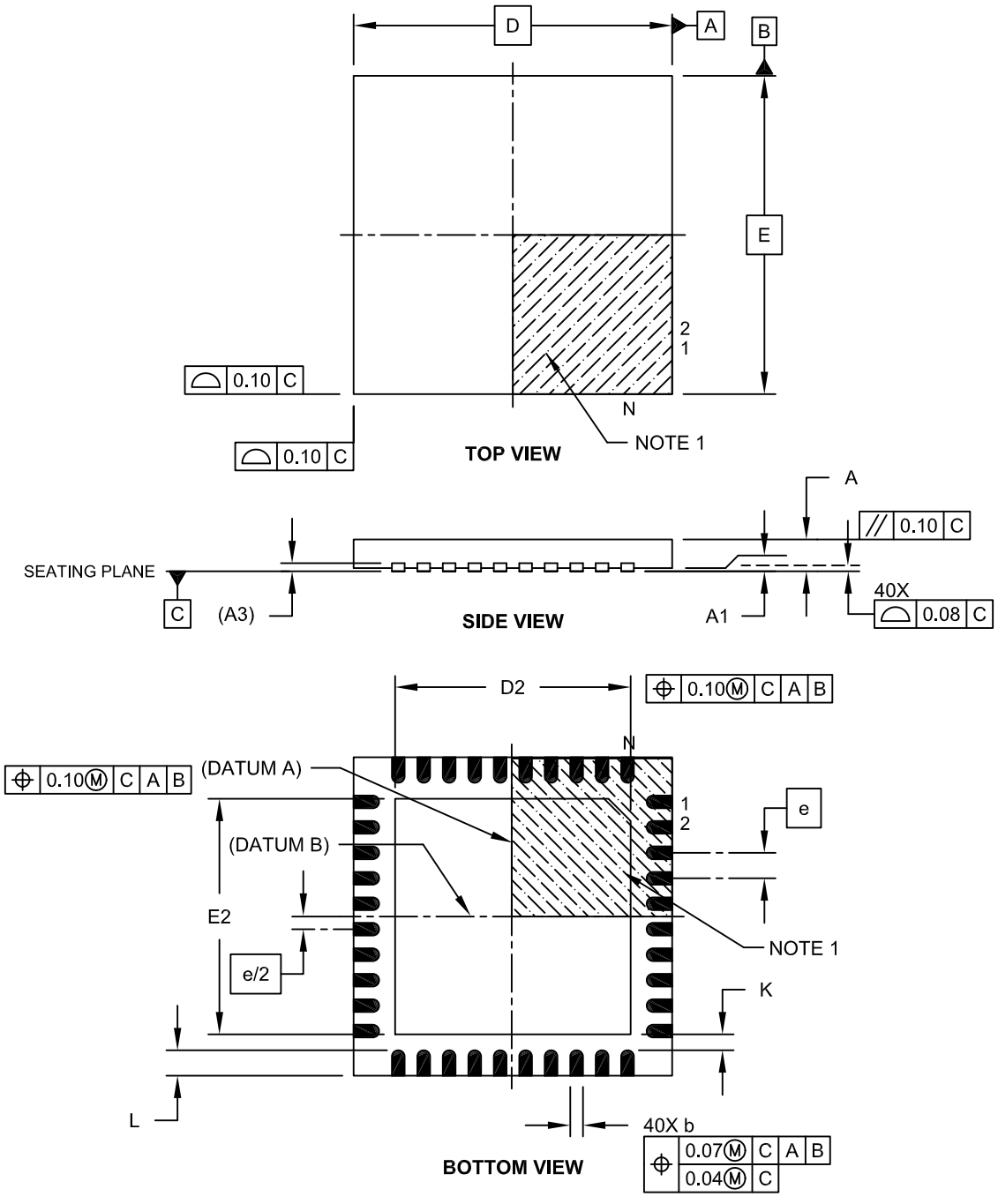
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

### 40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-156A Sheet 1 of 2

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