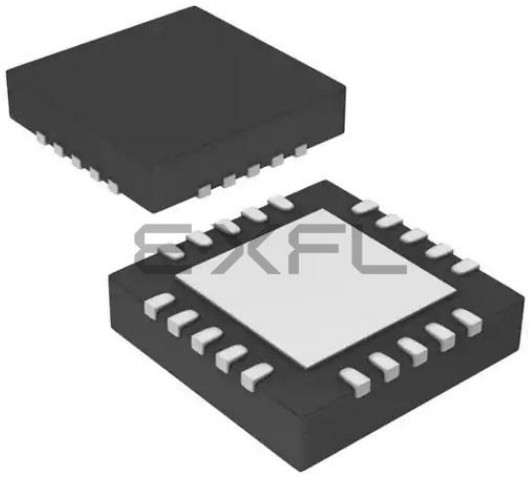

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl020t-i-ml

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.	EBASE + 0x180	CU, EXL	—	CpU (0x0B)	_general_exception_handler
RI	Execution of a reserved instruction.	EBASE + 0x180	EXL	—	RI (0x0A)	_general_exception_handler
Ov	Execution of an arithmetic instruction that overflowed.	EBASE + 0x180	EXL	—	Ov (0x0C)	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE + 0x180	EXL	—	Tr (0x0D)	_general_exception_handler
DDBL	EJTAG data address break (address only) or EJTAG data value break on load (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
DDBS	EJTAG data address break (address only) or EJTAG data value break on store (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
AdES	Store address alignment error.	EBASE + 0x180	EXL	—	ADES (0x05)	_general_exception_handler
DBE	Load or store bus error.	EBASE + 0x180	EXL	—	DBE (0x07)	_general_exception_handler
CBrk	EJTAG complex breakpoint.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIBImpr, DDBLImpr and/or DDBSImpr	—	—
Lowest Priority						

TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
UART1 Reception	_UART1_RX_VECTOR	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	Yes
UART1 Transmission	_UART1_TX_VECTOR	24	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	Yes
UART1 Error	_UART1_ERR_VECTOR	25	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
CCP1 Input Capture or Output Compare	_CCP1_VECTOR	29	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	No
CCP1 Timer	_CCT1_VECTOR	30	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	No
CCP2 Input Capture or Output Compare	_CCP2_VECTOR	31	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
CCP2 Timer	_CCT2_VECTOR	32	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
CCP3 Input Capture or Output Compare	_CCP3_VECTOR	33	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	No
CCP3 Timer	_CCT3_VECTOR	34	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	No
RESERVED	—	35	—	—	—	—	—
RESERVED	—	36	—	—	—	—	—
SPI2 Error	_SPI2_ERR_VECTOR	37	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
SPI2 Transmission	_SPI2_TX_VECTOR	38	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
SPI2 Reception	_SPI2_RX_VECTOR	39	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	Yes
UART2 Reception	_UART2_RX_VECTOR	40	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	Yes
UART2 Transmission	_UART2_TX_VECTOR	41	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
UART2 Error	_UART2_ERR_VECTOR	42	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
NVM Program or Erase Complete	_NVM_VECTOR	46	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
Core Performance Counter	_PERFORMANCE_COUNTER_VECTOR	47	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	No

REGISTER 8-5: CLKSTAT: CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	SPDIVRDY	FRCRDY

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **SPLLRDY**: PLL Lock bit
1 = PLL is locked and ready
0 = PLL is not locked

bit 6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** LPRC Oscillator Ready bit
1 = LPRC oscillator is stable and ready
0 = LPRC oscillator is not stable

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready bit
1 = SOSC is stable and ready
0 = SOSC is not stable

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready bit
1 = POSC is stable and ready
0 = POSC is not stable

bit 1 **SPDIVRDY:** System PLL (with postscaler, SPLLDIV) Clock Ready Status bit
1 = SPLLDIV is stable and ready
0 = SPLLDIV is not stable

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready bit
1 = FRC oscillator is stable and ready
0 = FRC oscillator is not stable

13.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

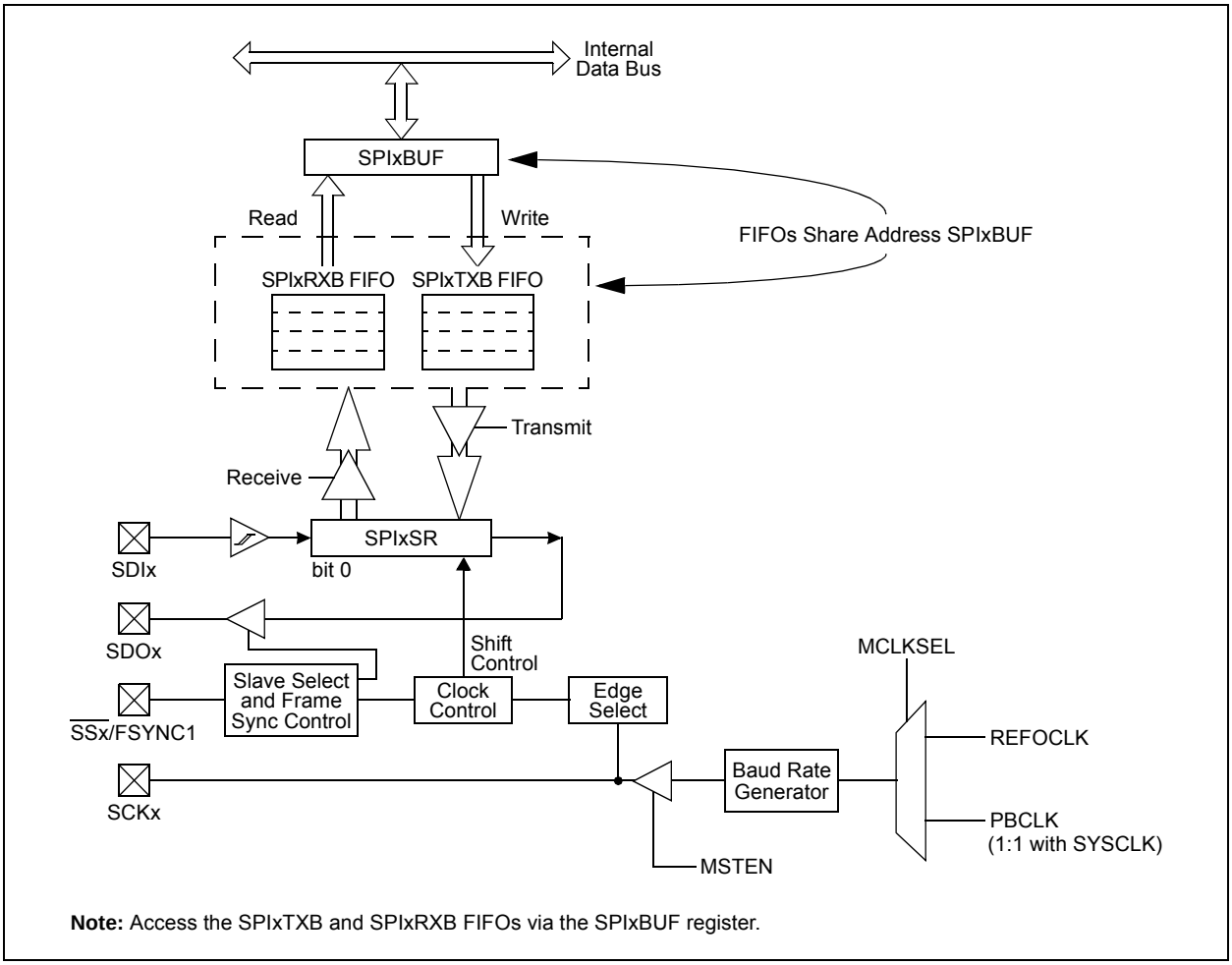
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes Support
- Four Different Clock Formats
- Enhanced Framed SPI Protocol Support
- User-Configurable 8-Bit, 16-Bit and 32-Bit Data Width
- Separate SPI FIFO Buffers for Receive and Transmit:
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable Interrupt Event on Every 8-Bit, 16-Bit and 32-Bit Data Transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol

FIGURE 13-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access the SPIxTXB and SPIxRXB FIFOs via the SPIxBUF register.

REGISTER 13-3: SPIxSTAT: SPIx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPIx Frame Error status bit
1 = Frame error is detected
0 = No frame error is detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPIx Activity Status bit
1 = SPIx peripheral is currently busy with some transactions
0 = SPIx peripheral is currently Idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** SPIx Transmit Underrun (TUR) bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When the SPIx Shift register is empty
0 = When the SPIx Shift register is not empty

bit 6 **SPIROV:** SPIx Receive Overflow (ROV) Flag bit
1 = New data is completely received and discarded; the user software has not read the previous data in the SPIxBUF register
0 = No overflow has occurred
This bit is set in hardware; it can only be cleared (= 0) in software.

bit 5 **SPIRBE:** SPIx RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CPU Read Pointer (CRPTR) = SPI Write Pointer (SWPTR))
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

TABLE 16-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(3)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	ADC1BUF14	31:16	ADC1BUF14<31:0>																0000
		15:0																	0000
07F0	ADC1BUF15	31:16	ADC1BUF15<31:0>																0000
		15:0																	0000
0800	AD1CON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON		SIDL	—	—	FORM<2:0>			SSRC<3:0>				MODE12	ASAM	SAMP	DONE	0000
0810	AD1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	—	0000
0820	AD1CON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	EXTSAM	—	SAMC<4:0>					ADCS<7:0>								0000
0840	AD1CHS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CH0NA<2:0>			CH0SA<4:0>					0000
0850	AD1CSS	31:16	—	CSS<30:28>			—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CSS<13:0>(1,2)														0000
0870	AD1CON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ASEN	LPEN	—	BGREQ	—	—	ASINT<1:0>		—	—	—	—	WM<1:0>		CM<1:0>		0000
0880	AD1CHIT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CHH<13:0>(1,2)														0000

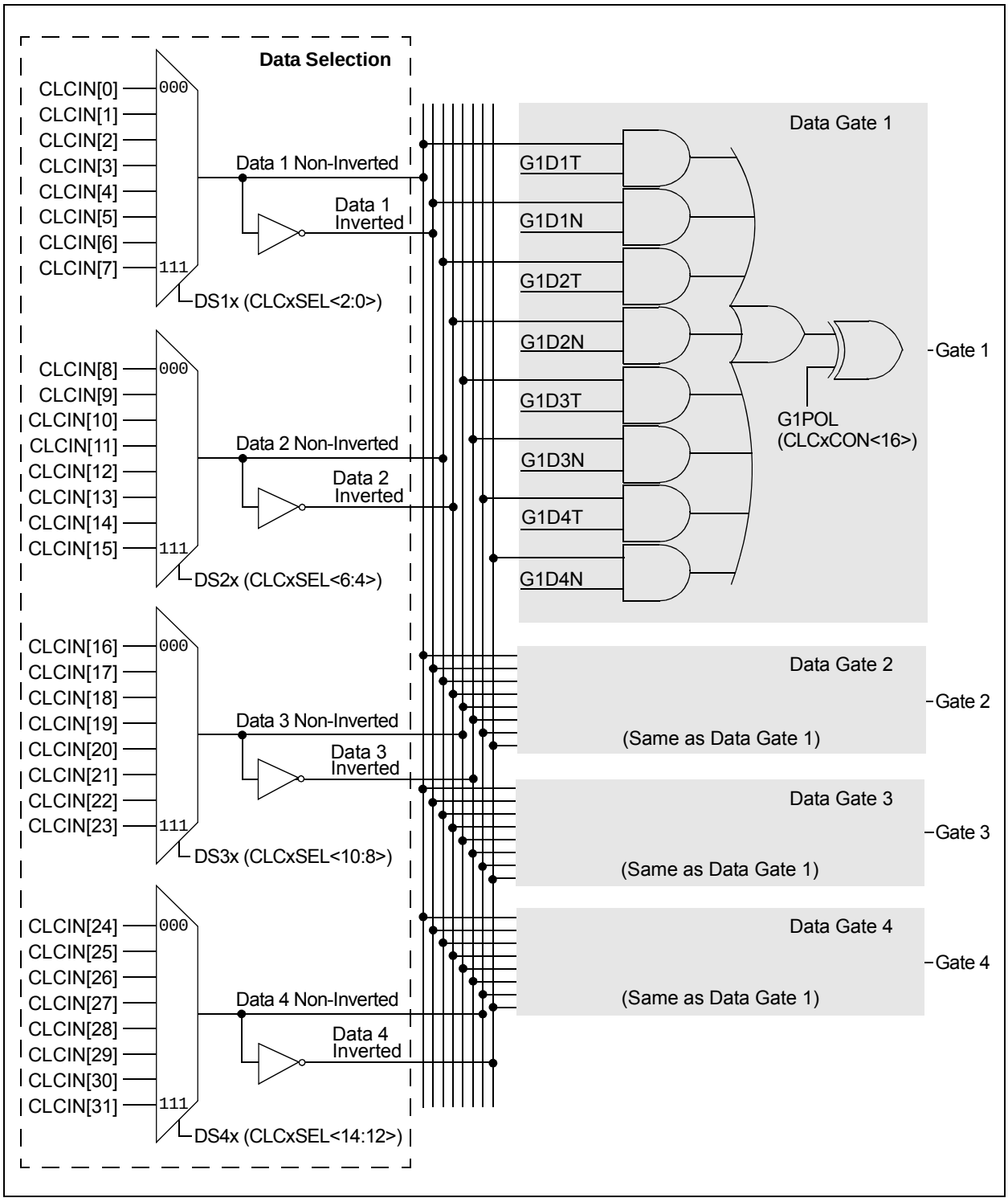
Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

2: The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

3: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

FIGURE 18-3: CLCx INPUT SOURCE SELECTION DIAGRAM



REGISTER 19-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 AND 2) (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
High-to-low transition only.
If CPOL = 1 (inverted polarity):
Low-to-high transition only.
01 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
Low-to-high transition only.
If CPOL = 1 (inverted polarity):
High-to-low transition only.
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)
1 = Non-inverting input connects to the internal reference defined by the CVREFSEL bit in the CMSTAT register
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = Inverting input of the comparator connects to the band gap reference voltage
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

REGISTER 20-1: DAC1CON: CDAC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DACDAT<4:0>				
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	—	—	—	—	—	DACOE
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **DACDAT<4:0>:** CDAC Voltage Reference Selection bits

11111 = (DACDAT<4:0> * VREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits
•
•
•
00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled
0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** CDAC Voltage Reference Output Enable bit

1 = Voltage level is output on the CDAC1 pin
0 = Voltage level is disconnected from the CDAC1 pin

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** CDAC Voltage Reference Source Select bits

11 = Reference voltage is AVDD
10 = No reference is selected – output is AVSS
01 = Reference voltage is the VREF+ input pin voltage
00 = No reference is selected – output is AVSS

TABLE 23-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

TABLE 26-12: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**
DVR10	VBG	Band Gap Reference Voltage	—	1.2	—	V	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 1.9V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Series Resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	0.9	—	1.2	V	RETEN = 1, RETVR (FPOR<2>) = 0

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-13: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ(2)**	**Max**	**Units**
DC18	VHLVD(1)	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0101	3.25	—	3.63	V
			HLVDL<3:0> = 0110	2.95	—	3.30	V
			HLVDL<3:0> = 0111	2.75	—	3.09	V
			HLVDL<3:0> = 1000	2.65	—	2.98	V
			HLVDL<3:0> = 1001	2.45	—	2.80	V
			HLVDL<3:0> = 1010	2.35	—	2.69	V
			HLVDL<3:0> = 1011	2.25	—	2.55	V
			HLVDL<3:0> = 1100	2.15	—	2.44	V
			HLVDL<3:0> = 1101	2.08	—	2.33	V
			HLVDL<3:0> = 1110	2.00	—	2.22	V
DC101	VTHL	HLVD Voltage on LVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.2	—	V

Note 1: Trip points for values of HLVD<3:0>, from '0000' to '0100', are not implemented.

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

26.2 AC Characteristics and Timing Parameters

FIGURE 26-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

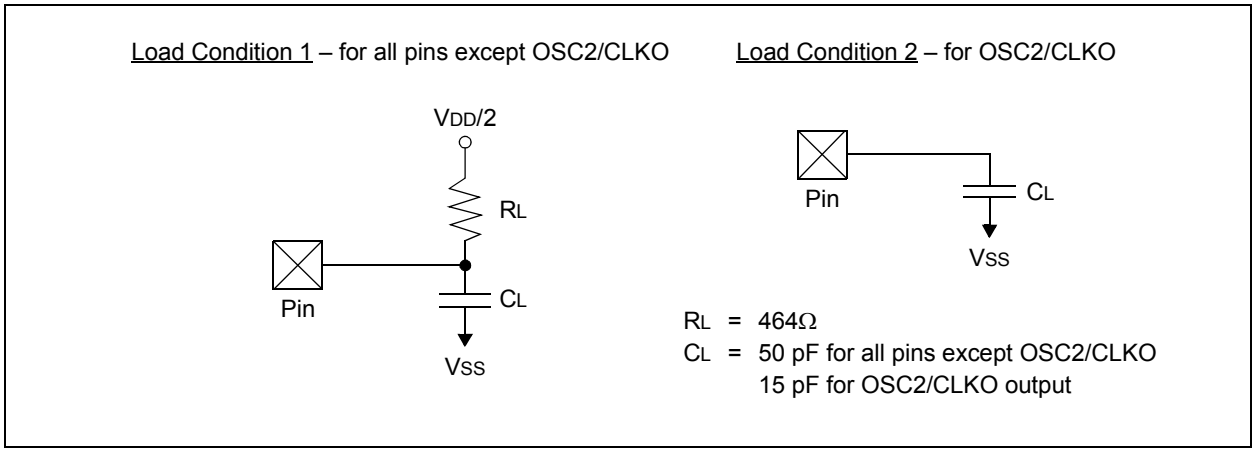


TABLE 26-16: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
DO50	COSCO	OSC2/CLKO Pin	—	15	pF	In XT and HS modes when external clock is used to drive OSC1/CLKI
DO56	CIO	All I/O Pins and OSC2	—	50	pF	EC mode

FIGURE 26-14: EJTAG TIMING CHARACTERISTICS

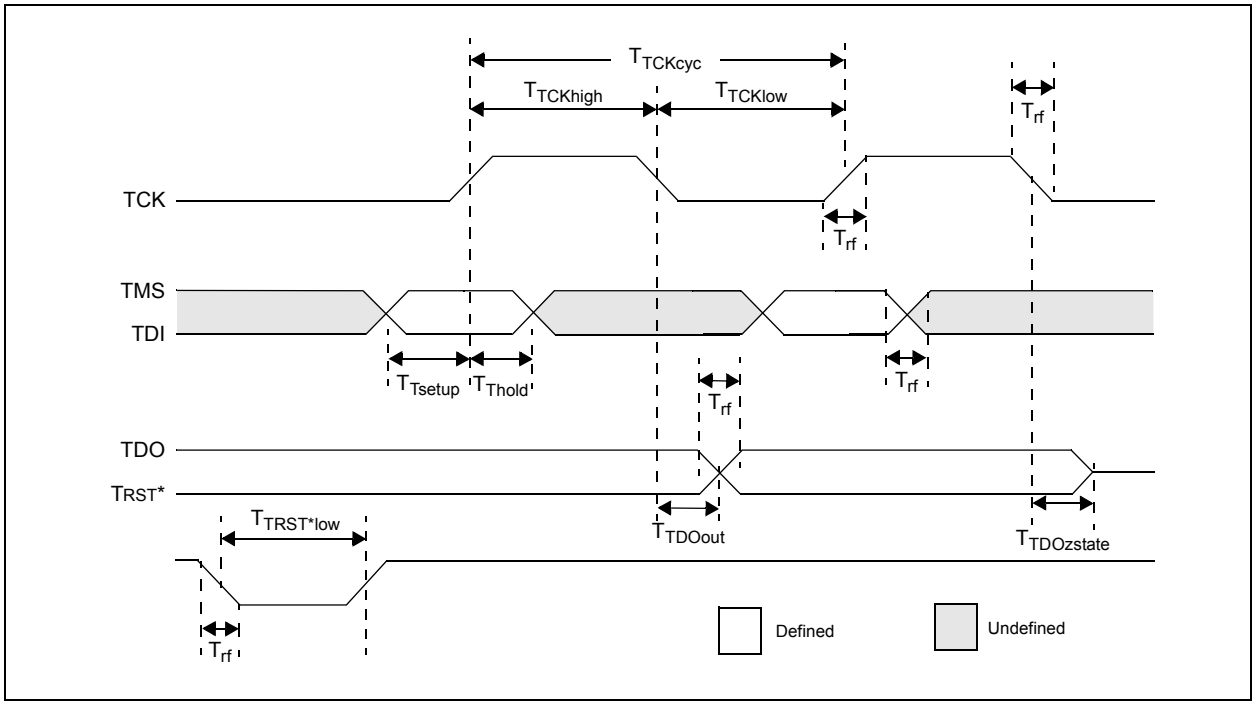


TABLE 26-33: EJTAG TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)						
Param. No.	**Symbol**	**Description(1)**	**Min**	**Max**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	
EJ2	TTCKHIGH	TCK High Time	10	—	ns	
EJ3	TTCKLOW	TCK Low Time	10	—	ns	
EJ4	TTSETUP	TAP Signals Setup Time before Rising TCK	5	—	ns	
EJ5	TTHOLD	TAP Signals Hold Time after Rising TCK	3	—	ns	
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	

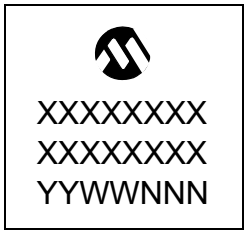
Note 1: These parameters are characterized but not tested in manufacturing.

27.1 Package Marking Information (Continued)

28-Lead SSOP

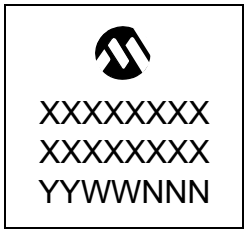
Example

28-Lead QFN



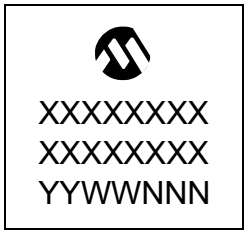
Example

28-Lead UQFN



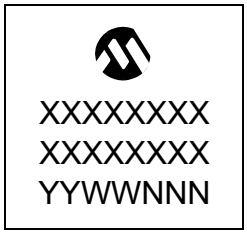
Example

36-Lead VQFN



Example

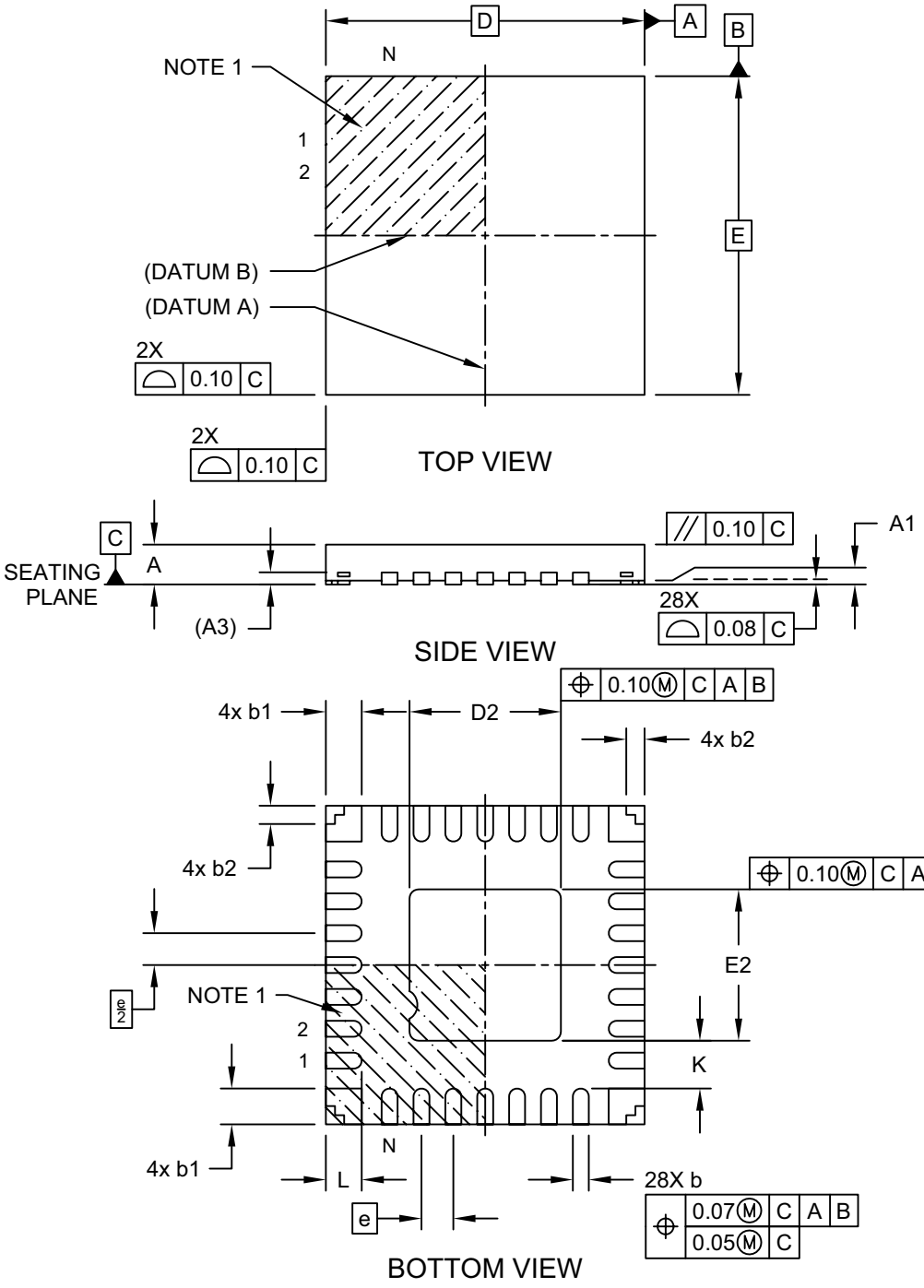
40-Lead UQFN



Example

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

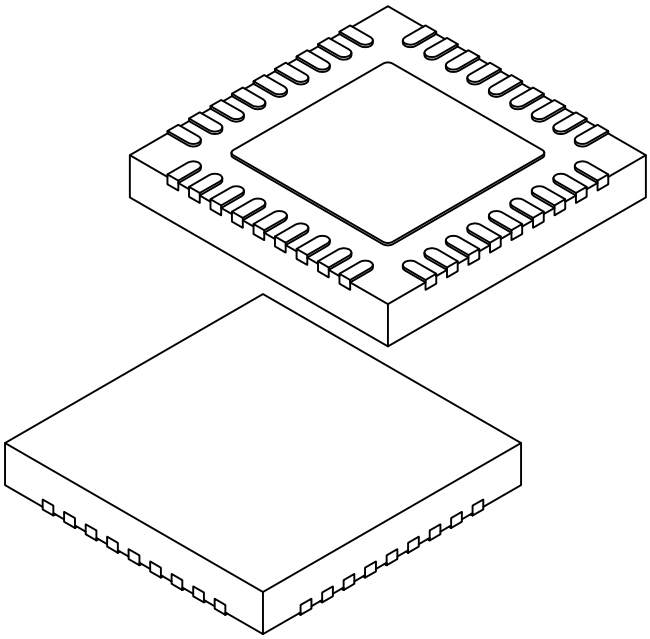
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.45	0.55	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

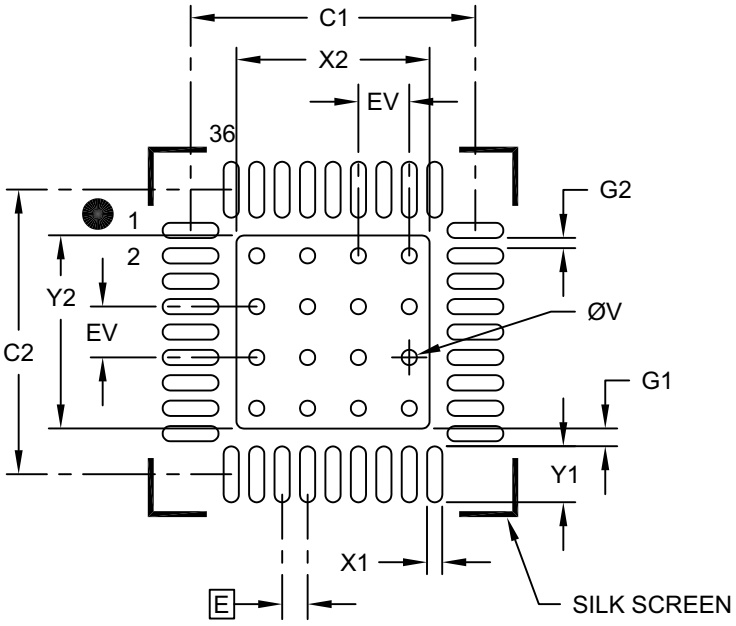
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-272B-M2 Sheet 2 of 2

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.60	
Contact Pad Spacing	C2		5.60	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			1.10
Contact Pad to Center Pad (X36)	G1	0.35		
Space Between Contact Pads (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

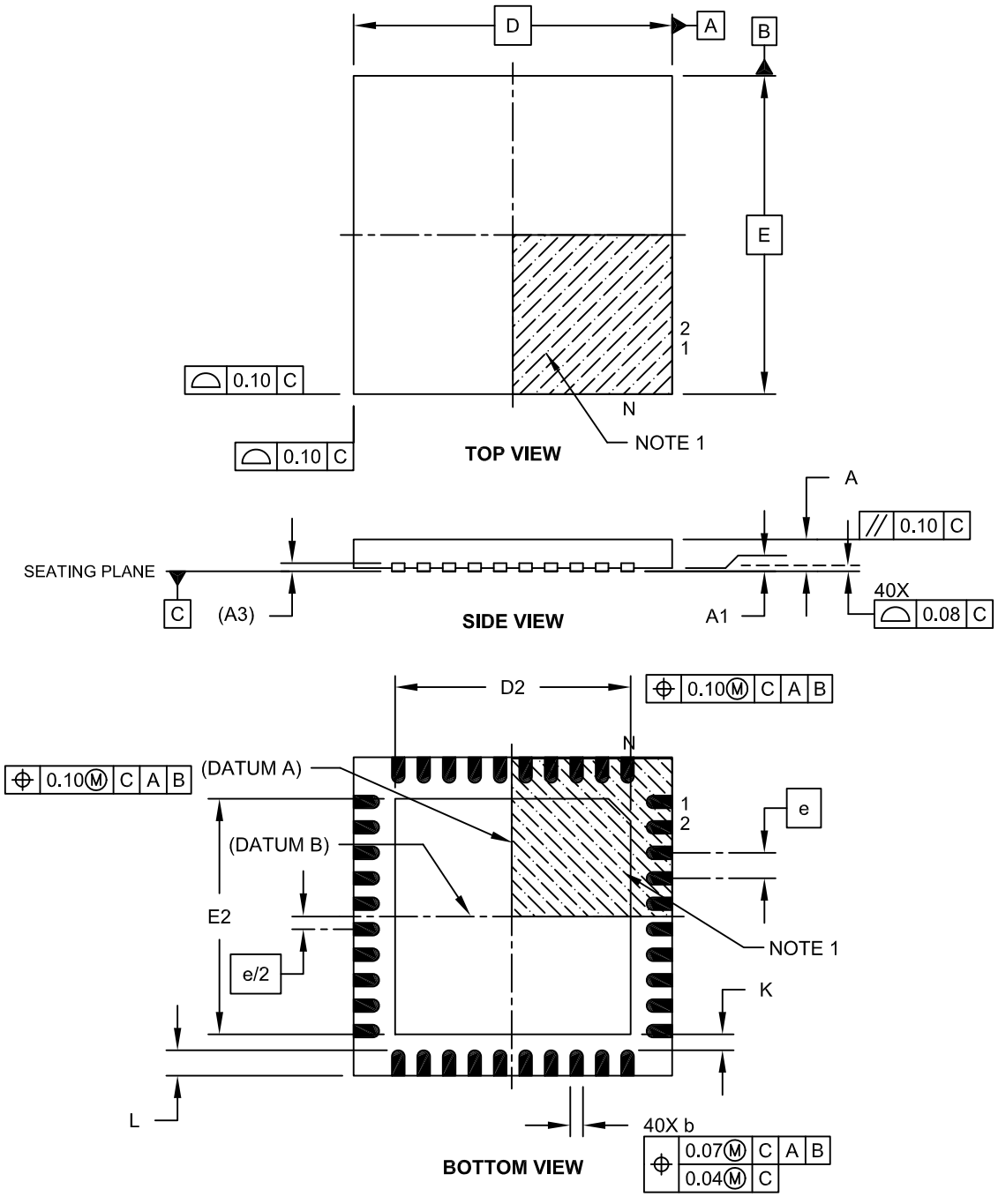
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

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NOTES: