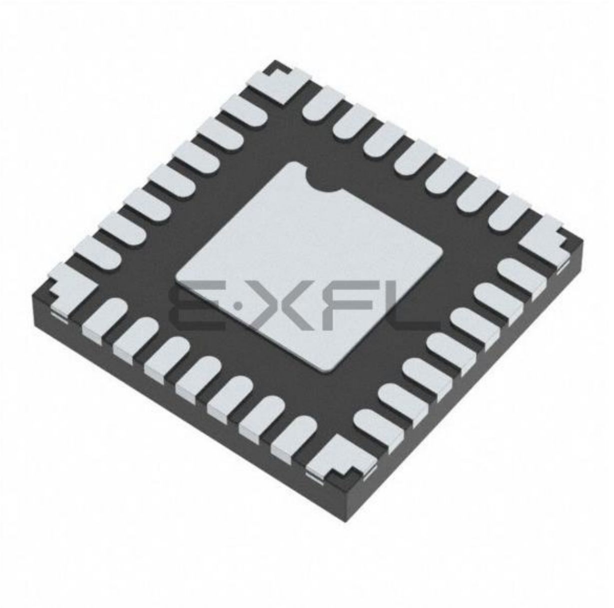

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl028-i-m6

NOTES:

3.0 CPU

Note:	This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0064GPL036 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

3.1 Features

The PIC32MM0064GPL036 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
  - Multiply-add and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero and one detect instructions
  - `WAIT` instruction
  - Conditional move instructions
  - Vectored interrupts
  - Atomic interrupt enable/disable
  - One GPR shadow set to minimize latency of interrupts
  - Bit field manipulation instructions
- microMIPS™ Instruction Set:
  - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
  - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
  - Added seventeen new and thirty-five MIPS32® corresponding commonly used instructions in 16-bit opcode format.
  - Stack Pointer implicit in instruction.
  - MIPS32 assembly and ABI compatible.
- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
  - Configurable using high-performance multiplier array.
  - Maximum issue rate of one 32x16 multiply per clock.
  - Maximum issue rate of one 32x32 multiply every other clock.
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
  - No minimum frequency: 0 MHz.
  - Power-Down mode (triggered by `WAIT` instruction).
- EJTAG Debug/Profiling:
  - CPU control with start, stop and single stepping.
  - Software breakpoints via the `SDBBP` instruction.
  - Optional simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
  - PC and/or load/store address sampling for profiling.
  - Performance counters.
  - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0064GPL036 family processor core is shown in Figure 3-1.

The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (`MFHI`) and Move-From-LO (`MFLO`) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, `MUL`, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit `MFLO` instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (`MADD`) and Multiply-Subtract (`MSUB`), are used to perform the multiply-accumulate and multiply-subtract operations. The `MADD` instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the `MSUB` instruction multiplies two operands and then subtracts the product from the HI and LO registers. The `MADD` and `MSUB` operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information is available by accessing the CP0 registers listed in Table 3-2.

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a ‘1’ to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as ‘0’

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating-Point Unit bit
0 = Floating-Point Unit is not implemented

5.0 FLASH PROGRAM MEMORY

Note:	This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0064GPL036 family devices contain an internal Flash program memory for executing user code. The Program and Boot Flash Memory can be write-protected. The erase page size is 512 32-bit words. The program row size is 64 32-bit words. The memory can be programmed by rows or by two 32-bit words.

The devices implement an Error Correcting Code (ECC). The memory control block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC bits. The ECC provides improved resistance to Flash errors. The ECC single-bit error will be transparently corrected. The ECC double-bit error results in a bus error exception.

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is described in **Section 5. "Flash Programming"** in the *"PIC32 Family Reference Manual"*. EJTAG programming is performed using the JTAG port of the device. ICSP programming requires fewer connections than for EJTAG programming. The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site.

5.1 Flash Controller Registers Write Protection

The NVMPWP and NVMBWP registers, and the WR bit in the NVMCON register are protected (locked) from an accidental write. A special unlock sequence is required to modify the content of these registers or bits.

To unlock, the following steps should be done:

1. Disable interrupts prior to the unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the NVMKEY register in two back-to-back Assembly or 'C' instructions.
3. Write the new value to the required bits.
4. Re-enable interrupts.

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	VS<6:0>						
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22-16 **VS<6:0>**: Vector Spacing bits

Spacing Between Vectors:
0000000 = 0 Bytes
0000001 = 8 Bytes
0000010 = 16 Bytes
0000100 = 32 Bytes
0001000 = 64 Bytes
0010000 = 128 Bytes
0100000 = 256 Bytes
1000000 = 512 Bytes
All other values are reserved. The operation of this device is undefined if a reserved value is written to this field. If MVEC = 0, this field is ignored.

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MVEC:** Multivector Configuration bit

1 = Interrupt controller configured for Multivectored mode
0 = Interrupt controller configured for Single Vectored mode

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of Group Priority 7 or lower start the interrupt proximity timer
110 = Interrupts of Group Priority 6 or lower start the interrupt proximity timer
101 = Interrupts of Group Priority 5 or lower start the interrupt proximity timer
100 = Interrupts of Group Priority 4 or lower start the interrupt proximity timer
011 = Interrupts of Group Priority 3 or lower start the interrupt proximity timer
010 = Interrupts of Group Priority 2 or lower start the interrupt proximity timer
001 = Interrupts of Group Priority 1 start the interrupt proximity timer
000 = Disables interrupt proximity timer

bit 7-5 **Unimplemented:** Read as ‘0’

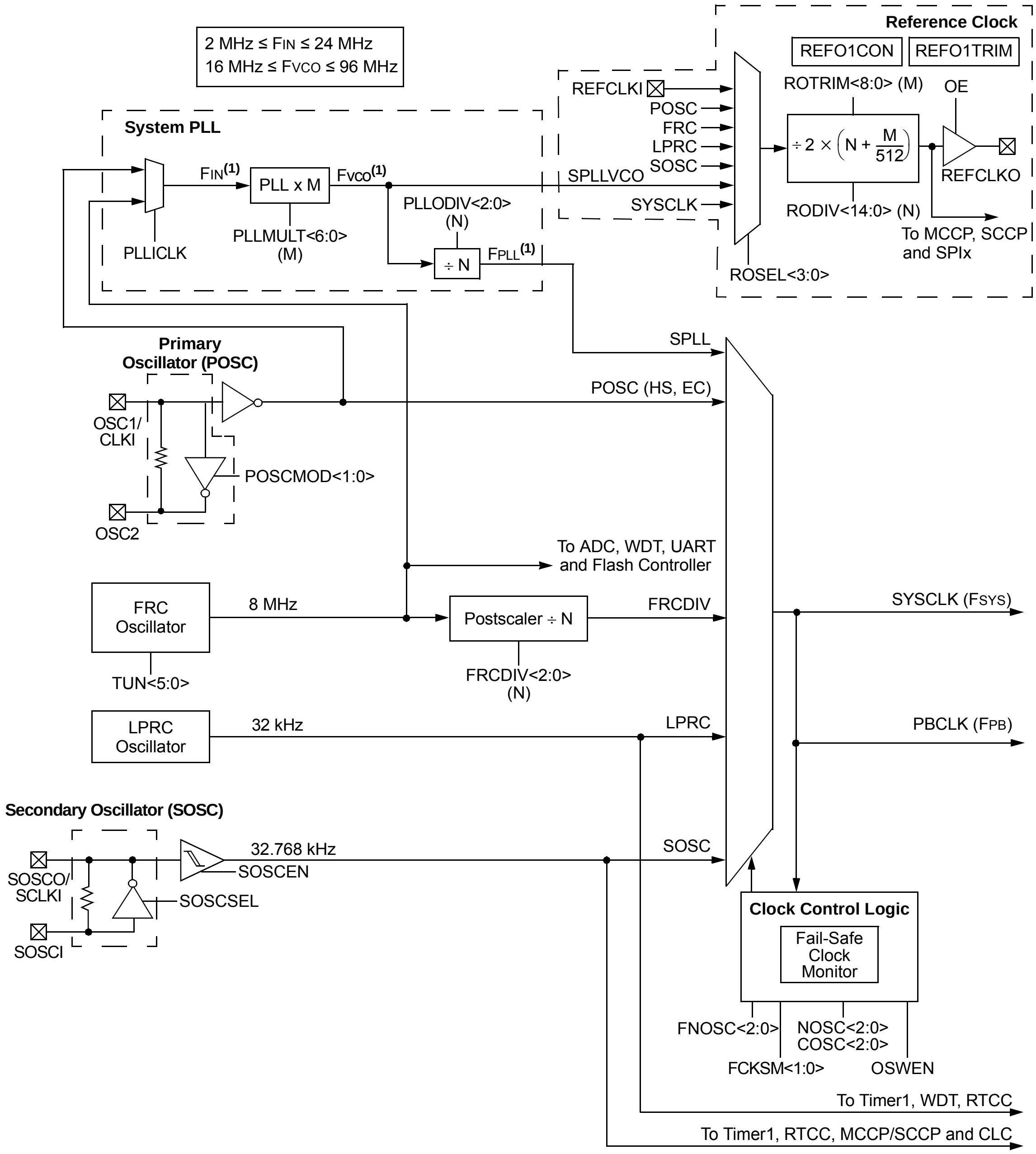
bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

FIGURE 8-1: PIC32MM0064GPL036 FAMILY OSCILLATOR DIAGRAM



Note 1: Refer to Table 26-18 in **Section 26.0 “Electrical Characteristics”** for frequency limitations.

9.8.5 OUTPUT MAPPING

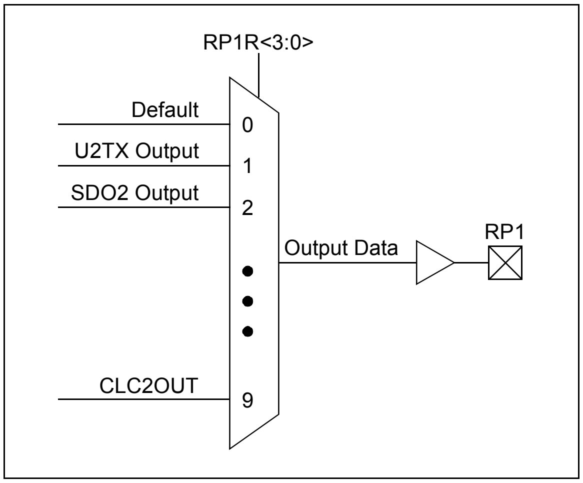
The RPORx registers are used to assign the peripheral output to the required remappable pin, RPn. Each RPORx register contains 4-bit fields corresponding to the remappable pins. A special value is defined for each peripheral output. This value should be written to the remappable pin bit field in the RPORx register to connect the peripheral output to the RPn pin. All possible (implemented) values for the peripheral's outputs are listed in Table 9-3.

Example 9-2 and Figure 9-3 illustrate the peripheral's output selection for the remappable pin.

EXAMPLE 9-2: UART2 TX OUTPUT ASSIGNMENT TO RP13/RB13 PIN

```
RPOR4bits.RP13R = 1;        // connect UART2 TX (= 1)
                            // to RP13 pin
```

FIGURE 9-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RP1



9.8.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MM0064GPL036 family devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

9.8.6.1 Control Register Lock

Under normal operation, the RPORx and RPINRx registers can be written, but they can also be locked to prevent accidental writes. This feature is controlled by the IOLOCK bit in the RPCON register. If the IOLOCK bit is set, then the contents of the RPORx and RPINRx registers cannot be changed.

To modify the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 23.4 "System Registers Write Protection"** for details.

TABLE 9-3: OUTPUT PIN SELECTION

Output Function Number	Function	Output Name
0	None (not connected)	—
1	U2TX	UART2 Transmit
2	$\overline{\text{U2RTS}}$	UART2 Request-to-Send
3	SDO2	SPI2 Data Output
4	SCK2OUT	SPI2 Clock Output
5	SS2OUT	SPI2 Slave Select Output
6	OCM2	SCCP2 Output Compare
7	OCM3	SCCP3 Output Compare
8	CLC1OUT	CLC1 Output
9	CLC2OUT	CLC2 Output

11.0 WATCHDOG TIMER (WDT)

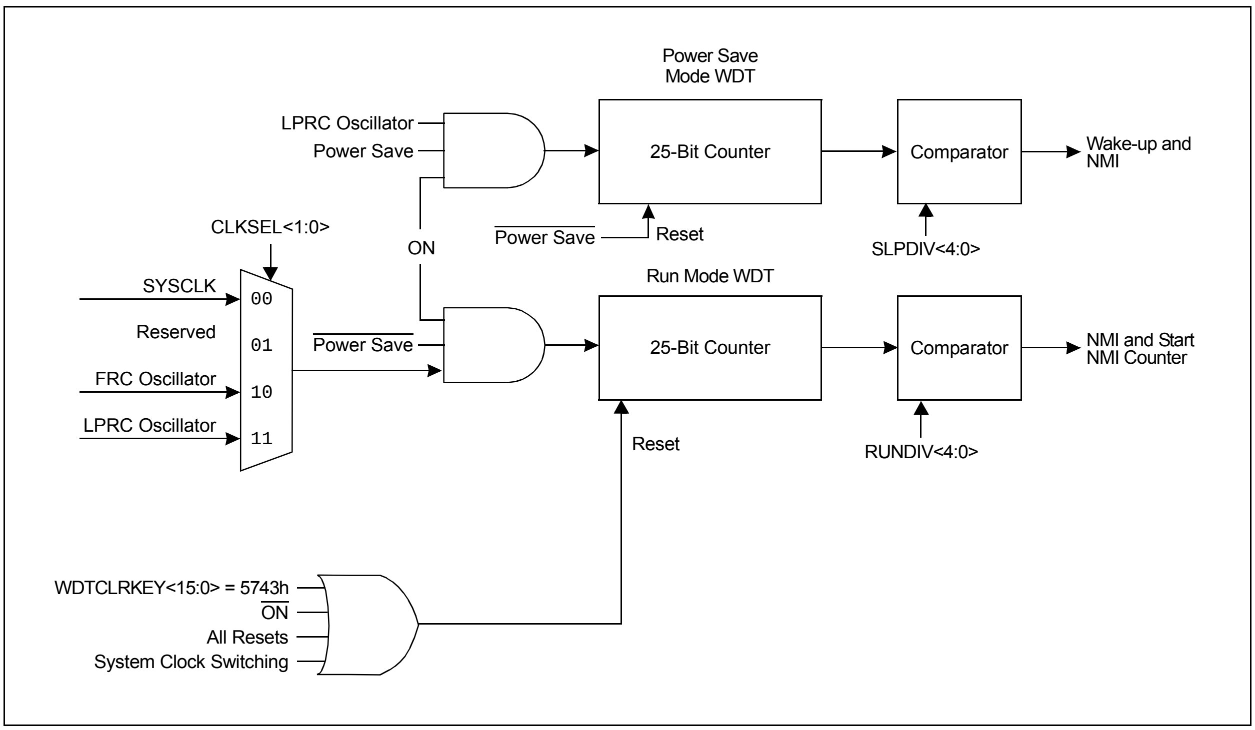
> **Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. "Dual Watchdog Timer"** (DS60001365) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 11-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R/W-y
	CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits

To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to this location using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)

1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RUNDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits

On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

bit 7-6 **CLKSEL<1:0>:** Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits

On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits

On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit

On Reset, this bit is set to the value of the WINDIS Configuration bit in FWDT.

1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

TABLE 12-1: MCCP/SCCP REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0100	CCP1CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0110	CCP1CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0120	CCP1CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0130	CCP1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0140	CCP1TMR	31:16	CCP1 TMRH<15:0>																0000
		15:0	CCP1 TMRL<15:0>																0000
0150	CCP1PR	31:16	CCP1 PRH<15:0>																0000
		15:0	CCP1 PRL<15:0>																0000
0160	CCP1RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0170	CCP1RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0180	CCP1BUF	31:16	CCP1 BUFH<15:0>																0000
		15:0	CCP1 BUFL<15:0>																0000
0200	CCP2CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0210	CCP2CON2	31:16	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0220	CCP2CON3	31:16	OETRIG	—	—	—	—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0230	CCP2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0240	CCP2TMR	31:16	CCP2 TMRH<15:0>																0000
		15:0	CCP2 TMRL<15:0>																0000
0250	CCP2PR	31:16	CCP2 PRH<15:0>																0000
		15:0	CCP2 PRL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 12-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 7-6 **TMRPS<1:0>:** CCPx Time Base Prescale Select bits

- `11` = 1:64 prescaler
- `10` = 1:16 prescaler
- `01` = 1:4 prescaler
- `00` = 1:1 prescaler

bit 5 **T32:** 32-Bit Time Base Select bit

- `1` = 32-bit time base for timer, single edge output compare or input capture function
- `0` = 16-bit time base for timer, single edge output compare or input capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit

- `1` = Input Capture mode
- `0` = Output Compare/PWM or Timer mode (exact function is selected by the MOD<3:0> bits)

bit 3-0 **MOD<3:0>:** CCPx Mode Select bits

CCSEL = `1` (Input Capture modes):

- `1xxx` = Reserved
- `011x` = Reserved
- `0101` = Capture every 16th rising edge
- `0100` = Capture every 4th rising edge
- `0011` = Capture every rising and falling edge
- `0010` = Capture every falling edge
- `0001` = Capture every rising edge
- `0000` = Capture every rising and falling edge (Edge Detect mode)

CCSEL = `0` (Output Compare modes):

- `1111` = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
- `1110` = Reserved
- `110x` = Reserved
- `10xx` = Reserved
- `0111` = Variable Frequency Pulse mode
- `0110` = Center-Aligned Pulse Compare mode, buffered
- `0101` = Dual Edge Compare mode, buffered
- `0100` = Dual Edge Compare mode
- `0011` = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
- `0010` = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
- `0001` = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
- `0000` = 16-Bit/32-Bit Timer mode: Output functions are disabled

Note 1: This control bit has no function in Input Capture modes.

2: This control bit has no function when TRIGEN = `0`.

3: Values greater than ‘`0011`’ will cause a FIFO buffer overflow in Input Capture mode.

REGISTER 17-1: CRCCON: CRC CONTROL REGISTER (CONTINUED)

bit 2 **MOD:** CRC Calculation Mode bit
1 = Alternate mode
0 = Legacy mode

bit 1-0 **Unimplemented:** Read as ‘0’

REGISTER 17-2: CRCXOR:CRC XOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	X<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	X<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **X<31:1>:** XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 20 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

bit 19 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 3
0 = The Data Source 2 signal is disabled for Gate 3

bit 18 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3

bit 17 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 3
0 = The Data Source 1 signal is disabled for Gate 3

bit 16 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

REGISTER 19-1: CMSTAT: COMPARATOR MODULE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	—	C2EVT	C1EVT
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SIDL	—	—	—	—	CVREFSEL
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-18 **Unimplemented:** Read as ‘0’

bit 17 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 16 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all enabled comparators in Idle mode

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **CVREFSEL:** Comparator Reference Voltage Select Enable bit
1 = External voltage reference from the VREF+ pin is selected
0 = Voltage from CDAC1 is selected

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
`110` and `111` = Reserved (selects Fast RC (FRC) Oscillator with Divide-by-N)
`101` = Low-Power RC Oscillator (LPRC)
`100` = Secondary Oscillator (SOSC)
`011` = Reserved
`010` = Primary Oscillator (XT, HS, EC)
`001` = Primary or FRC Oscillator with PLL
`000` = Fast RC (FRC) Oscillator with Divide-by-N

REGISTER 23-6: FSEC/AFSEC: CODE-PROTECT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	CP	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **CP:** Code Protection Enable bit
`1` = Code protection is disabled
`0` = Code protection is enabled

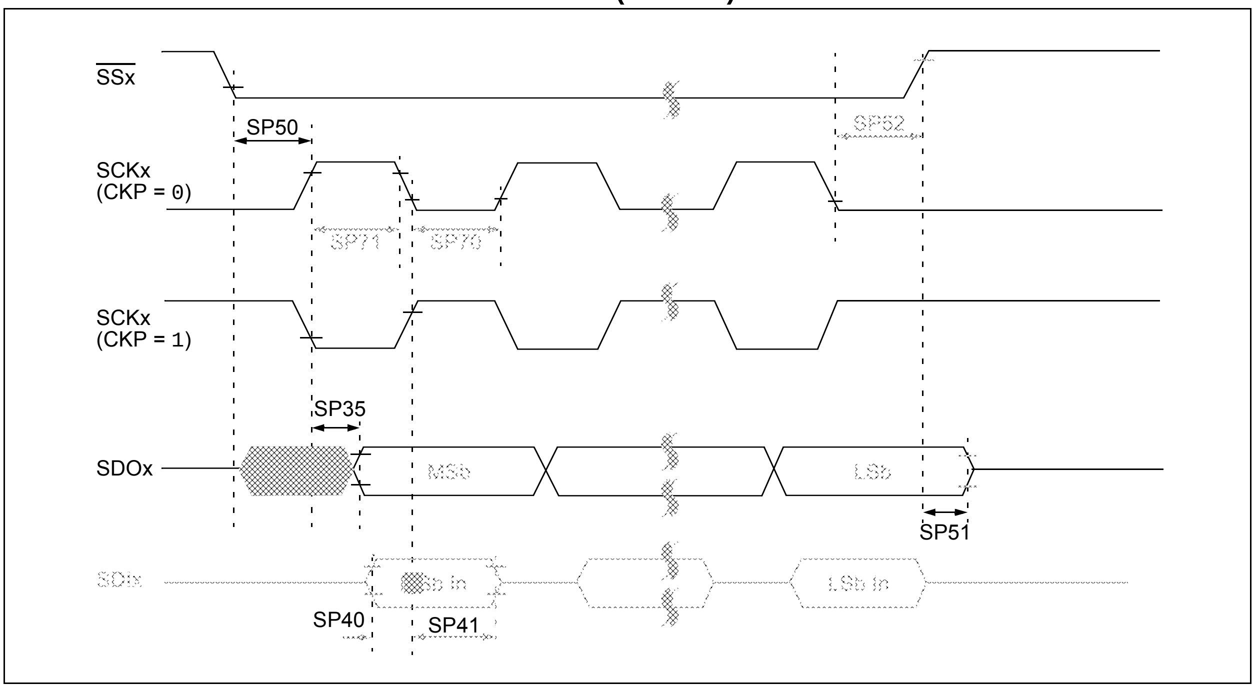
bit 30-0 **Reserved:** Program as ‘`1`’

TABLE 26-28: SPIx MODULE MASTER MODE TIMING REQUIREMENTS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param. No.	**Symbol**	**Characteristics[(1)]**	**Min**	**Max**	**Units**
SP10	TscL, TscH	SCKx Output Low or High Time	10	—	ns
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	7	ns
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	7	—	ns
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	7	—	ns
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns

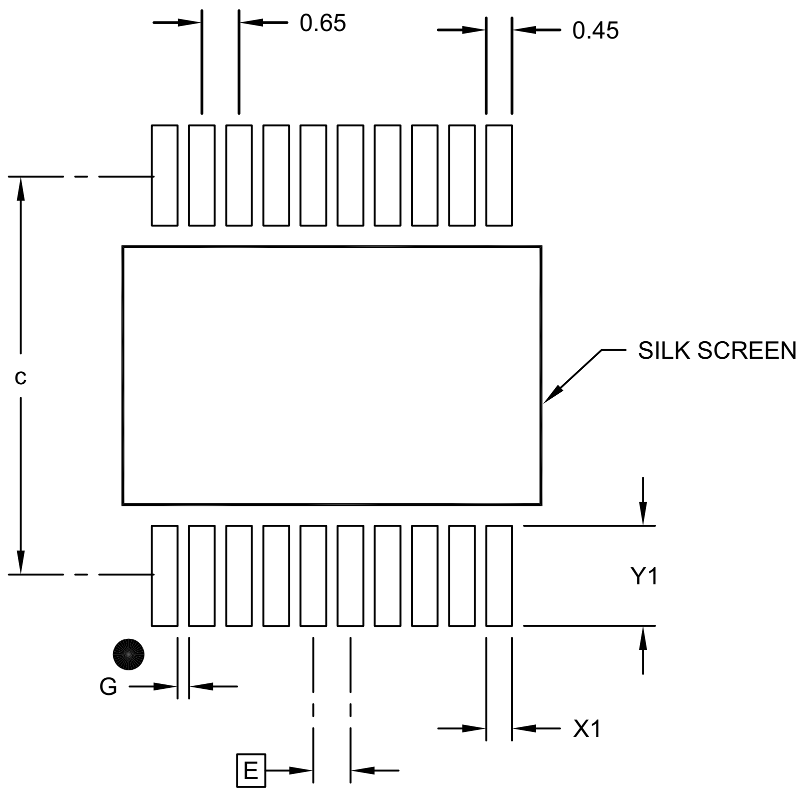
Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

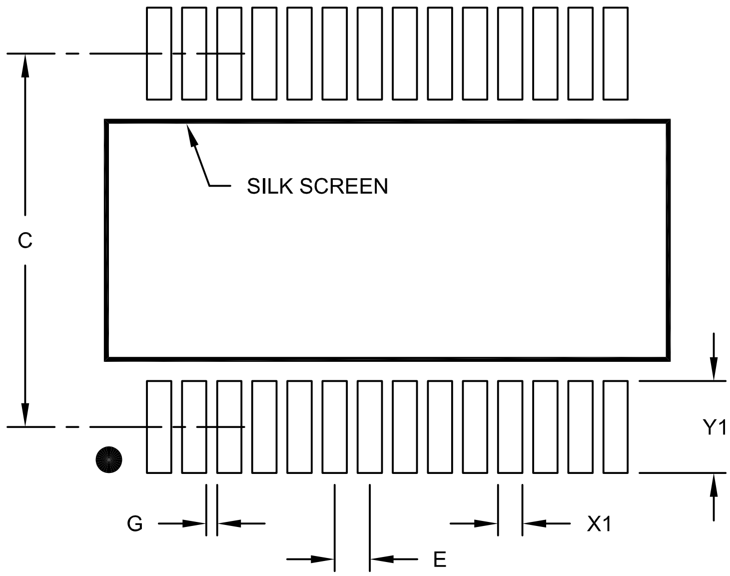
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

NOTES: