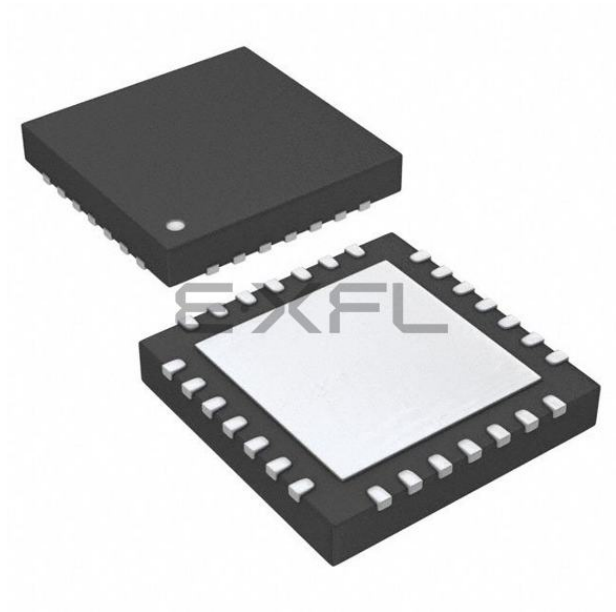
Microchip Technology - PIC32MM0016GPL028-I/ML Datasheet



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What is "Embedded - Microcontrollers"?

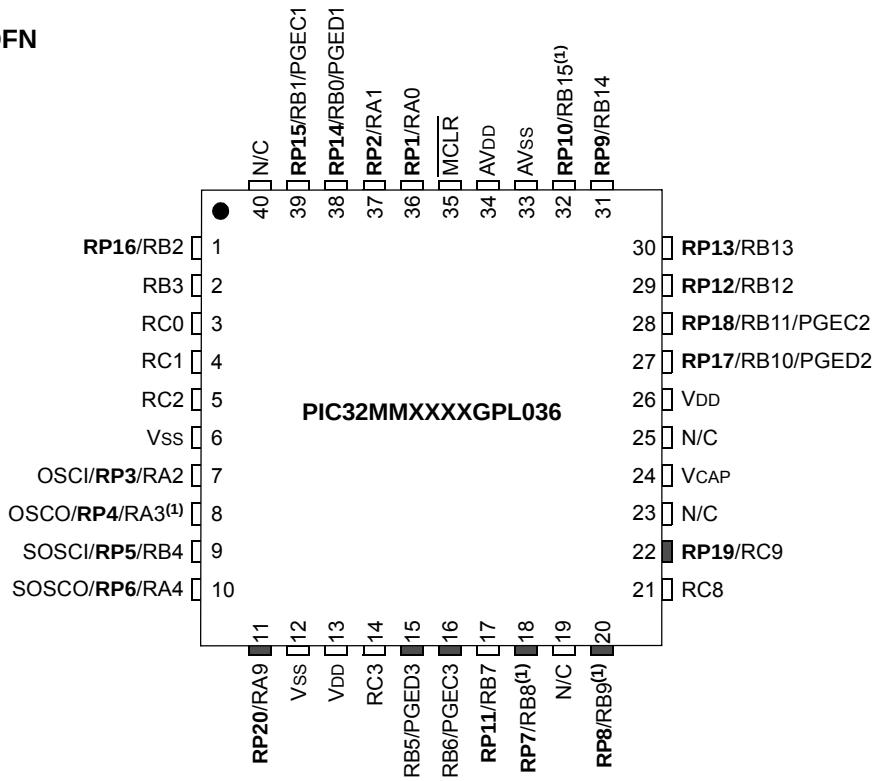
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl028-i-ml

Pin Diagrams (Continued)

40-Pin UQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

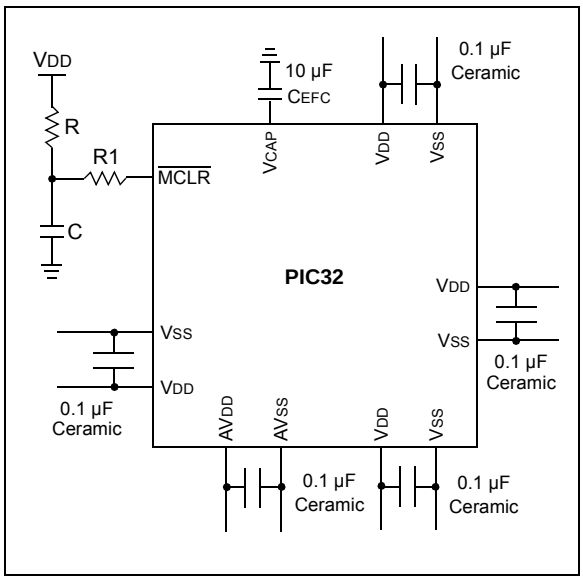
TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP16**/RB2	21	RC8
2	AN11/C1INA/RB3	22	**RP19**/RC9
3	AN12/RC0	23	N/C
4	AN13/RC1	24	VCAP
5	RC2	25	N/C
6	VSS	26	VDD
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	27	PGED2/TDO/**RP17**/RB10
8	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	28	PGEC2/TDI/**RP18**/RB11
9	SOSCI/**RP5**/RB4	29	AN7/LVDIN/**RP12**/RB12
10	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	30	AN8/**RP13**/RB13
11	**RP20**/RA9	31	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
12	VSS	32	AN10/REFCLKO/**RP10**/U1RX/$\overline{SS1}$/FSYNC1/INT0/RB15(1)
13	VDD	33	AVSS
14	RC3	34	AVDD
15	PGED3/RB5	35	$\overline{MCLR}$
16	PGEC3/RB6	36	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
17	**RP11**/RB7	37	VREF-/AN1/**RP2**/OCM1F/RA1
18	TCK/**RP7**/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	38	PGED1/AN2/C1IND/C2INB/**RP14**/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1
20	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)	40	N/C

Note 1: Pin has an increased current drive strength.

NOTES:

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides for two specific device functions:

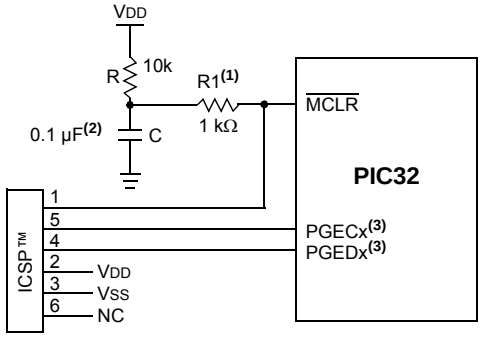
- Device Reset
- Device Programming and Debugging

Pulling The $\overline{MCLR}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{MCLR}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS(1,2,3)



Note 1: $470\Omega \leq R1 \leq 1\ k\Omega$ will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met without interfering with the debug/programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 Capacitor on Internal Voltage Regulator (V_{CAP})

A low-ESR (<1 Ohm) capacitor is required on the V_{CAP} pin, which is used to stabilize the internal voltage regulator output. The V_{CAP} pin must not be connected to V_{DD} and must have a C_{EFC} capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. The recommended value of the C_{EFC} capacitor is 10 µF. On the printed circuit board, it should be placed as close to the V_{CAP} pin as possible. If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to this capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF.

REGISTER 7-5: IFSx: INTERRUPT FLAG STATUS REGISTER x(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS<31:0>:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note 1: This register represents a generic definition of the IFSx register. Refer to Table 7-3 for the exact bit definitions.

REGISTER 7-6: IECx: INTERRUPT ENABLE CONTROL REGISTER x(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC<31-0>:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This register represents a generic definition of the IECx register. Refer to Table 7-3 for the exact bit definitions.

REGISTER 8-4: REFO1TRIM: REFERENCE OSCILLATOR TRIM REGISTER(1,2,3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to the RODIVx value
111111110 = 510/512 divisor added to the RODIVx value
•
•
•
100000000 = 256/512 divisor added to the RODIVx value
•
•
•
000000010 = 2/512 divisor added to the RODIVx value
000000001 = 1/512 divisor added to the RODIVx value
000000000 = 0 divisor added to the RODIVx value

bit 22-0 **Unimplemented:** Read as '0'

Note 1: While the ON bit (REFO1CON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

2: Do not write to this register when the ON bit (REFO1CON<15>) is not equal to the ACTIVE bit (REFO1CON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFO1CON<30:16>) = 0.

NOTES:

NOTES:

REGISTER 13-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 23 **MCLKSEL:** Master Clock Enable bit(1)
1 = REFCLKO is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator (1:1 with SYSCLK)

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** SPIx Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode

bit 12 **DISSDO:** Disable SDOx Pin bit(4)
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16/8-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
1	0	32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
0	1	16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame
0	0	16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPIx Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 26.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 9.8 "Peripheral Pin Select (PPS)"** for more information).

14.1 UART Control Registers

TABLE 14-1: UART1 AND UART2 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	U1MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
0610	U1STA(1)	31:16	UART1 MASK<7:0>								UART1 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
0620	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART1 Transmit Register								0000
0630	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART1 Receive Register								0000
0640	U1BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
0680	U2MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
0690	U2STA(1)	31:16	UART2 MASK<7:0>								UART2 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
06A0	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART2 Transmit Register								0000
06B0	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART2 Receive Register								0000
06C0	U2BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to the empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

REGISTER 15-2: RTCCON2: RTCC CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FDIV<4:0>					—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CLKSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

REGISTER 16-7: AD1CHIT: ADC COMPARE HIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CHH<13:8>(1,2)					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-0 **CHH<13:0>:** ADC Compare Hit bits(1,2)

If CM<1:0> = 11:

1 = ADC Result Buffer x has been written with data or a match has occurred

0 = ADC Result Buffer x has not been written with data

For All Other Values of CM<1:0>:

1 = A match has occurred on ADC Result Channel n

0 = No match has occurred on ADC Result Channel n

Note 1: The CHH<13:11> bits are not implemented in 20-pin devices.

2: The CHH<13:12> bits are not implemented in 28-pin devices.

REGISTER 23-3: FPOR/AFPOR: POWER-UP SETTINGS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	LPBOREN	RETVR	BOREN<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Reserved:** Program as '1'

bit 3 **LPBOREN:** Low-Power BOR Enable bit
1 = Low-Power BOR is enabled when the main BOR is disabled
0 = Low-Power BOR is disabled

bit 2 **RETVR:** Retention Voltage Regulator Enable bit
1 = Retention regulator is disabled
0 = Retention regulator is enabled and controlled by the RETEN bit during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and is disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

REGISTER 23-8: DEVID: DEVICE ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	VER<3:0>(1)				ID<27:24>(1)			
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<23:16>(1)							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<15:8>(1)							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

Note 1: Reset values are dependent on the device variant.

REGISTER 23-9: SYSKEY: SYSTEM UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SYSKEY<31:0>:** Unlock and Lock Key bits

TABLE 23-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

NOTES:

TABLE 26-5: IDLE CURRENT (I_{IDLE})(2)

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)					
Parameter No.	**Typical(1)**	**Max**	**Units**	**VDD**	**Conditions**
DC40	0.26	0.46	mA	2.0V	FSYS = 1 MHz
	0.26	0.46	mA	3.3V	
DC41	0.85	1.5	mA	2.0V	FSYS = 8 MHz
	0.85	1.5	mA	3.3V	
DC42	2.3	3.7	mA	2.0V	FSYS = 25 MHz
	2.3	3.7	mA	3.3V	
DC44	0.18	0.34	mA	2.0V	FSYS = 32 kHz
	0.18	0.34	mA	3.3V	

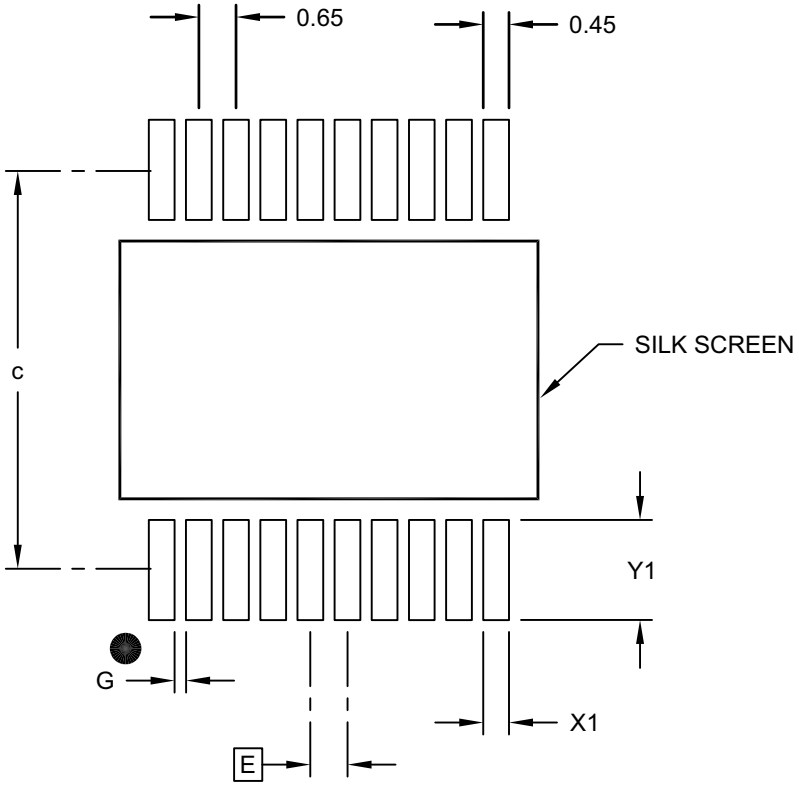
Note 1: Data in the "Typical" column is at +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with:

- Oscillator is configured in EC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = `010` and POSCMOD<1:0> (FOSCSEL<9:8>) = `00`)
- OSC1 pin is driven with external square wave with levels from 0.3V to VDD – 0.3V
- OSC2 is configured as I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = `1`)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = `00`)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = `0` and SOSCSEL (FOSCSEL<12>) = `0`)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = `00` and LPBOREN (FPOR<3>) = `0`)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = `0`)
- All I/O pins (excepting OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

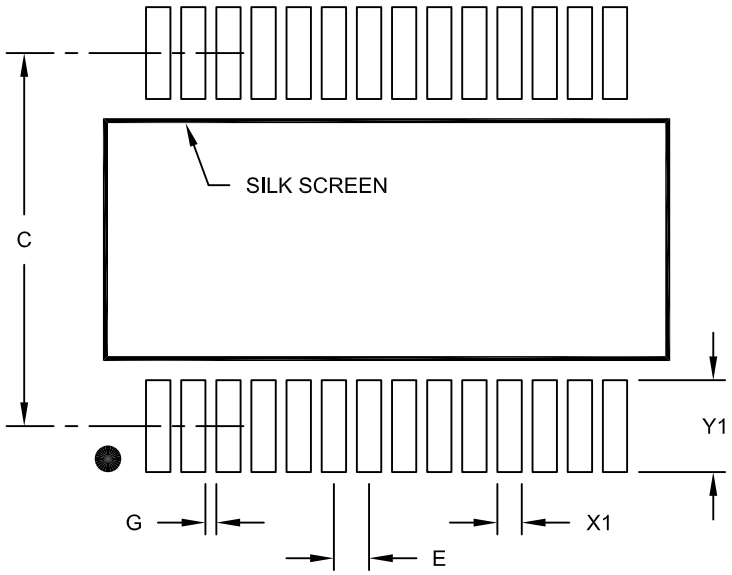
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

NOTES: