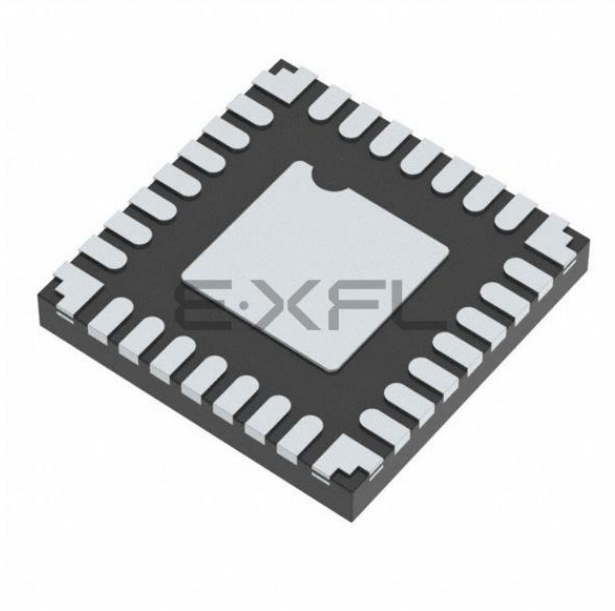

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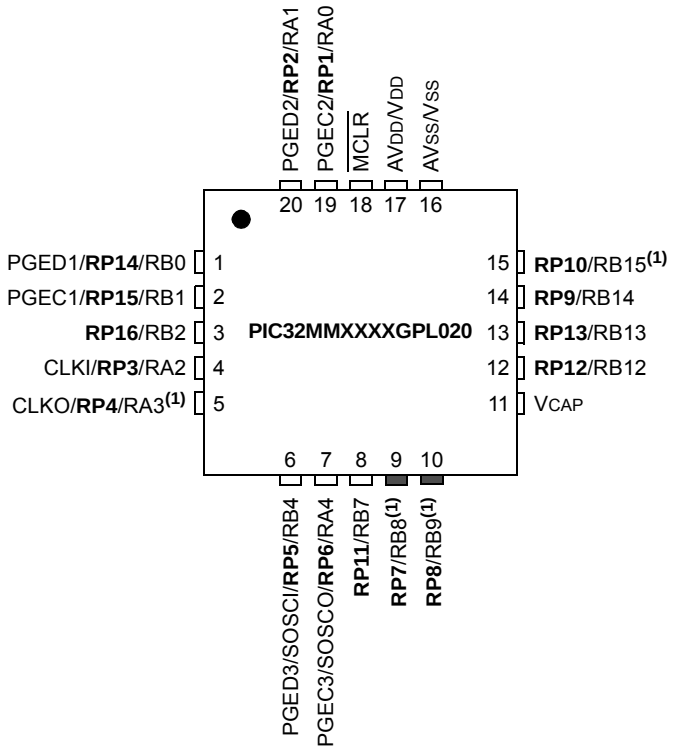
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl028t-i-m6

Pin Diagrams (Continued)

20-Pin QFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

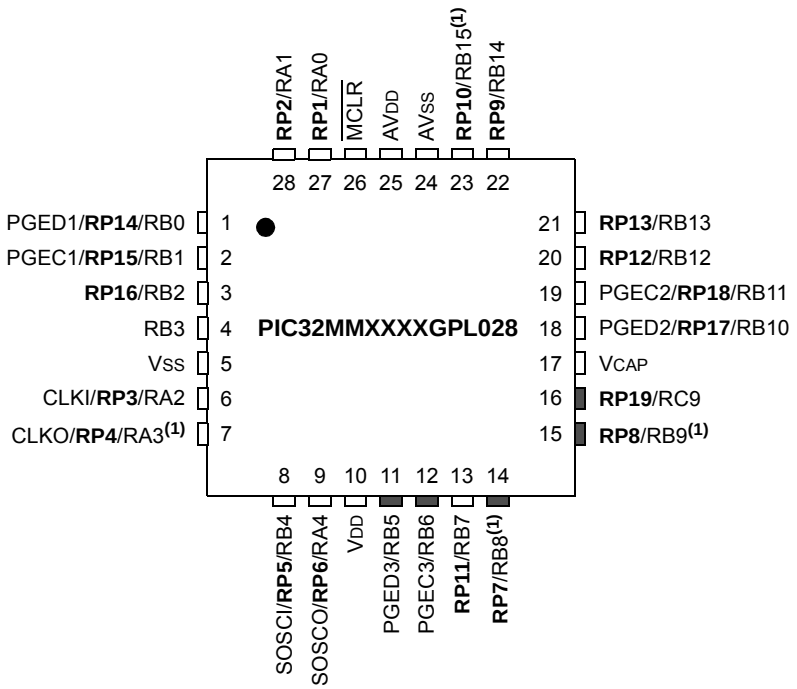
TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 20-PIN QFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	11	VCAP
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	12	TDO/AN7/LVDIN/**RP12**/RB12
3	AN4/**RP16**/RB2	13	TDI/AN8/**RP13**/RB13
4	OSC1/CLKI/AN5/C1INB/**RP3**/OCM1C/RA2	14	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
5	OSC2/CLKO/AN6/C1INA/**RP4**/OCM1D/RA3(1)	15	AN10/REFCLKO/**RP10**/U1RX/$\overline{SS1}$/FSYNC1/INT0/RB15(1)
6	PGED3/SOSCI/**RP5**/RB4	16	AVSS/VSS
7	PGEC3/SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	17	AVDD/VDD
8	**RP11**/RB7	18	$\overline{MCLR}$
9	TCK/**RP7**/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	19	PGEC2/VREF+/AN0/**RP1**/OCM1E/INT3/RA0
10	TMS/REFCLKI/**RP8**/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)	20	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

Pin Diagrams (Continued)

28-Pin QFN/UQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: Pin has an increased current drive strength. Refer to **Section 26.0 "Electrical Characteristics"** for details.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/**RP14**/RB0	15	TMS/REFCLKI/**RP8**/T1CK/T1G/U1RTS/U1BCLK/SDO1/C2OUT/OCM1B/INT2/RB9(1)
2	PGEC1/AN3/C1INC/C2INA/**RP15**/RB1	16	**RP19**/RC9
3	AN4/C1INB/**RP16**/RB2	17	VCAP
4	AN11/C1INA/RB3	18	PGED2/TDO/**RP17**/RB10
5	VSS	19	PGEC2/TDI/**RP18**/RB11
6	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	20	AN7/LVDIN/**RP12**/RB12
7	OSC2/CLKO/AN6/**RP4**/OCM1D/RA3(1)	21	AN8/**RP13**/RB13
8	SOSCI/**RP5**/RB4	22	CDAC1/AN9/**RP9**/RTCC/U1TX/SDI1/C1OUT/INT1/RB14
9	SOSCO/SCLKI/**RP6**/PWRLCLK/RA4	23	AN10/REFCLKO/**RP10**/U1RX/SS1/FSYNC1/INT0/RB15(1)
10	VDD	24	AVSS
11	PGED3/RB5	25	AVDD
12	PGEC3/RB6	26	MCLR
13	**RP11**/RB7	27	VREF+/AN0/**RP1**/OCM1E/INT3/RA0
14	TCK/**RP7**/U1CTS/SCK1/OCM1A/RB8(1)	28	VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: Pin has an increased current drive strength.

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS60001108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 21. "UART"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 60. "32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS60001336)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

TABLE 1-1: PIC32MM0064GPL036 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	20-Pin QFN	20-Pin SSOP	28-Pin QFN/ UQFN	28-Pin SPDIP/ SSOP/SOIC	36-Pin VQFN	40-Pin UQFN			
RP1	19	2	27	2	33	36	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	20	3	28	3	34	37	I/O	ST/DIG	
RP3	4	7	6	9	7	7	I/O	ST/DIG	
RP4	5	8	7	10	8	8	I/O	ST/DIG	
RP5	6	9	8	11	9	9	I/O	ST/DIG	
RP6	7	10	9	12	10	10	I/O	ST/DIG	
RP7	9	12	14	17	18	18	I/O	ST/DIG	
RP8	10	13	15	18	19	20	I/O	ST/DIG	
RP9	14	17	22	25	28	31	I/O	ST/DIG	
RP10	15	18	23	26	29	32	I/O	ST/DIG	
RP11	8	11	13	16	17	17	I/O	ST/DIG	
RP12	12	15	20	23	26	29	I/O	ST/DIG	
RP13	13	16	21	24	27	30	I/O	ST/DIG	
RP14	1	4	1	4	35	38	I/O	ST/DIG	
RP15	2	5	2	5	36	39	I/O	ST/DIG	
RP16	3	6	3	6	1	1	I/O	ST/DIG	
RP17	—	—	18	21	24	27	I/O	ST/DIG	
RP18	—	—	19	22	25	28	I/O	ST/DIG	
RP19	—	—	16	19	21	22	I/O	ST/DIG	
RP20	—	—	—	—	11	11	I/O	ST/DIG	
RTCC	14	17	22	25	28	31	O	DIG	Real-Time Clock alarm/seconds output
SCK1	9	12	14	17	18	18	I/O	ST/DIG	SPI1 clock (input or output)
SCLKI	7	10	9	12	10	10	I	ST	Secondary Oscillator external clock input
SDI1	14	17	22	25	28	31	I	ST	SPI1 data input
SDO1	10	13	15	18	19	20	O	DIG	SPI1 data output
SOSCI	6	9	8	11	9	9	—	—	Secondary Oscillator crystal
SOSCO	7	10	9	12	10	10	—	—	Secondary Oscillator crystal
$\overline{SS1}$	15	18	23	26	29	32	I	ST	SPI1 slave select input
T1CK	10	13	15	18	19	20	I	ST	Timer1 external clock input
T1G	10	13	15	18	19	20	I	ST	Timer1 clock gate input
TCK	9	12	14	17	18	18	I	ST	JTAG clock input
TDI	13	16	19	22	25	28	I	ST	JTAG data input
TDO	12	15	18	21	24	27	O	DIG	JTAG data output
TMS	10	13	15	18	19	20	I	ST	JTAG mode select input
U1BCLK	10	13	15	18	19	20	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{U1CTS}$	9	12	14	17	18	18	I	ST	UART1 transmission control input
$\overline{U1RTS}$	10	13	15	18	19	20	O	DIG	UART1 reception control output
U1RX	15	18	23	26	29	32	I	ST	UART1 receive data input
U1TX	14	17	22	25	28	31	O	DIG	UART1 transmit data output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output ANA = Analog level input/output

The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information is available by accessing the CP0 registers listed in Table 3-2.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	C000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	0003
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	—	WDTR	SWNMI	—	—	—	GNMI	—	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	SBOREN	RETEN	VREGS	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	VS<6:0>						
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22-16 **VS<6:0>**: Vector Spacing bits

Spacing Between Vectors:
0000000 = 0 Bytes
0000001 = 8 Bytes
0000010 = 16 Bytes
0000100 = 32 Bytes
0001000 = 64 Bytes
0010000 = 128 Bytes
0100000 = 256 Bytes
1000000 = 512 Bytes
All other values are reserved. The operation of this device is undefined if a reserved value is written to this field. If MVEC = 0, this field is ignored.

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multivector Configuration bit

1 = Interrupt controller configured for Multivectored mode
0 = Interrupt controller configured for Single Vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of Group Priority 7 or lower start the interrupt proximity timer
110 = Interrupts of Group Priority 6 or lower start the interrupt proximity timer
101 = Interrupts of Group Priority 5 or lower start the interrupt proximity timer
100 = Interrupts of Group Priority 4 or lower start the interrupt proximity timer
011 = Interrupts of Group Priority 3 or lower start the interrupt proximity timer
010 = Interrupts of Group Priority 2 or lower start the interrupt proximity timer
001 = Interrupts of Group Priority 1 start the interrupt proximity timer
000 = Disables interrupt proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER (CONTINUED)

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>(1)				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
11111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

8.2 Oscillator Control Registers

TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			—	—	—	—	—	—	—	—	0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN	xx0x
2020	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>								0001
		15:0	—	—	—	—	—	—	—	—	PLLICLK	—	—	—	—	—	—	—	0000
20A0	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
20B0	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
21D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	SPDIVRDY	FRCRDY	0000
2200	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the FOSCSEL Configuration bits and the type of Reset.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

17.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

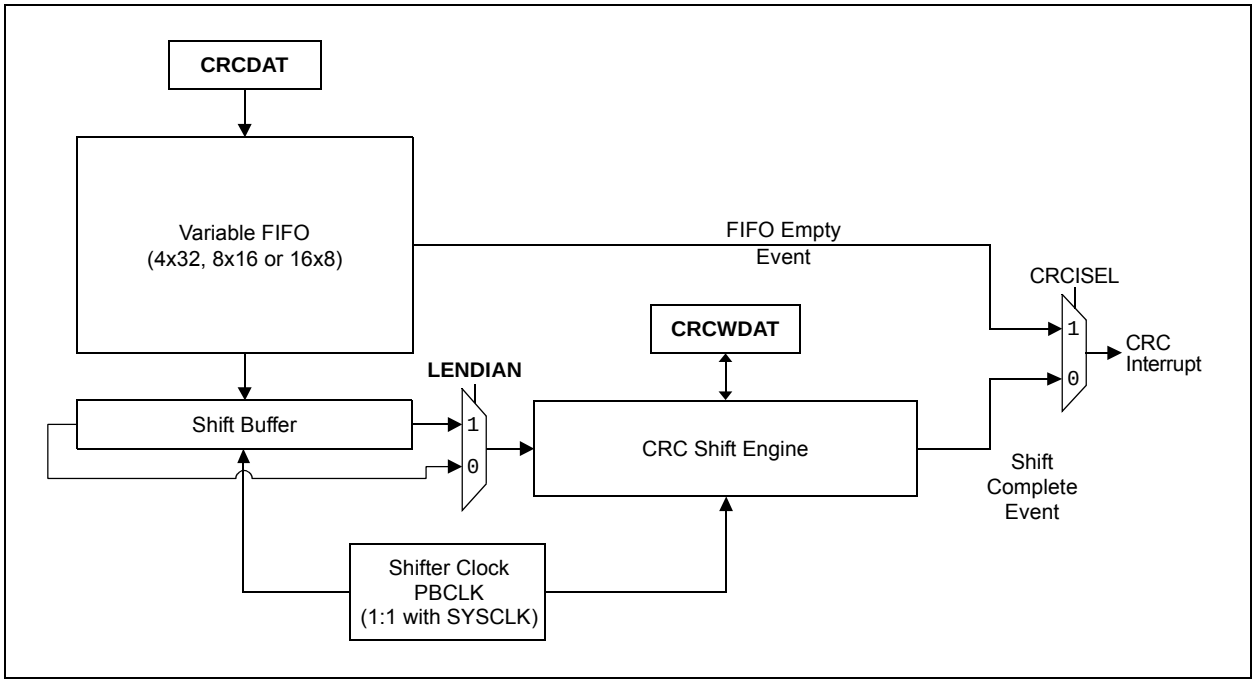
Note: This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 60. "32-Bit Programmable Cyclic Redundancy Check"** (DS60001336) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 17-1 displays a simplified block diagram of the CRC generator.

FIGURE 17-1: CRC BLOCK DIAGRAM



REGISTER 18-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits

For CLC1:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART1 RX input
011 = SPI1 SDO output
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin

For CLC2:
111 = SCCP3 compare match event
110 = SCCP2 compare match event
101 = SCCP2 OCM2 output
100 = UART2 RX input
011 = SPI2 SDO output
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

For CLC1:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion (EOC) event
011 = UART1 TX output
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:
111 = Reserved
110 = MCCP1 compare match event
101 = Reserved
100 = ADC End-of-Conversion event
011 = UART2 TX output
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

111 = MCCP1 OCM1C output
110 = MCCP1 OCM1B output
101 = MCCP1 OCM1A output
100 = REFCLKO output
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (FSYS)
000 = CLCINA I/O pin

REGISTER 18-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 1
0 = The Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 1
0 = The Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

NOTES:

22.4 On-Chip Voltage Regulator Low-Power Modes

The main on-chip regulator always consumes an incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode and/or Retention mode. Standby mode is controlled by the VREGS bit (PWRCON<0>), and Retention mode is controlled by the RETEN (PWRCON<1>) and RETVR (FPOR<2>) bits. The available Regulator Low-Power modes are listed in Table 22-2. For more information about the wake-up time and the current consumption for different modes, refer to the electrical specifications listed in Table 26-6 and Table 26-22.

TABLE 22-2: VOLTAGE REGULATOR LOW-POWER MODES

Mode	VREGS Bit (PWRCON<0>)	RETEN Bit (PWRCON<1>)	RETVR Bit (FPOR<2>)	Wake-up Time (Table 26-22)	Current (Table 26-6)
Normal	1	0	1	Fastest	Highest
Standby Only	0	0	1	Medium	Medium
Retention Only	1	1	0	Medium	Medium
Standby and Retention	0	1	0	Slowest	Lowest

22.4.1 REGULATOR STANDBY MODE

Whenever the device goes into Sleep mode, the regulator can be made to enter Standby mode. This feature is controlled by the VREGS bit (PWRCON<0>). Clearing the VREGS bit enables Standby mode. If Standby mode is used, the voltage regulator needs some time to switch to normal operation mode and generate output. During this time, the code execution is disabled. The delay is applied every time the device resumes operation after Standby mode.

22.4.2 REGULATOR RETENTION MODE

When in Sleep mode, the device can use a separate low-power, low-voltage/retention regulator to power critical circuits. This regulator, which operates at 1V nominal, maintains power to data RAM, WDT, Timer1 and the RTCC, while all other core digital logic is powered down. The low-voltage/retention regulator is available only when Sleep mode is invoked. It is controlled by the RETVR Configuration bit (FPOR<2>) and in firmware by the RETEN bit (PWRCON<1>). RETVR must be programmed to zero (= 0) and the RETEN bit must be set (= 1) for the retention regulator to be enabled.

22.5 Low-Power Brown-out Reset

The PIC32MM0064GPL036 family devices have a second low-power Brown-out Reset circuit with a reduced precision of the trip point. This low-power BOR circuit can be activated when the main BOR is disabled. The circuit is enabled by programming the LPBOREN Configuration bit (FPOR<3>) to '1'.

TABLE 23-7: UNIQUE DEVICE IDENTIFIER (UDID) REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1840	UDID1	31:16	UDID Word 1<31:0>																xxxx
		15:0																	xxxx
1844	UDID2	31:16	UDID Word 2<31:0>																xxxx
		15:0																	xxxx
1848	UDID3	31:16	UDID Word 3<31:0>																xxxx
		15:0																	xxxx
184C	UDID4	31:16	UDID Word 4<31:0>																xxxx
		15:0																	xxxx
1850	UDID5	31:16	UDID Word 5<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 23-8: RESERVED REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	RESERVED1	31:16	Reserved Register 1<31:0>																0000
		15:0																	0000
0480	RESERVED2	31:16	Reserved Register 2<31:0>																0000
		15:0																	0000
2280	RESERVED3	31:16	Reserved Register 3<31:0>																0C00
		15:0																	0000

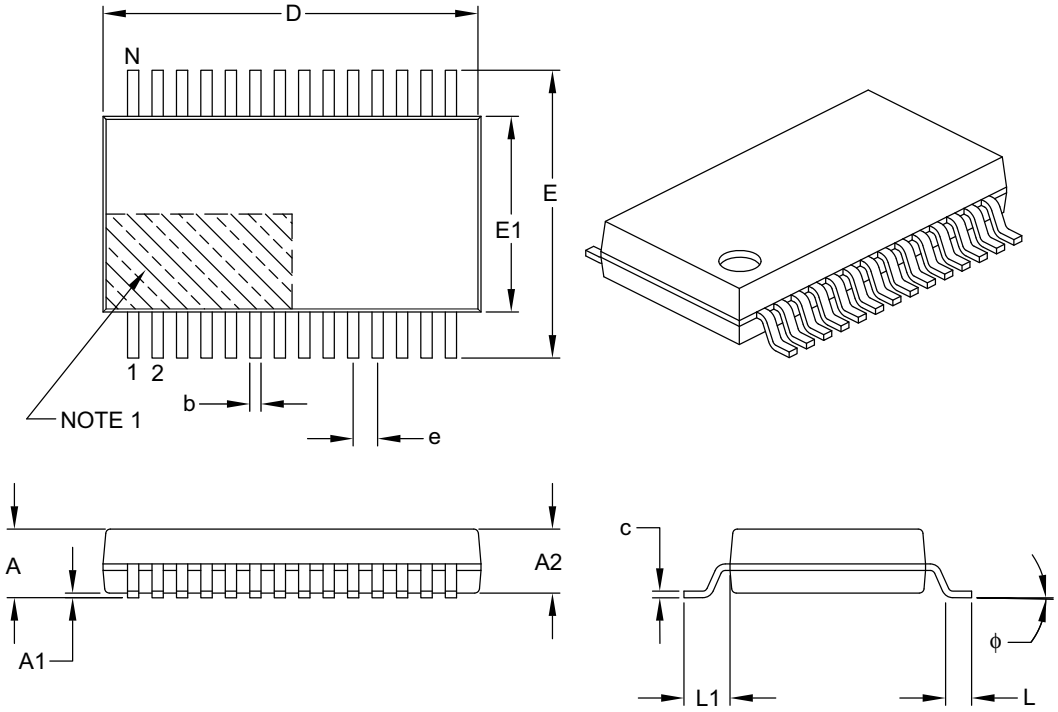
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

NOTES:

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

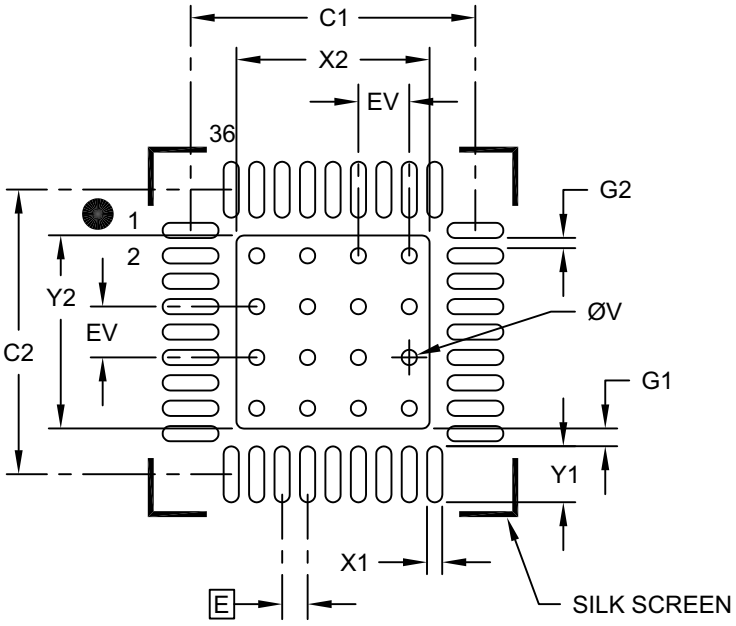
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.60	
Contact Pad Spacing	C2		5.60	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			1.10
Contact Pad to Center Pad (X36)	G1	0.35		
Space Between Contact Pads (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2