**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 29 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 14x10/12b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-VFQFN Exposed Pad |
| Supplier Device Package | 36-SQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0016gpl036-i-m2 |

## 3.0 CPU

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0064GPL036 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

### 3.1 Features

The PIC32MM0064GPL036 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
  - Multiply-add and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero and one detect instructions
  - `WAIT` instruction
  - Conditional move instructions
  - Vectored interrupts
  - Atomic interrupt enable/disable
  - One GPR shadow set to minimize latency of interrupts
  - Bit field manipulation instructions
- microMIPS™ Instruction Set:
  - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
  - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
  - Added seventeen new and thirty-five MIPS32® corresponding commonly used instructions in 16-bit opcode format.
  - Stack Pointer implicit in instruction.
  - MIPS32 assembly and ABI compatible.
- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
  - Configurable using high-performance multiplier array.
  - Maximum issue rate of one 32x16 multiply per clock.
  - Maximum issue rate of one 32x32 multiply every other clock.
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
  - No minimum frequency: 0 MHz.
  - Power-Down mode (triggered by `WAIT` instruction).
- EJTAG Debug/Profiling:
  - CPU control with start, stop and single stepping.
  - Software breakpoints via the `SDBBP` instruction.
  - Optional simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
  - PC and/or load/store address sampling for profiling.
  - Performance counters.
  - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0064GPL036 family processor core is shown in Figure 3-1.

## 4.0 MEMORY ORGANIZATION

PIC32MM microcontrollers provide 4 Gbytes of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The data memory can be made executable, allowing the CPU to execute code from data memory.

Key features include:

- 32-Bit Native Data Width
- Separate Boot Flash Memory (BFM) for Protected Code
- Robust Bus Exception Handling to Intercept Runaway Code
- Simple Memory Mapping with Fixed Mapping Translation (FMT) Unit

The PIC32MM0064GPL036 family devices implement two address spaces: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions. Physical addresses are used by peripherals, such as Flash controllers, that access memory independently of the CPU.

The virtual address space is divided into two segments of 512 Mbytes each, labeled kseg0 and kseg1. The Program Flash Memory (PFM) and Data RAM Memory (DRM) are accessible from either kseg0 or kseg1, while the Boot Flash Memory (BFM) and peripheral SFRs are accessible only from kseg1.

The Fixed Mapping Translation (FMT) unit translates the memory segments into corresponding physical address regions. Figure 4-1 through Figure 4-3 illustrate the fixed mapping scheme, implemented by the PIC32MM0064GPL036 family core, between the virtual and physical address space.

The mapping of the memory segments depends on the CPU error level, set by the ERL bit in the CPU STATUS Register (SR). Error level is set (ERL = 1) by the CPU on a Reset, Soft Reset or NMI. In this mode, the CPU can access memory by the physical address. This mode is provided for compatibility with other MIPS® processor cores that use a TLB-based MMU. The C start-up code clears the ERL bit to zero, so that when application software starts up, it sees the proper virtual to physical memory mapping.

### 4.1 Alternate Configuration Bits Space

Every Configuration Word has an associated Alternate Word (designated by the letter A as the first letter in the name of the word). During device start-up, Primary Words are read, and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and Alternate Words are used. If uncorrectable ECC errors are found in Primary and Alternate Words, the BCFGFAIL (RCON<26>) flag is set, and the default configuration is used. The Primary Configuration bits area is located at the address range, from 0x1FC01780 to 0x1FC017E8. The Alternate Configuration bits area is located at the address range, from 0x1FC01700 to 0x1FC01768.

**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-1, HS | R/W-1, HS | U-0 | U-0 | R/W-0, HS | R/W-0, HS | U-0 | U-0 |
| | PORIO | PORCORE | — | — | BCFGERR | BCFGFAIL | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS | U-0 |
| | — | — | — | — | — | — | CMR | — |
| 7:0 | R/W-0, HS | R/W-0, HS | U-0 | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-1, HS | R/W-1, HS |
| | EXTR | SWR | — | WDTO | SLEEP | IDLE(2) | BOR | POR |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **PORIO:** VDD POR Flag bit
Set by hardware at detection of a VDD POR event.
1 = A Power-on Reset has occurred due to VDD voltage
0 = A Power-on Reset has not occurred due to VDD voltage

bit 30 **PORCORE:** Core Voltage POR Flag bit
Set by hardware at detection of a core POR event.
1 = A Power-on Reset has occurred due to core voltage
0 = A Power-on Reset has not occurred due to core voltage

bit 29-28 **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary Configuration registers
0 = No error occurred during a read of the Primary Configuration registers

bit 26 **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary and Alternate Configuration registers
0 = No error occurred during a read of the Primary and Alternate Configuration registers

bit 25-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

**Note 1:** User software must clear bits in this register to view the next detection.
**2:** The IDLE bit will also be set when the device wakes from Sleep mode.

**REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | VS<6:0> | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-23 **Unimplemented:** Read as '0'

bit 22-16 **VS<6:0>**: Vector Spacing bits

Spacing Between Vectors:
0000000 = 0 Bytes
0000001 = 8 Bytes
0000010 = 16 Bytes
0000100 = 32 Bytes
0001000 = 64 Bytes
0010000 = 128 Bytes
0100000 = 256 Bytes
1000000 = 512 Bytes
All other values are reserved. The operation of this device is undefined if a reserved value is written to this field. If MVEC = 0, this field is ignored.

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multivector Configuration bit

1 = Interrupt controller configured for Multivectored mode
0 = Interrupt controller configured for Single Vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of Group Priority 7 or lower start the interrupt proximity timer
110 = Interrupts of Group Priority 6 or lower start the interrupt proximity timer
101 = Interrupts of Group Priority 5 or lower start the interrupt proximity timer
100 = Interrupts of Group Priority 4 or lower start the interrupt proximity timer
011 = Interrupts of Group Priority 3 or lower start the interrupt proximity timer
010 = Interrupts of Group Priority 2 or lower start the interrupt proximity timer
001 = Interrupts of Group Priority 1 start the interrupt proximity timer
000 = Disables interrupt proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

**REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)**

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 5 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 4 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 4 uses Shadow Set 0

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 3 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 2 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
- 1111 = Reserved
- •
- •
- •
- 0010 = Reserved
- 0001 = Interrupt with a priority level of 1 uses Shadow Set 1
- 0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
- 1 = Single vector is presented with a shadow set
- 0 = Single vector is not presented with a shadow set

**Note 1:** These bits are ignored if the MVEC bit (INTCON<12>) = 0.

## 9.0 I/O PORTS

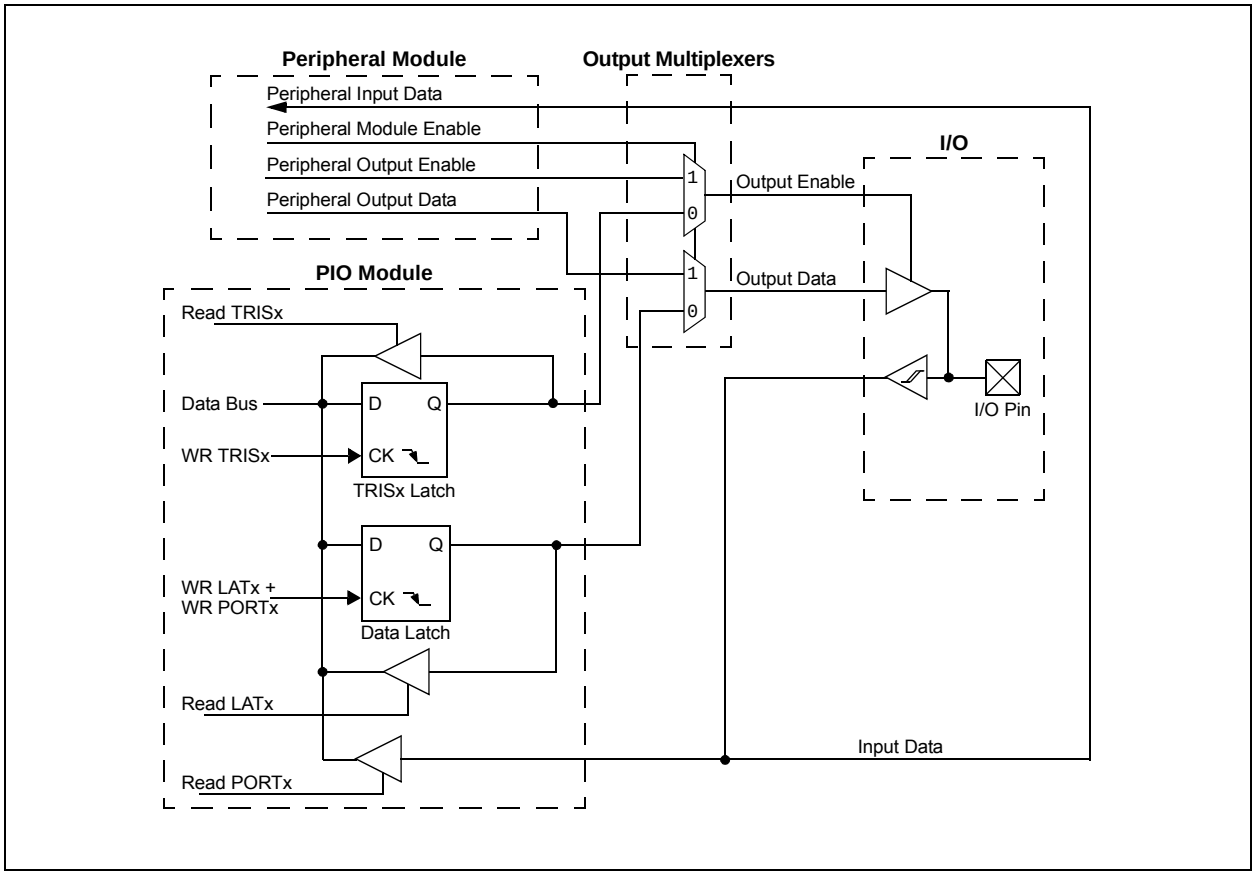
**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

Many of the device pins are shared among the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. Some pins in the devices are 5V tolerant pins. Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when Change-in-Pin State is Detected
- Operation during Sleep and Idle modes
- Fast Bit Manipulation using the CLR, SET and INV registers

Figure 9-1 illustrates a block diagram of a typical multiplexed I/O port.

**FIGURE 9-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**



**REGISTER 13-2: SPIxCON2: SPIx CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SPISGNEXT | — | — | FRMERREN | SPIROVEN | SPITUREN | IGNROV | IGNTUR |
| 7:0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | AUDEN(1) | — | — | — | AUDMONO(1,2) | — | AUDMOD<1:0>(1,2) | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** SPIx Sign-Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign-extended
0 = Data from RX FIFO is not sign-extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame error overflow generates error events
0 = Frame error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive Overflow (ROV) generates error events
0 = Receive Overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit Underrun (TUR) generates error events
0 = Transmit Underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow (ROV) bit (for audio data transmissions)
1 = A ROV is not a critical error; during ROV, data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error which stops SPIx operation

bit 8 **IGNTUR:** Ignore Transmit Underrun (TUR) bit (for audio data transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error which stops SPIx operation

bit 7 **AUDEN:** Enable Audio Codec Support bit(1)
1 = Audio protocol is enabled
0 = Audio protocol is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
1 = Audio data is mono (each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bits(1,2)
11 = PCM/DSP mode
10 = Right Justified mode
01 = Left Justified mode
00 = $I^2S$ mode

**Note 1:** These bits can only be written when the ON bit = 0.
**2:** These bits are only valid for AUDEN = 1.

**REGISTER 14-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to the empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

**TABLE 16-1: ADC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(3) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0700 | ADC1BUF0 | 31:16 | ADC1BUF0<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0710 | ADC1BUF1 | 31:16 | ADC1BUF1<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0720 | ADC1BUF2 | 31:16 | ADC1BUF2<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0730 | ADC1BUF3 | 31:16 | ADC1BUF3<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0740 | ADC1BUF4 | 31:16 | ADC1BUF4<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0750 | ADC1BUF5 | 31:16 | ADC1BUF5<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0760 | ADC1BUF6 | 31:16 | ADC1BUF6<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0770 | ADC1BUF7 | 31:16 | ADC1BUF7<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0780 | ADC1BUF8 | 31:16 | ADC1BUF8<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0790 | ADC1BUF9 | 31:16 | ADC1BUF9<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 07A0 | ADC1BUF10 | 31:16 | ADC1BUF10<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 07B0 | ADC1BUF11 | 31:16 | ADC1BUF11<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 07C0 | ADC1BUF12 | 31:16 | ADC1BUF12<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 07D0 | ADC1BUF13 | 31:16 | ADC1BUF13<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** The CSS<13:11> and CHH<13:11> bits are not implemented in 20-pin devices.

**2:** The CSS<13:12> and CHH<13:12> bits are not implemented in 28-pin devices.

**3:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**REGISTER 16-5: AD1CHS: ADC INPUT SELECT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CH0NA<2:0> | | | CH0SA<4:0>(1) | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-5 **CH0NA<2:0>:** Negative Input Select bits
111-001 = Reserved
000 = Negative input is AVSS

bit 4-0 **CH0SA<4:0>:** Positive Input Select bits(1)
11111 = Reserved
11110 = Positive input is AVDD
11101 = Positive input is AVSS
11100 = Positive input is Band Gap Reference (VBG)
11011-01110 = Reserved
01101 = Positive input is AN13(2,3)
01100 = Positive input is AN12(2,3)
01011 = Positive input is AN11(2)
01010 = Positive input is AN10
01001 = Positive input is AN9
01000 = Positive input is AN8
00111 = Positive input is AN7
00110 = Positive input is AN6
00101 = Positive input is AN5
00100 = Positive input is AN4
00011 = Positive input is AN3
00010 = Positive input is AN2
00001 = Positive input is AN1
00000 = Positive input is AN0

**Note 1:** The CH0SA<4:0> positive input selection is only used when CSCNA (AD1CON2<10>) = 0 and ASEN (AD1CON5<15>) = 0. The AD1CSS bits specify the positive inputs when CSCNA = 1 or ASEN = 1.

**2:** This option is not implemented in the 20-pin devices.

**3:** This option is not implemented in the 28-pin devices.

## 23.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MM0064GPL036 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. "Programming and Diagnostics"** (DS61129) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

### 23.1 Configuration Bits

PIC32MM0064GPL036 family devices contain a Boot Flash Memory (BFM) with an associated configuration space. All Configuration Words are listed in Table 23-3 and Table 23-4; Register 23-1 through Register 23-6 describe the configuration options.

### 23.2 Code Execution from RAM

PIC32MM0064GPL036 family devices allow executing the code from RAM. The starting boundary of this special RAM space can be adjusted using the EXECADDR<7:0> bits in the CFGCON register with a 1-Kbyte step. Writing a non-zero value to these bits will move the boundary, effectively reducing the total amount of program memory space in RAM. Refer to Table 23-5 and Register 23-7 for more information.

### 23.3 Device ID

The Device ID identifies the device used. The ID can be read from the DEVID register. The Device IDs for PIC32MM0064GPL036 family devices are listed in Table 23-1. Also refer to Table 23-5 and Register 23-8 for more information.

**TABLE 23-1: DEVICE IDs FOR PIC32MM0064GPL036 FAMILY DEVICES**

| Device | DEVID |
|---|---|
| PIC32MM0016GPL020 | 0x06B04053 |
| PIC32MM0032GPL020 | 0x06B0C053 |
| PIC32MM0064GPL020 | 0x06B14053 |
| PIC32MM0016GPL028 | 0x06B02053 |
| PIC32MM0032GPL028 | 0x06B0A053 |
| PIC32MM0064GPL028 | 0x06B12053 |
| PIC32MM0016GPL036 | 0x06B06053 |
| PIC32MM0032GPL036 | 0x06B0E053 |
| PIC32MM0064GPL036 | 0x06B16053 |

### 23.4 System Registers Write Protection

The critical registers in the PIC32MM0064GPL036 family devices are protected (locked) from an accidental write. If the registers are locked, a special unlock sequence is required to modify the content of these registers.

To unlock the registers, the following steps should be done:

1. Disable interrupts prior to the system unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the SYSKEY register, in two back-to-back assembly or 'C' instructions.
3. Write the new value to the required register.
4. Write a non-key value (such as 0x00000000) to the SYSKEY register to perform a lock.
5. Re-enable interrupts.

The registers that require this unlocking sequence are listed in Table 23-2.

**TABLE 23-2: SYSTEM LOCKED REGISTERS**

| Register Name | Register Description | Peripheral |
|---|---|---|
| OSCCON | Oscillator Control | Oscillator |
| SPLLCON | System PLL Control | Oscillator |
| OSCTUN | FRC Tuning | Oscillator |
| PMDCON | Peripheral Module Disable Control | PMD |
| RSWRST | Software Reset | Reset |
| RPCON | Peripheral Pin Select Configuration | I/O Ports |
| RNMICON | Non-Maskable Interrupt Control | Reset |
| PWRCON | Power Control | Reset |
| RTCCON1 | RTCC Control 1 | RTCC |

The SYSKEY register read value indicates the status. A value of '0' indicates the system registers are locked. A value of '1' indicates the system registers are unlocked. For more information about the SYSKEY register, refer to Table 23-5 and Register 23-9.

**TABLE 23-4: ALTERNATE CONFIGURATION WORDS SUMMARY**

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31\15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 |
| 1740 | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 1744 | AFDEVOPT | 31:16 | USERID<15:0> | | | | | | | | | | | | | | | |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | SOSCHP | r-1 | r-1 | r-1 |
| 1748 | AFICD | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | ICS<1:0> | | JTAGEN | r-1 | r-1 |
| 174C | AFPOR | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | LPBOREN | RETVR | BOREN<1:0> | |
| 1750 | AFWDT | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | FWDTEN | RCLKSEL<1:0> | | RWDTPS<4:0> | | | | | WINDIS | FWDTWINSZ<1:0> | | SWDTPS<4:0> | | | | |
| 1754 | AFOSCSEL | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | FCKSM<1:0> | | r-1 | SOSCSEL | r-1 | OSCIOFNC | POSCMOD<1:0> | | IESO | SOSCEN | r-1 | PLLSRC | r-1 | FNOSC<2:0> | | |
| 1758 | AFSEC | 31:16 | CP | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 175C | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 1760 | RESERVED | 31:16 | r-0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| 1764 | RESERVED | 31:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | | 15:0 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |

**Legend:** r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

**REGISTER 23-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/P | R/P | r-1 | R/P | r-1 | R/P | R/P | R/P |
| | FCKSM<1:0> | | — | SOSCSEL | — | OSCIOFNC | POSCMOD<1:0> | |
| 7:0 | R/P | R/P | r-1 | R/P | r-1 | R/P | R/P | R/P |
| | IESO | SOSCEN | — | PLLSRC | — | FNOSC<2:0> | | |

| Legend: | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
- 1 = Crystal is used (RA4 and RB4 pins are controlled by SOSC)
- 0 = External clock is connected to the SOSCO pin (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
- 1 = OSC2/CLKO pin operates as normal I/O
- 0 = System clock is connected to the OSC2/CLKO pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Secondary Oscillator is enabled
- 0 = Secondary Oscillator is disabled

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

**REGISTER 23-7: CFGCON: CONFIGURATION CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | r-0 | U-0 | r-0 | r-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EXECADDR<7:0> | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-y | U-0 | r-1 | r-1 |
| | — | — | — | — | JTAGEN | — | — | — |

| **Legend:** | r = Reserved bit | y = Value set from Configuration bits on Reset |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **Reserved:** Must be written as '0'

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **Reserved:** Must be written as '0'

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits

11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at the 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at the 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit

1 = JTAG port is enabled
0 = JTAG port is disabled
The Reset value of this bit is the value of the JTAGEN (FICD<2>) Configuration bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Must be written as '1'

## 24.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 24.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 24.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 24.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

**TABLE 26-3: OPERATING VOLTAGE SPECIFICATIONS**

| **Operating Conditions:** 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Max** | **Units** | **Conditions** |
| DC10 | VDD | **Supply Voltage** | 2.0 | 3.6 | V | |
| DC16 | VPOR(1) | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | VSS | — | V | |
| DC17A | SVDD(1) | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.05 | — | V/ms | 0-3.3V in 66 ms, 0-2.0V in 40 ms |
| DC17B | VBOR | **Brown-out Reset Voltage** on VDD Transition, High-to-Low | 2.0 | 2.22 | V | |

**Note 1:** If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

**TABLE 26-14: COMPARATOR SPECIFICATIONS**

| **Operating Conditions:** 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(2)** | **Max** | **Units** |
| D300 | VIOFF | Input Offset Voltage | -20 | — | 20 | mV |
| D301 | VICM | Input Common-Mode Voltage | AVSS – 0.3V | — | AVDD + 0.3V | V |
| D307 | TRESP(1) | Response Time | — | 150 | — | ns |

**Note 1:** Measured with one input at VDD/2 and the other transitioning from VSS to VDD.

**2:** Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**TABLE 26-15: VOLTAGE REFERENCE SPECIFICATIONS**

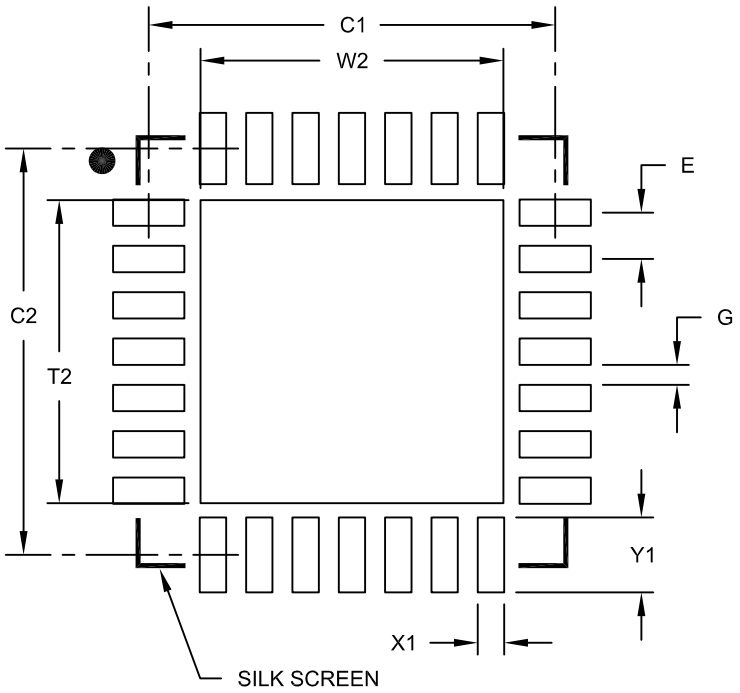
| **Operating Conditions:** 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(2)** | **Max** | **Units** |
| VRD310 | TSET | Settling Time(1) | — | — | 10 | µs |
| VRD311 | VRA | Accuracy | -1 | — | 1 | LSb |
| VRD312 | VRUR | Unit Resistor Value (R) | — | 4.5 | — | kΩ |

**Note 1:** Measures the interval while VRDAT<4:0> transitions from '11111' to '00000'.

**2:** Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

### 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 4.25 |
| Optional Center Pad Length | T2 | | | 4.25 |
| Contact Pad Spacing | C1 | | 5.70 | |
| Contact Pad Spacing | C2 | | 5.70 | |
| Contact Pad Width (X28) | X1 | | | 0.37 |
| Contact Pad Length (X28) | Y1 | | | 1.00 |
| Distance Between Pads | G | 0.20 | | |

Notes:

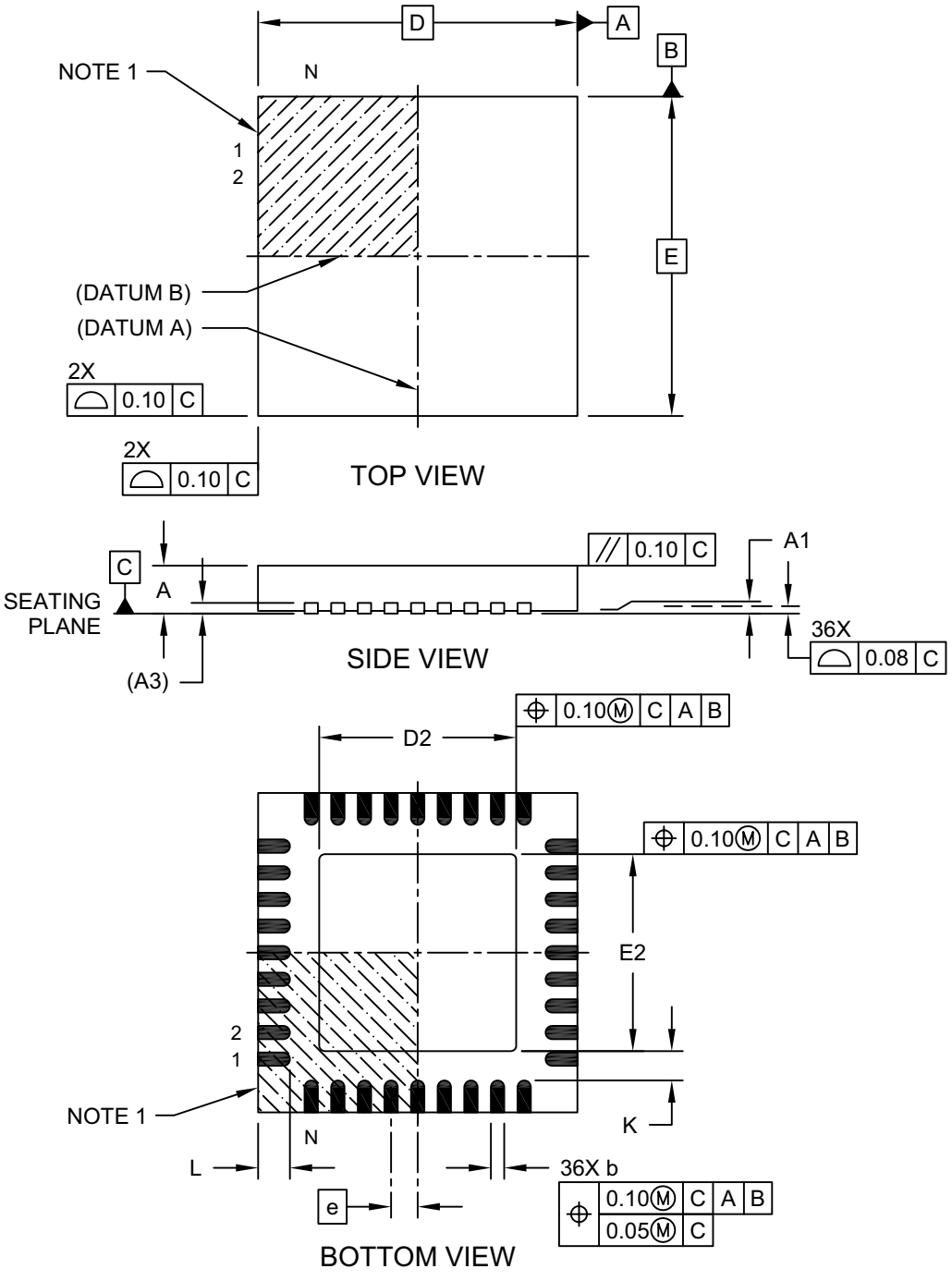
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

**36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]**
**SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2

**NOTES:**